National Semiconductor

June 1992

# DS0025C Two Phase MOS Clock Driver

## General Description

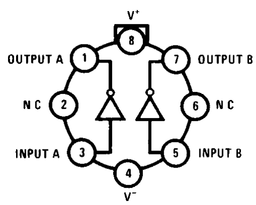
The DS0025C is a monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL line drivers or buffers such as the DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse width may be set by selection of the input capacitor eliminating the need for tight input pulse control.

## Features

- 8-lead TO-5 or 8-lead or 14-lead dual-in-line package
- High Output Voltage Swings—up to 25V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DS8830, DM7440
- “Zero” Quiescent Power

## Connection Diagrams

**Metal Can Package**



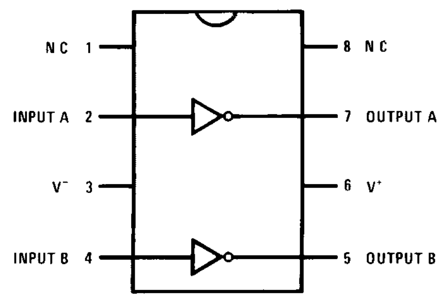

TL/F/5852–1

Note: Pin 4 connected to case.

**Top View**

**Order Number DS0025CH**
**See NS Package Number H08C**

**Dual-In-Line Package**

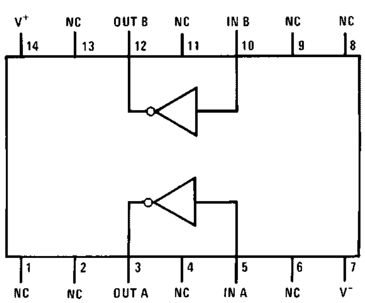



TL/F/5852–2

**Top View**

**Order Number DS0025CJ-8**
**or DS0025CN**
**See NS Package Number J08A or N08E**

**Dual-In-Line Package**




TL/F/5852–3

**Top View**

**Order Number DS0025CJ**
**See NS Package Number J14A**



RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| $(V^+ - V^-)$Voltage Differential | 25V |
| Input Current | 100 mA |
| Peak Output Current | 1.5A |
| Storage Temperature | −65°C to +150°C |
| Operating Temperature | 0°C to +85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

## Recommended Operating Conditions

| | Min | Max |
|---|---|---|
| $V^+$ $V^-$ Differential Voltage | | 20V |
| Temperature | 0 | 70 |
| Maximum Power Dissipation* at 25°C | | |
| 8-Pin Cavity Package | | 1150 mW |
| 14-Pin Cavity Package | | 1410 mW |
| Molded Package | | 1080 mW |
| Metal Can (TO-5) Package | | 670 mW |

* Derate 8-pin cavity package 7.8 mW/°C above 25°C; derate 14-pin cavity package 9.5 mW/°C above 25°C; derate molded package 8.7 mW/°C above 25°C; derate metal can (TO-5) package 4.5 mW/°C above 25°C.

## Electrical Characteristics (Notes 2 and 3) See test circuit.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{d\ ON}$ | Turn-On Delay Time | $C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$ | | | 15 | 30 | ns |
| $t_{RISE}$ | Rise Time | $C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$ | | | 25 | 50 | ns |
| $t_{d\ OFF}$ | Turn-Off Delay Time | $C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$ (Note 4) | | | 30 | 60 | ns |
| $t_{FALL}$ | Fall Time | $C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$ | (Note 4) | 60 | 90 | 120 | ns |
| | | | (Note 5) | 100 | 150 | 250 | ns |
| PW | Pulse Width (50% to 50%) | $C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$ (Note 5) | | | 500 | | ns |
| $V_{O+}$ | Positive Output Voltage Swing | $V_{IN} = 0V$, $I_{OUT} = -1$ mA | | $V^+ - 1.0$ | $V^+ - 0.7V$ | | V |
| $V_{O-}$ | Negative Output Voltage Swing | $I_{IN} = 10$ mA, $I_{OUT} = 1$ mA | | | $V^- + 0.7V$ | $V^- + 1.5V$ | V |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

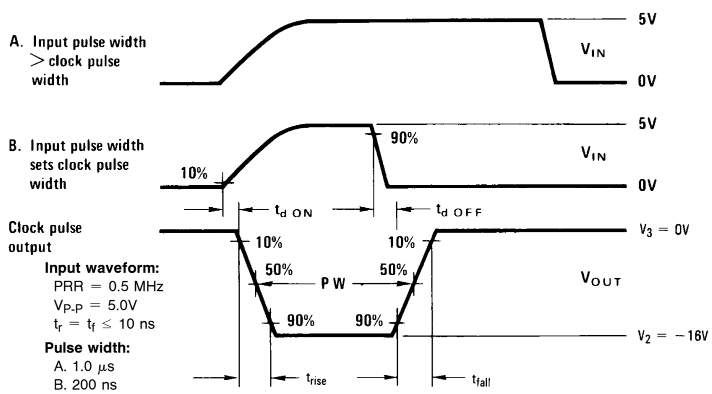
**Note 2:** Unless otherwise specified min/max limits apply across the 0°C to 70°C range for the DS0025C.

**Note 3:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

**Note 4:** Parameter values apply for clock pulse width determined by input pulse width.

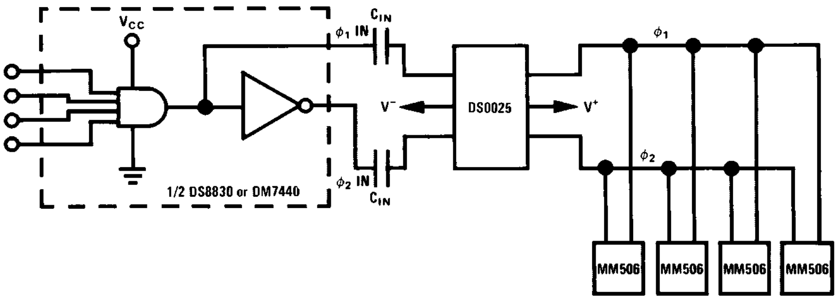
**Note 5:** Parameter values for input width greater than output clock pulse width.

## Timing Diagram



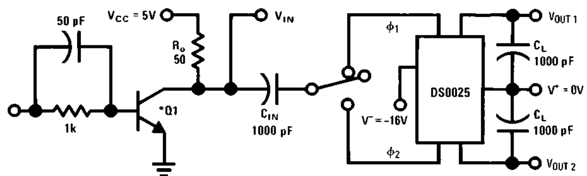

TL/F/5852–5

## Typical Application




TL/F/5852–4

## AC Test Circuit

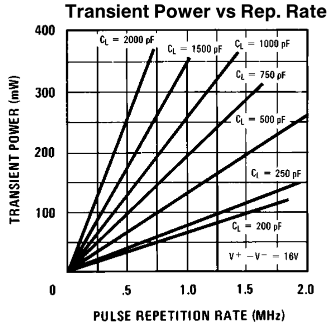



TL/F/5852–6

*Q1 is selected high speed NPN switching transistor.

## Typical Performance

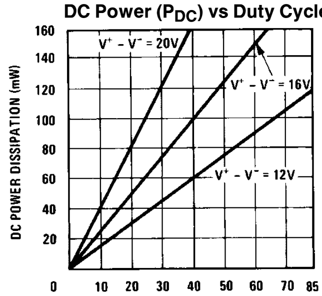
**Transient Power vs Rep. Rate**




TL/F/5852–7

$P_{AC} = (V^+ - V^-)^2 f C_L$

**DC Power ($P_{DC}$) vs Duty Cycle**

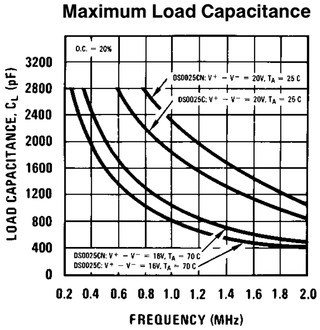



TL/F/5852–8

DUTY CYCLE (%)

$$P_{DC} = \frac{(V^+ - V^-)^2\ (DC)}{1k}$$

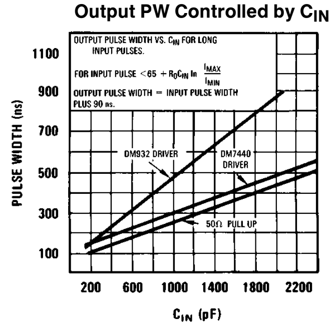
**Maximum Load Capacitance**




TL/F/5852–9

$$C_L < \frac{(P_{MAX})\ (1k) - (V^+ - V^-)^2\ (DC)}{(f)\ (1k)\ (V^+ - V^-)^2} < \frac{(I_{pk})\ (t_r)}{V^+ - V^-}$$

**Output PW Controlled by $C_{IN}$**




TL/F/5852–10

$I_{MAX}$ = Peak Current delivered by driver

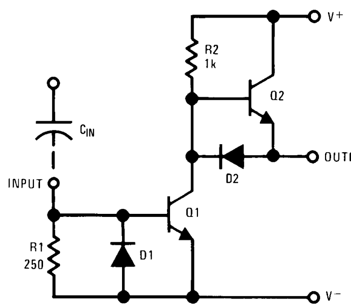
$$I_{MIN} \frac{V_{BE}}{R1} = \frac{0.6}{1k}$$

## Applications Information

### Circuit Operation

Input current forced into the base of $Q_1$ through the coupling capacitor $C_{IN}$ causes $Q_1$ to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that $Q_1$ turns off, $Q_2$ receives base drive through $R_2$, turning $Q_2$ on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.




TL/F/5852–11

**FIGURE 1. DS0025 Schematic (One-Half Circuit)**

It may be noted that $Q_1$ must switch off before $Q_2$ begins to supply current, hence high internal transients currents from $V^-$ to $V^+$ cannot occur.

### Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

### Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns. For $V^+ - V^- = 20V$, $I = 0.8A$.

### Transient Output Power

The average transient power ($P_{ac}$) dissipated, is equal to the energy needed to charge and discharge the output capacitive load ($C_L$) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, $f = 1.0$ MHz, $C_L = 1000$ pF, $P_{AC} = 400$ mW.

### Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

$$= 80 \text{ mW for } V^+ - V^- = 20V, DC = 20\%$$

### Package Power Dissipation

Total average power = transient output power + internal power.

## Example Calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30–50 ns and 16V amplitude over the temperature range 0°–70°C?

**Power Dissipation:**

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

**Transient Peak Current Limitation:**

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

**Average Internal Power:**

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power.

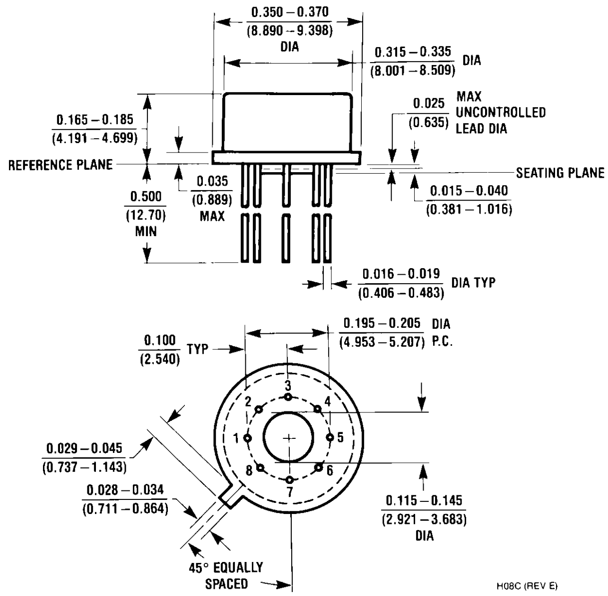
385 mW = transient output power.

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

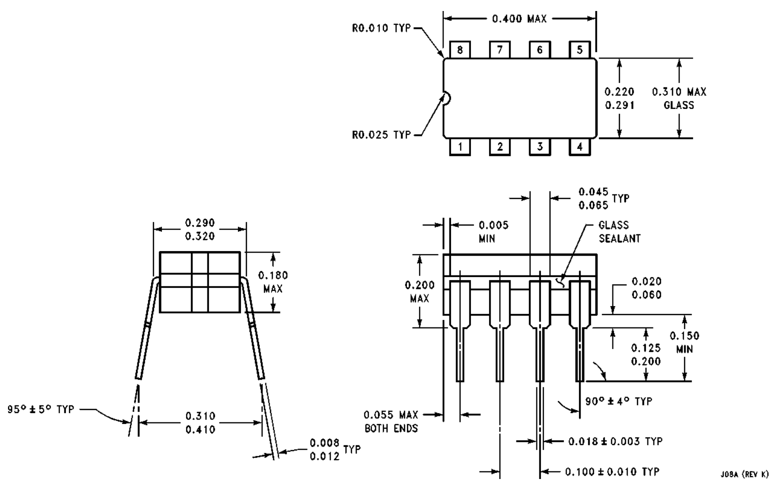
From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

For further information please refer to National Semiconductors Application Note AN-76.

## **Physical Dimensions** inches (millimeters)

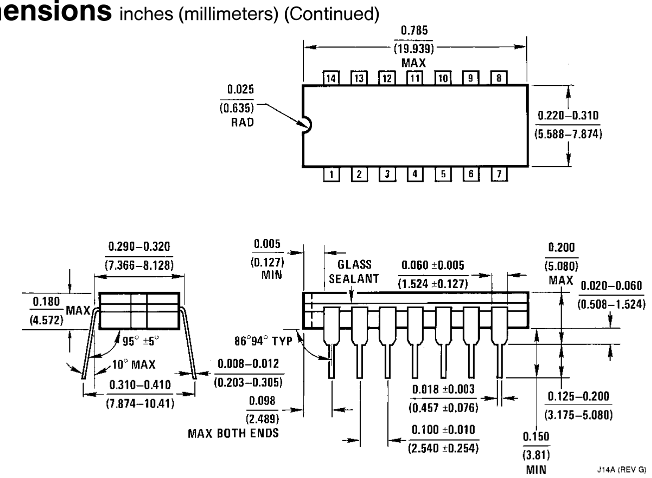



**Order Number DS0025CH**
**NS Package Number H08C**

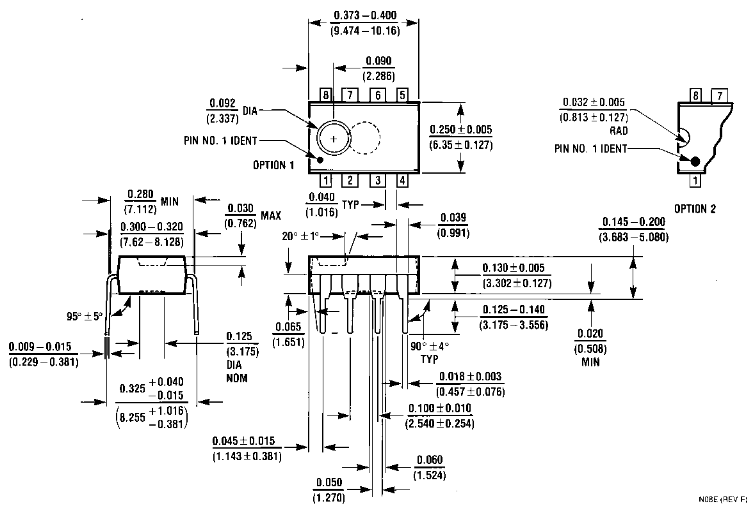



**Order Number DS0025CJ**
**NS Package Number J08A**

## Physical Dimensions inches (millimeters) (Continued)




**Order Number DS0025CJ**
**NS Package Number J14A**




**Order Number DS0025CN**
**NS Package Number N08E**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**National Semiconductor Corporation**
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

**National Semiconductor Europe**
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**
Tel: 81-043-299-2309
Fax: 81-043-299-2408