PLESSEY
Semiconductors

T-73-53

SP9687

ULTRA FAST COMPARATOR

The SP9687 is an ultra-fast dual comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be operated in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is high, and $\overline{LE}$ is low, the comparator latch is transparent. When LE is driven low and $\overline{LE}$ high, the outputs are latched, see Fig.3. If the latch function is not used, LE must be connected to ECL HI (or ground) and LE to ECL LO.

The device is pin compatible with the AM687 and operates from conventional +5V and -5.2V rails.

FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- 50 ohm Line Driving Capability
- Excellent Common Mode Rejection
- Supply Voltages +5V, -5.2V
- Operating Temperature Range:
  SP9687 — -30°C to +85°C
  SP9687AC — -55°C to +125°C
- Pin Compatible with AD9687
- Pin Compatible with AM687 — But Faster
- Comparators within each SP9687 are matched as follows:
  Input to Output Delay Matching 200ps (typ)
  Latch to Output Delay Matching 200ps (typ)

ORDERING INFORMATION

SP9687DG (Industrial - Ceramic DIL package)
SP9687BB DG (Plessey High Reliability Ceramic DIL package)
SP9687MP (Industrial - Miniature Plastic package)
SP9687AC DG (Military - Ceramic DIL package)

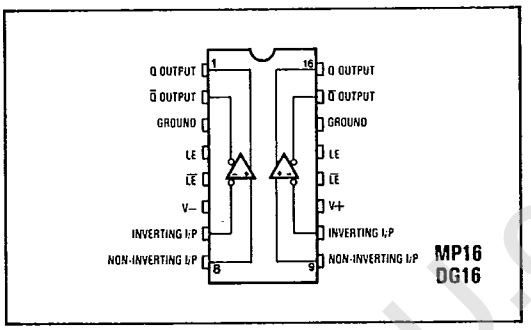
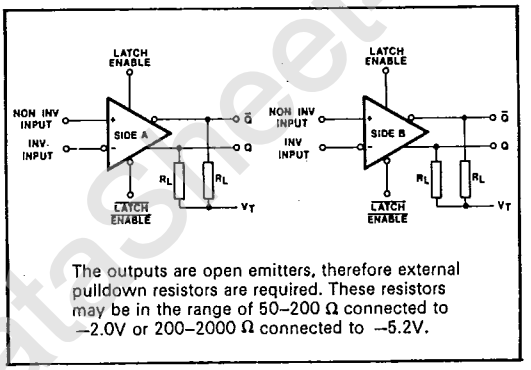


Fig.1 Pin connections



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to −2.0V or 200–2000 Ω connected to −5.2V.

Fig.2 Functional diagram

NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

OPERATING NOTES

Timing diagram

The timing diagram, Fig. 3, shows in graphic form a sequence of events in the SP9687. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strob operation, and the output transitions occur after a time $t_{pd(E)}$. The LE input is omitted for clarity.

ABSOLUTE MAXIMUM RATINGS T-73-53

Postive supply voltage	6V
Negative supply voltage	-6V
Output current	30mA
Input voltage	±3V
Differential input voltage	3.5V
Differential latch voltage	3.5V
Power dissipation	590mW
Storage temperature range	-65°C to +150°C
Junction operating temperature	<175°C
Lead temperature (soldering 60 sec)	300°C

Thermal characteristics

DG16	θ_{JA} = 110°C/W
	θ_{JC} = 33°C/W
LC20	θ_{JA} = 73°C/W
	θ_{JC} = 22°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = -30°C to +85°C: V_{CC} = 5.0V ± 0.25V: V_{EE} = -5.2V ± 0.25V:
R_L = 50Ω: V_T = -2.0V (see Fig.2)

Characteristic	Value Min.	Value Max.	Units	Conditions
Input offset voltage	-5	+5	mV	Rs < 100Ω 25°C
	-7	+7	mV	Rs < 100Ω
Input bias current		20	μA	25°C
		30	μA	
Input offset current		5	μA	25°C
		8	μA	
Input resistance	60		kΩ	25°C
Input capacitance		3	pF	25°C
Supply current I_{EE}		68	mA	Note 2 25°C
		75	mA	
Supply current Icc		46	mA	Note 2 25°C
		50	mA	
Common mode range	-2.5	+2.5	V	
Output logic levels				
Output high	-0.96	-0.81	V	25°C
	-1.045	-0.875	V	T_{amb} = Min.
	-0.89	-0.70	V	T_{amb} = Max.
Output low	-1.85	-1.65	V	25°C
	-1.89	-1.65	V	T_{amb} = Min.
	-1.83	-1.575	V	T_{amb} = Max.
Min. latch set up time		1	ns	Notes 1, 3, 4 25°C
		2	ns	
Input to output delay		3	ns	Notes 1, 3 (Q and $\overline{Q}$) 25°C
		4	ns	
Latch to output delay		3	ns	Notes 1, 3, 4 (Q and $\overline{Q}$) 25°C
		4.5	ns	
Minimum latch pulse width		3	ns	Note 1 25°C
Minimum hold time		1	ns	Note 1 25°C

NOTES

1. Guaranteed but not tested.
2. Refers to entire package. Other data in this table applies to each half.
3. ±100mV pulse with -10mV overdrive. See Figs 6 to 8.
4. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.

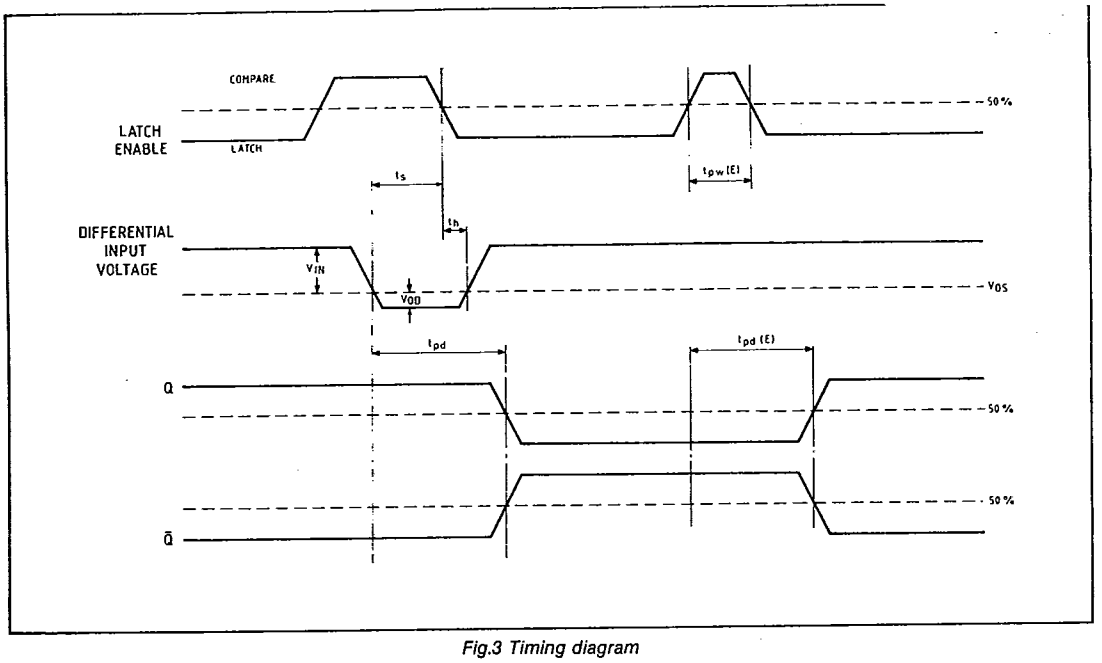


Fig.3 Timing diagram

PERFORMANCE CURVES

Unless otherwise specified, standard conditions for all curves are T_{amb} = 25°C, V_{CC} = 5.0V, V_{EE} = -5.2V

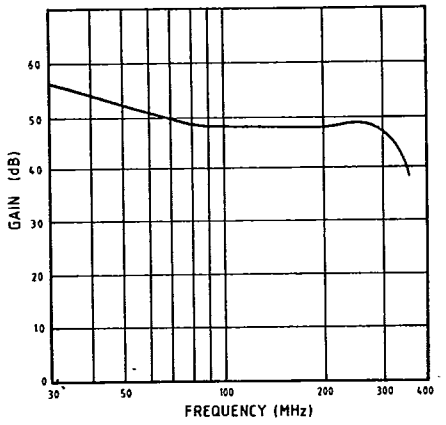


Fig.4 Open loop gain as a function of frequency

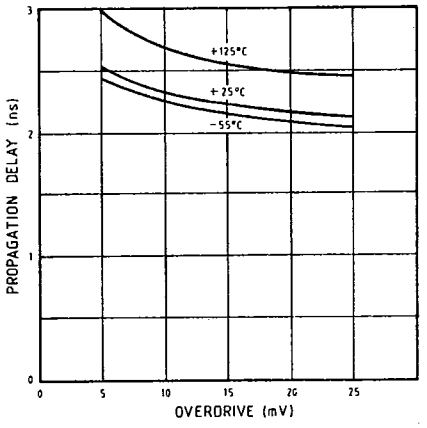


Fig.5 Propagation delay, latch to output as a function of overdrive

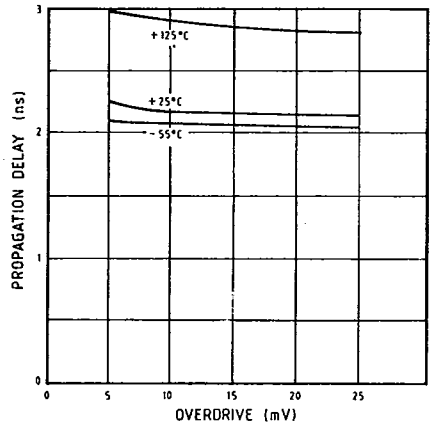


Fig.6 Propagation delay, input to output as a function of overdrive

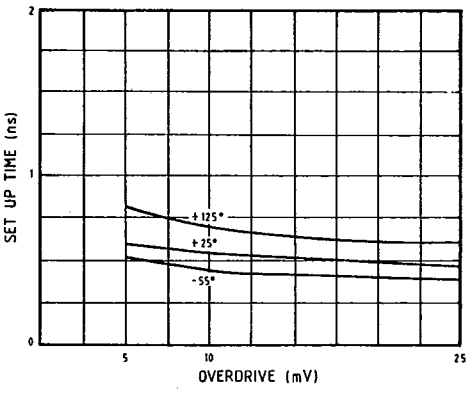


Fig.7 Set-up time as a function of temperature

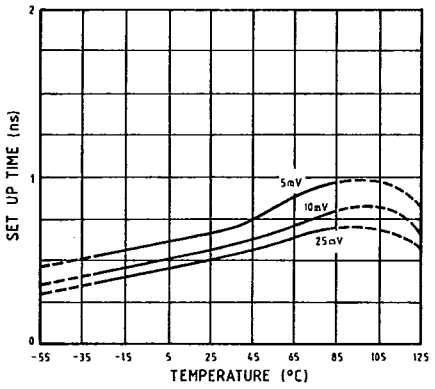


Fig.8 Set-up time as a function of input overdrive

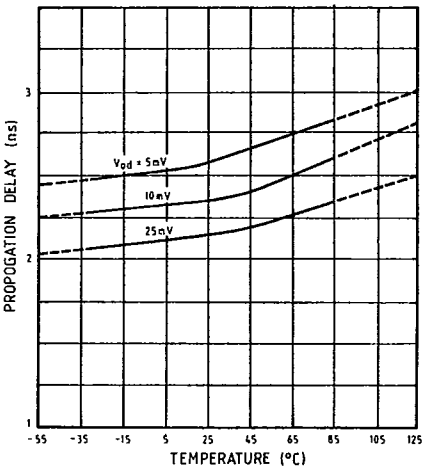


Fig.9 Propagation delay, input to output as a function of temperature

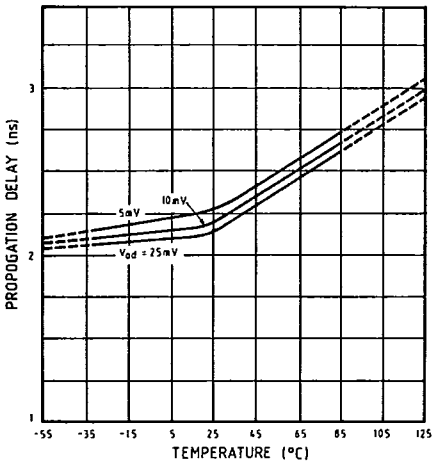


Fig.10 Propagation delay, latch to output as a function of temperature

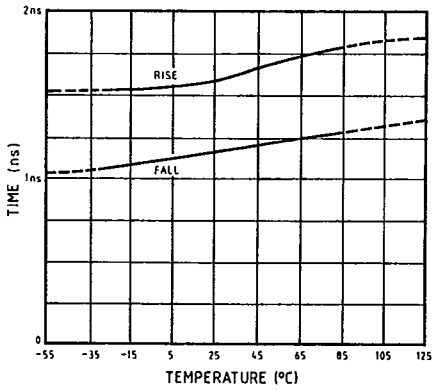


Fig.11 Output rise and fall times as a function of temperature

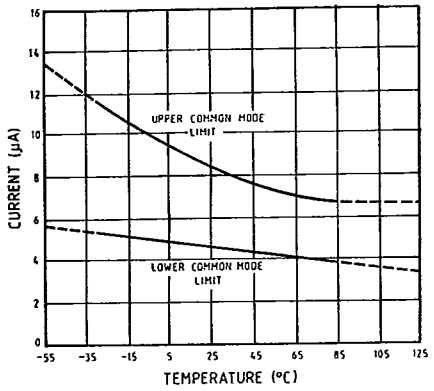


Fig.12 Input bias currents as a function of temperature

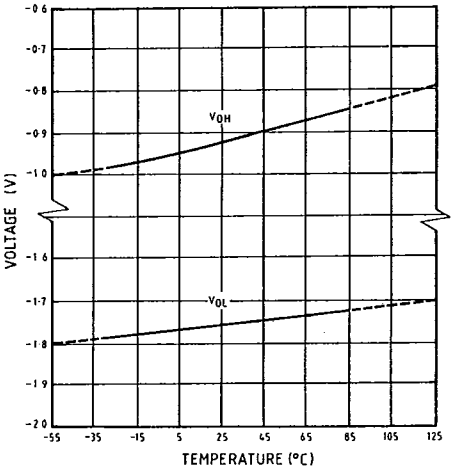


Fig.13 Output levels as a function of temperature

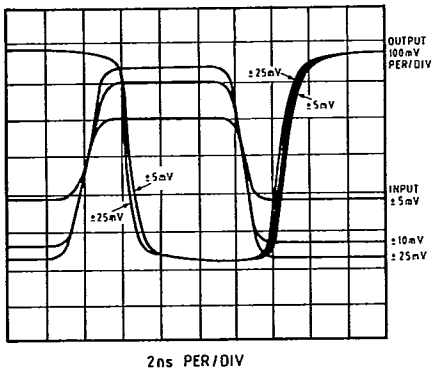


Fig.14 Response to various input signals levels