M52393P/FP

EDTV2 IDENTIFICATION SIGNAL DETECTOR

DESCRIPTION

The M52393 are integrated-circuits of a semiconductor, developed especially for EDTV2 identification signal detection.

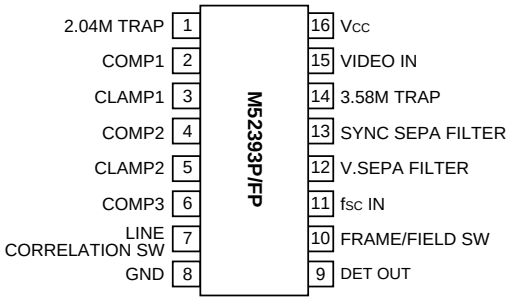
In contrast to such ICs, few products on the IC market had the simple function of detecting identification signals. For that purpose, many manufacturers had to combine discrete components (non-ICs) with gate arrays. There was a great demand for ICs that enabled cost reduction.

In order to satisfy demand, we have developed the EDTV2 identification signal processing ICs that include all necessary capabilities for detection (synchronous signal separation, line counter, filters, level detection, and bit judgment). The use of such ICs reduces parts, eliminates the need for complicated adjustment, and enables easy handling and cost reduction.

FEATURES

- All necessary detection capabilities, such as a synchronous signal separation circuit, are integrated into a single microchip. The use of the microchip can simplify application circuits, and eliminate the need for adjustment. (Only two inputs are provided: video signal input and fsc signal input.)
- Our original method is used for distinguishing EDTV2 identification signals from normal video signals. Therefore the accuracy of identification is improved.
- The detection level is adjustable.
- The microchip operates on a single supply voltage of 5V.
- Two types of packages are provided: DIP with a lead pitch of 2.54mm (M52393P); and SOP with a pitch of 1.27mm (M52393FP).

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N-A

APPLICATION

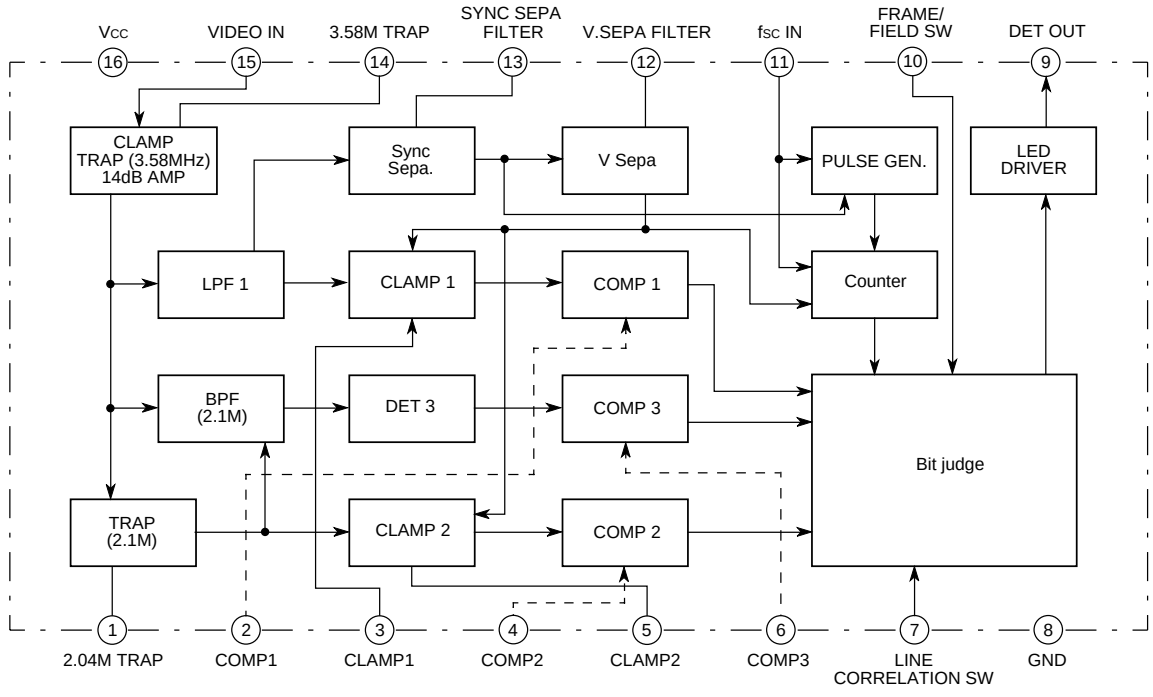
TV and videocassette recorder compatible with EDTV2.

RECOMMENDED OPERATING CONDITION

Supply voltage range.....4.7 to 5.3V

Rated supply voltage.....5V

BLOCK DIAGRAM



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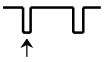
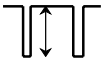
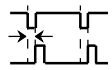
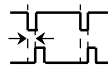
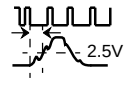
ABSOLUTE MAXIMUM RATINGS (Ta=25°C, Measured on a standard board, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6	V
P_d	Power dissipation	1400 (980)	mW
T_{opr}	Operating temperature	-20 to 75	°C
T_{stg}	Storage temperature	-40 to 125	°C
K_θ	Thermal derating (Ta≥25°C)	14 (9.8)	mW/°C

( ) indicate FP values.

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5.0V, unless otherwise noted)

SPECIFICATIONS

Symbol	Parameter	Test conditions					Limits			Unit
		Input	Input signal	Output	Output signal	Remarks	Min.	Typ.	Max.	
I_{CC1}	Circuit current1	SG15 SG11	0V F1	16	DC	Current	21	28	35	mA
V15	Clamp voltage	SG15 SG11	S1 F2	AC15		Sync chip voltage	2.2	2.5	2.8	V
G1	14dB Amp gain	SG15 SG11	S2 F1	AC1		G1=20log $\frac{M}{286mV}$	12	14	16	dB
TRP1	TRAP gain1	SG15 SG11	T1 F1	AC1		T1=20log $\frac{M}{143mV}$	10.3	13.3	16.3	dB
TRP2	TRAP gain2	SG15 SG11	T2 F1	AC1		T2=20log $\frac{M}{143mV}$	–	-12.0	-6.0	dB
TRP3	TRAP gain3	SG15 SG11	T3 F1	AC1		T3=20log $\frac{M}{143mV}$	–	-15.5	-9.5	dB
TRP4	TRAP gain4	SG15 SG11	T4 F1	AC1		T4=20log $\frac{M}{143mV}$	4.7	10.7	16.7	dB
SSD	Sync sepa. delay	SG15 SG11	S1 F1	12		Delay	0.7	1.0	1.3	µs
SSM	Sync sepa. delay at 30%	SG15 SG11	S3 F1	12		Delay SSM=SSD-M	0	–	0.5	µs
VSD	V sepa. delay	SG15 SG11	S1 F1	12		Delay	38	48	58	µs
VC1	CLAMP1 voltage	SG15 SG11	S1 F3	3	DC	Voltage	2.8	3.1	3.4	V
VC2	CLAMP2 voltage	SG15 SG11	S1 F3	5	DC	Voltage	2.8	3.1	3.4	V
LDI1	Driving capacity at Hi 1	SG15 SG11	S1 F1	9	DC	Voltage	4.0	4.2	4.5	V
LDI2	Driving capacity at Hi 2	SG15 SG11	S1 F1	9	DC	LDI2=LDI1-M	0	0.1	0.5	V
HDI1	Driving capacity at Lo 1	SG15 SG11	S1 F1	9	DC	Voltage	0	0.1	0.5	V
HDI2	Driving capacity at Lo 2	SG15 SG11	S1 F1	9	DC	HDI2=M-HDI1	0	0.2	0.5	V
V2	COMP. 1 voltage	SG11	F1	2	DC	Voltage	2.2	2.5	2.8	V
V4	COMP. 2 voltage	SG11	F1	4	DC	Voltage	2.2	2.5	2.8	V
V6	COMP. 3 voltage	SG11	F1	6	DC	Voltage	2.2	2.5	2.8	V

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TEST CONDITIONS

Symbol	Parameter	Supply voltage												Switch condition													
		1	2	3	4	5	6	7	9	10	11	14	16	1-1	1-2	3	5	7	9-1	9-2	10	11-1	11-2	12	14-1	14-2	14-3
I_{CC1}	Circuit current1							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
V15	Clamp voltage							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
G1	14dB Amp gain							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
TRP1	TRAP gain1							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
TRP2	TRAP gain2							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
TRP3	TRAP gain3							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
TRP4	TRAP gain4							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
SSD	Sync sepa. delay							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
SSM	Sync sepa. delay at 30%							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
VSD	V sepa. delay							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
VC1	CLAMP1 voltage							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
VC2	CLAMP2 voltage							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
LDI1	Driving capacity at Hi 1		0.4		0.4		0.4	2.5		2.5			5		ON	a	a	ON	ON	a	ON			a			ON
LDI2	Driving capacity at Hi 2		0.4		0.4		0.4	2.5		2.5			5		ON	a	a	ON	ON	b	ON			a			ON
HDI1	Driving capacity at Lo 1		0.4		0.4		0.4	0.5		2.5			5		ON	a	a	ON	ON	a	ON			a			ON
HDI2	Driving capacity at Lo 2		0.4		0.4		0.4	0.5		2.5			5		ON	a	a	ON	ON	c	ON			a			ON
V2	COMP. 1 voltage							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
V4	COMP. 2 voltage							G		G			5		ON	a	a	ON	ON	a	ON			a			ON
V6	COMP. 3 voltage							G		G			5		ON	a	a	ON	ON	a	ON			a			ON

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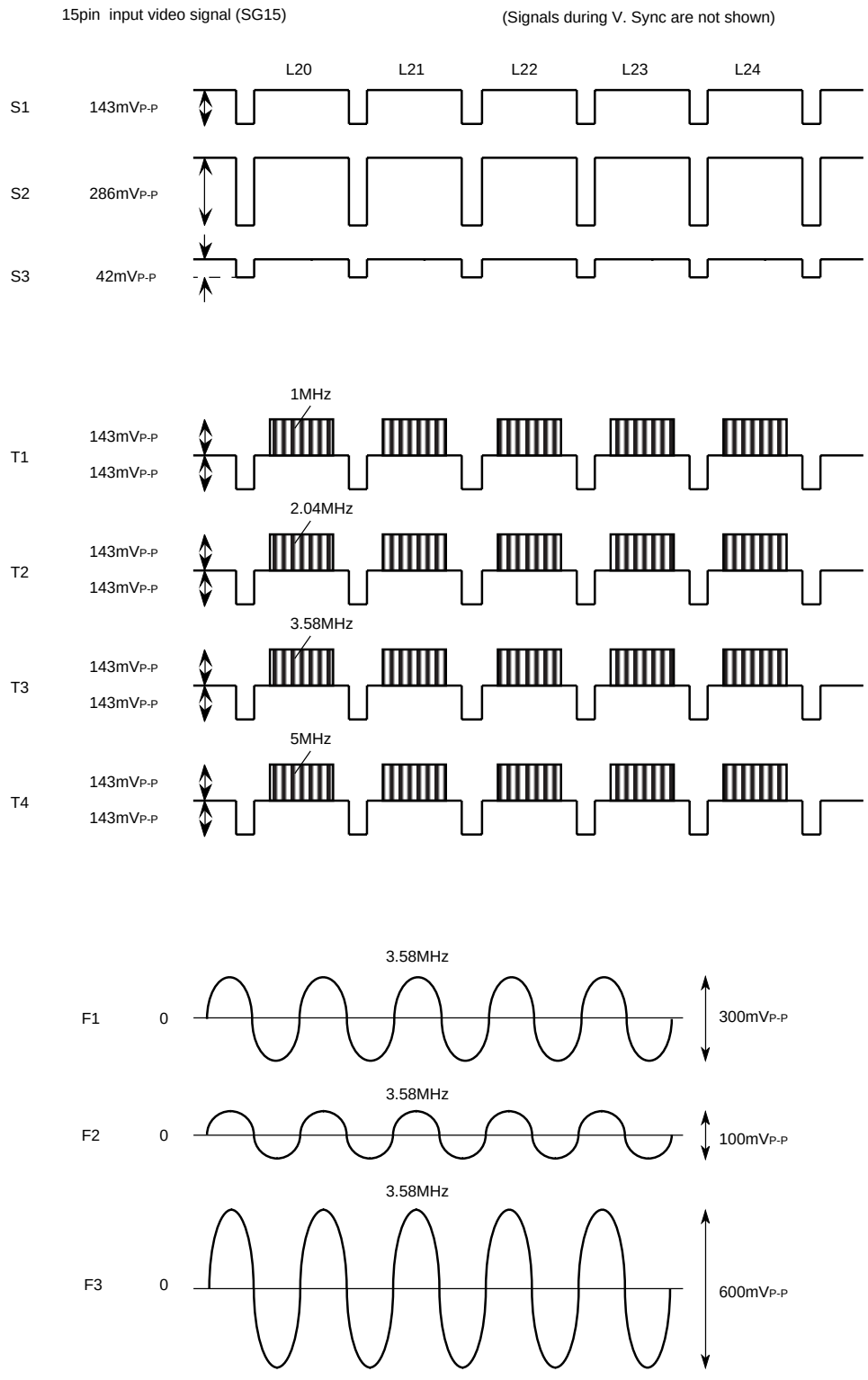
INPUT SIGNALS FOR TESTING



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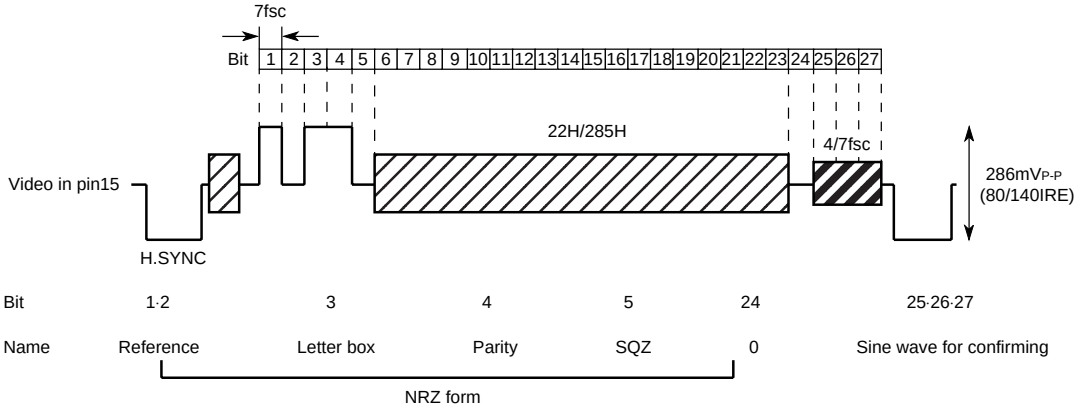
MODE TABLE

Mode		Conditions	Functions
COMP. 1 OFF		② 0 to 0.3V	Detector off at Bit 1 to 5, 24
COMP. 2 OFF		④ 0 to 0.3V	Detector off at Bit 25 to 27
COMP. 3 OFF		⑥ 0 to 0.3V	2.04MHz detector off at Bit 25 to 27
Line correlation SW (Shown in Fig.1)	ON	⑦ 0 to 0.5V	In a case an EDTV2 identification signal (or an equivarent one) is detected a couple of times during three lines of 21 to 23 (line 284 to 286), the output will be Lo (a standard signal).
	OFF	⑦ 2 to 3V (2.5V at open)	On the other hand, the output will be Hi (an EDTV2 signal) through the ID signal is detected a couple of times during the three lines.
Frame/Field SW (Shown in Fig.2)	Frame	⑩ 0 to 0.5V	The detection is performed once a field. The choice between Odd or Even is difficult. (effective data : 8 fields/ 8 frames)
	Field	⑩ 2 to 3V (2.5V at open)	The detection is performed in both fields. (effective data : 8 fields/4 frames)
TRICK MODE		⑭ 39μH 500Ω 47pF ON	The output state before the TRICK mode setting is kept regardless of an input signal.

FUNCATIONAL DESCRIPTION

Input signal



fsc in pin11 fsc, 0.3V_{P-P} ±6dB, Sine wave (ansynchronous signals are permitted)

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Output signal

DET OUT pin9

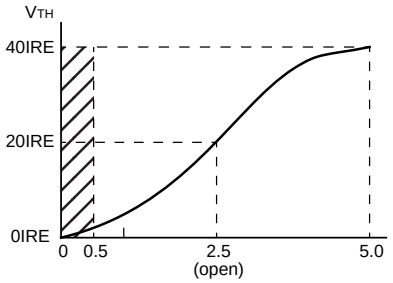
	Voltage	Condition	Current capacity
EDTV2	Hi (4.0 to 4.5V)	no load	MAX:5mA
Others	Lo (0.0 to 0.5V)	no load	

Detection block

This IC has 3 comparaters. Each comparaters detect in three parts the NRZ form, the sine wave for confirming (DC) and the sine wave for checking (AC).

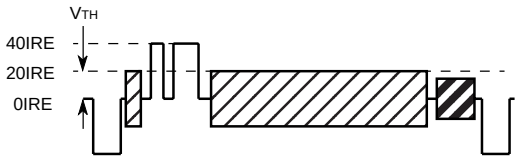
NRZ form (bit 1 to bit 5, bit 24) DC (COMP1)

COMP.1 V_{TH} CONTROL



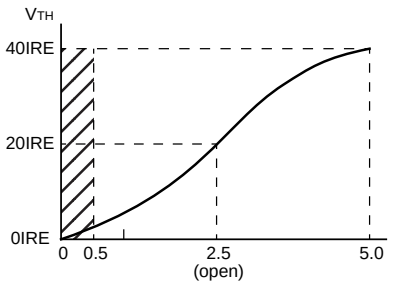
Pin2 COMP.1 CONT (V)

∗ COMP.1 OFF (at the pin 2 voltage of under 0.5V)



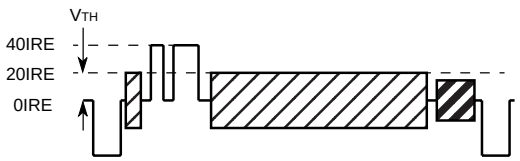
The sine wave for confirming (bit 25 to 27) DC (COMP.2)

COMP.2 V_{TH} CONTROL



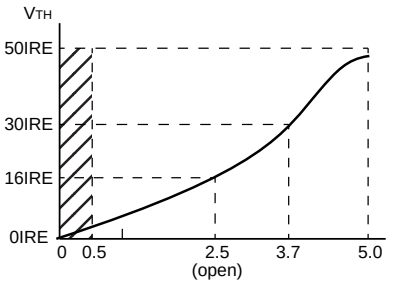
Pin4 COMP.2 CONT (V)

∗ COMP.2 OFF (at the pin 4 voltage of under 0.5V)



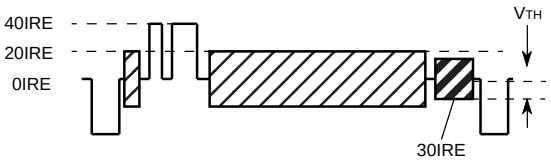
The sine wave for confirming (bit 25 to 27) AC (COMP.3)

COMP.3 V_{TH} CONTROL



Pin6 COMP.3 CONT (V)

∗ COMP.3 OFF (at the pin 6 voltage of under 0.5V)



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METHOD OF DETECTION

A line part (refer to Fig.1)

An EDTV2 ID is inserted into the line 22 (line 285), therefore the IC detects during 3lines (including before and after 2 lines of the line 22). A field contains the ID signal in its appropriate lines, whitch results in an EDTV2 signal.

In a case the ID signal is detected a couple of times during three lines, a signal is regarded as a standard signal not an EDTV2 considering the correlation between 2 or 3 lines (pin 7 is grounded). On the other hand, the line correlation is off by opening the pin 7. In this case, the signal is regerded as an EDTV2 even though the ID signal is detected a couple of times during the three lines.

A field part (refer to Fig.2)

In a case the ID signal is detected in 8 consecutive fields, a signal is regarded as an EDTV2 one and the pin 9 outputs high. However it can not be detected consecutivelly, a signal is not an EDTV2 one and the pin 9 is low. Detecting timing is varied in following 2 modes.

A field mode

The pin 10 is opened (2.5V). The detection is performed once a field. It takes more than 133ms (4 frames) for the distinction.

A frame mode

The pin 10 is grounded (0V). The detection is performed once a frame; once a Odd field or once a Even field. It takes more than 267ms (8 frames) for the distinction.

Note: The alternatvie of Odd or Even field is difficult because of no field distinction.

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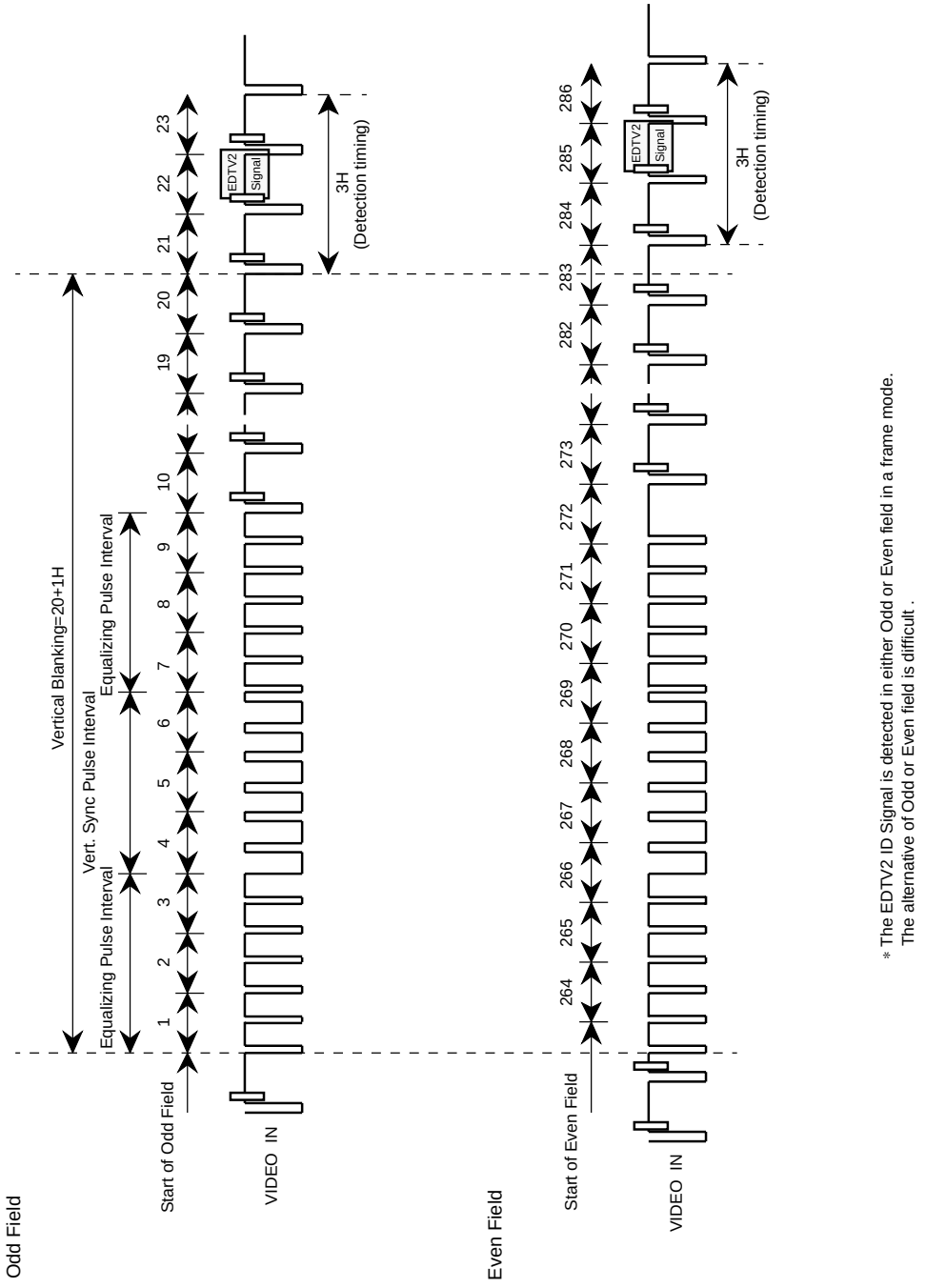

Fig. 1 Edtv2 signal detection (field mode)

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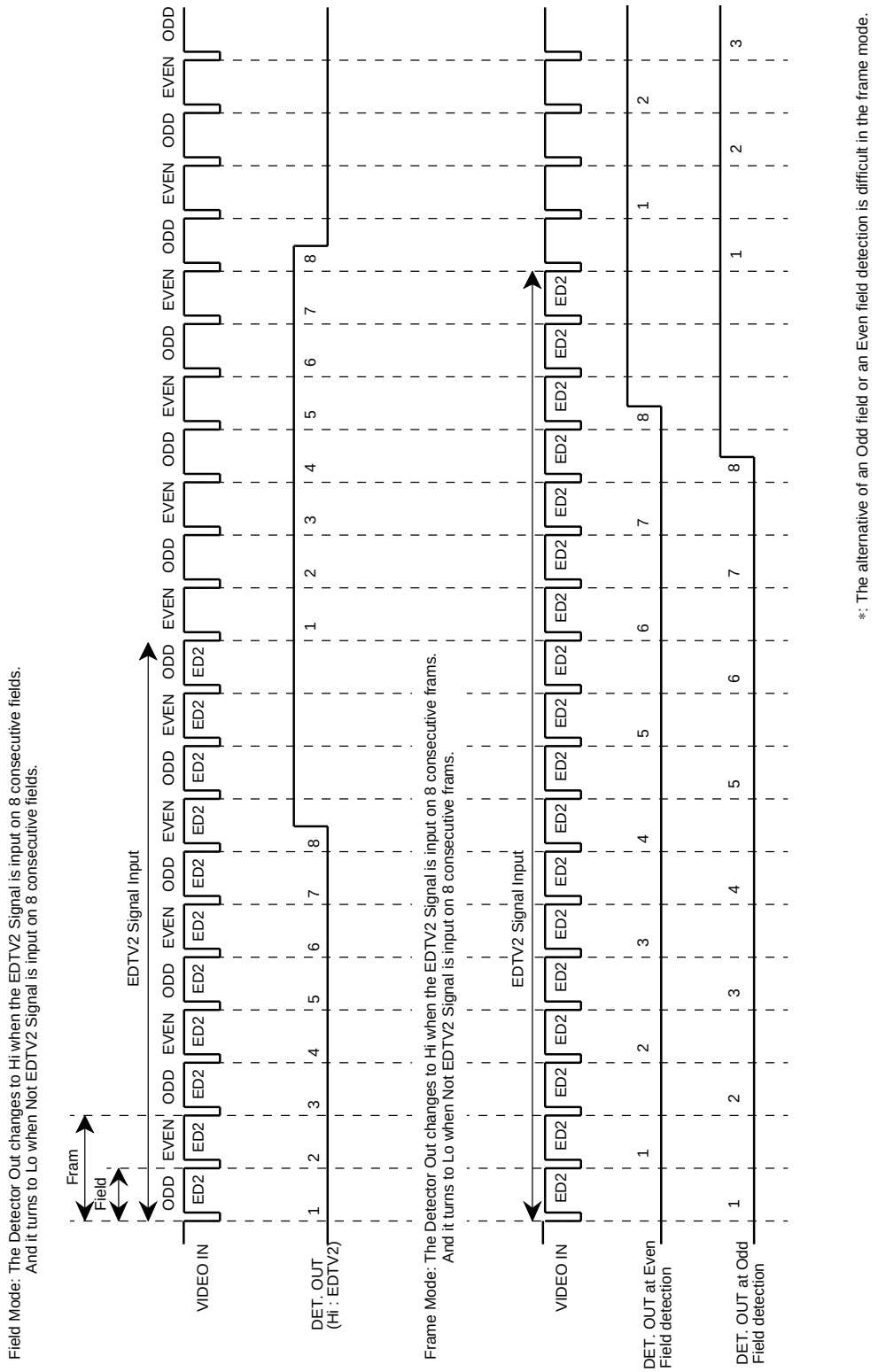

Fig. 2 Difference of detection between frame mode and field mode

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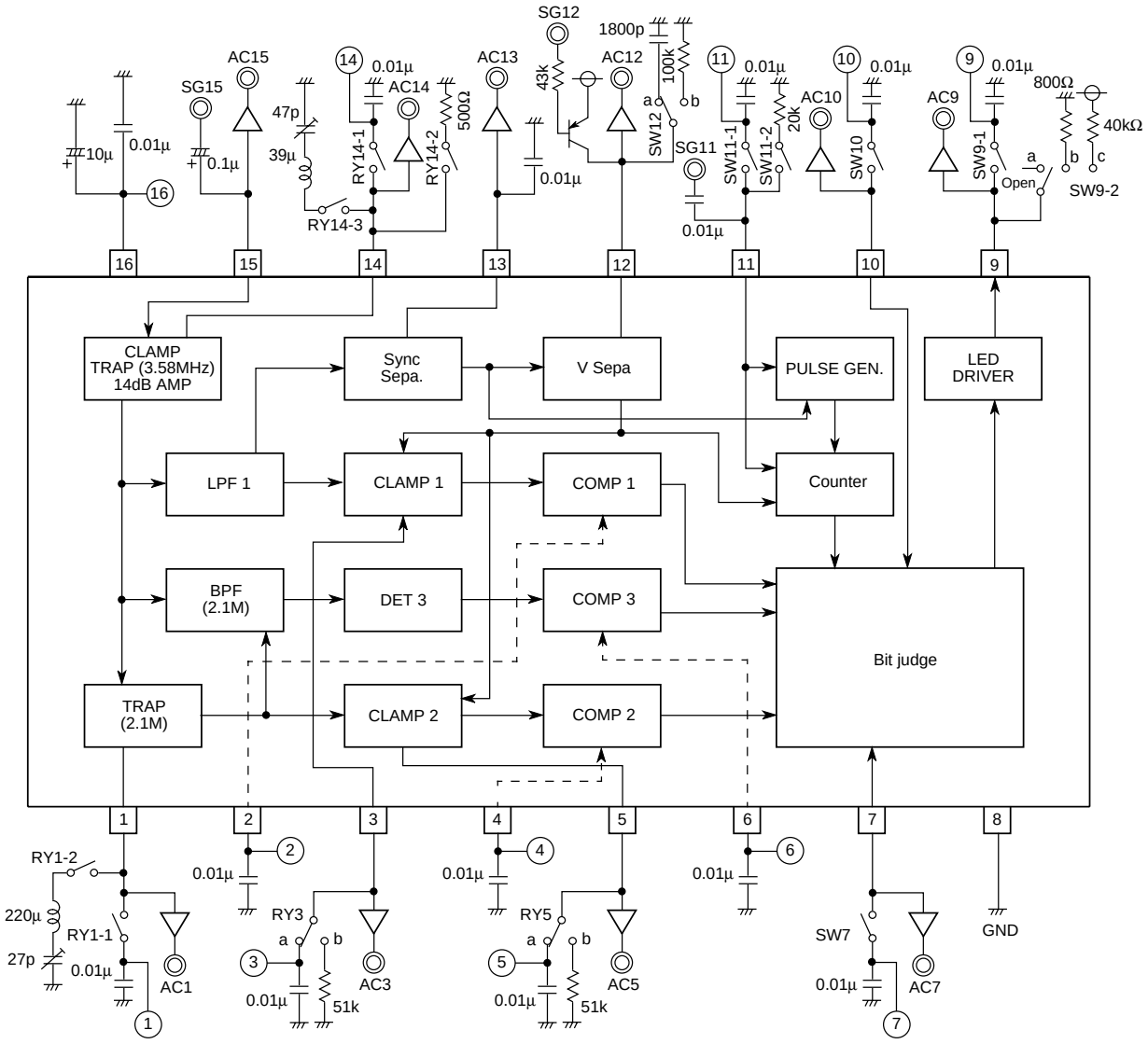
TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

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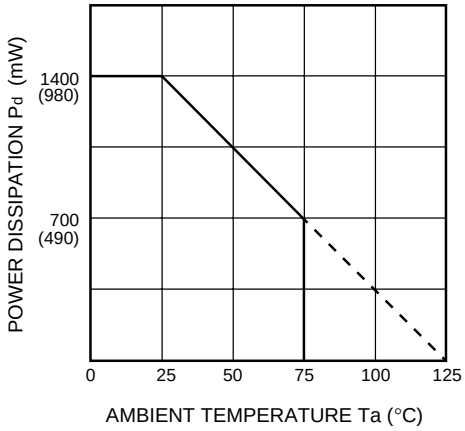
TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

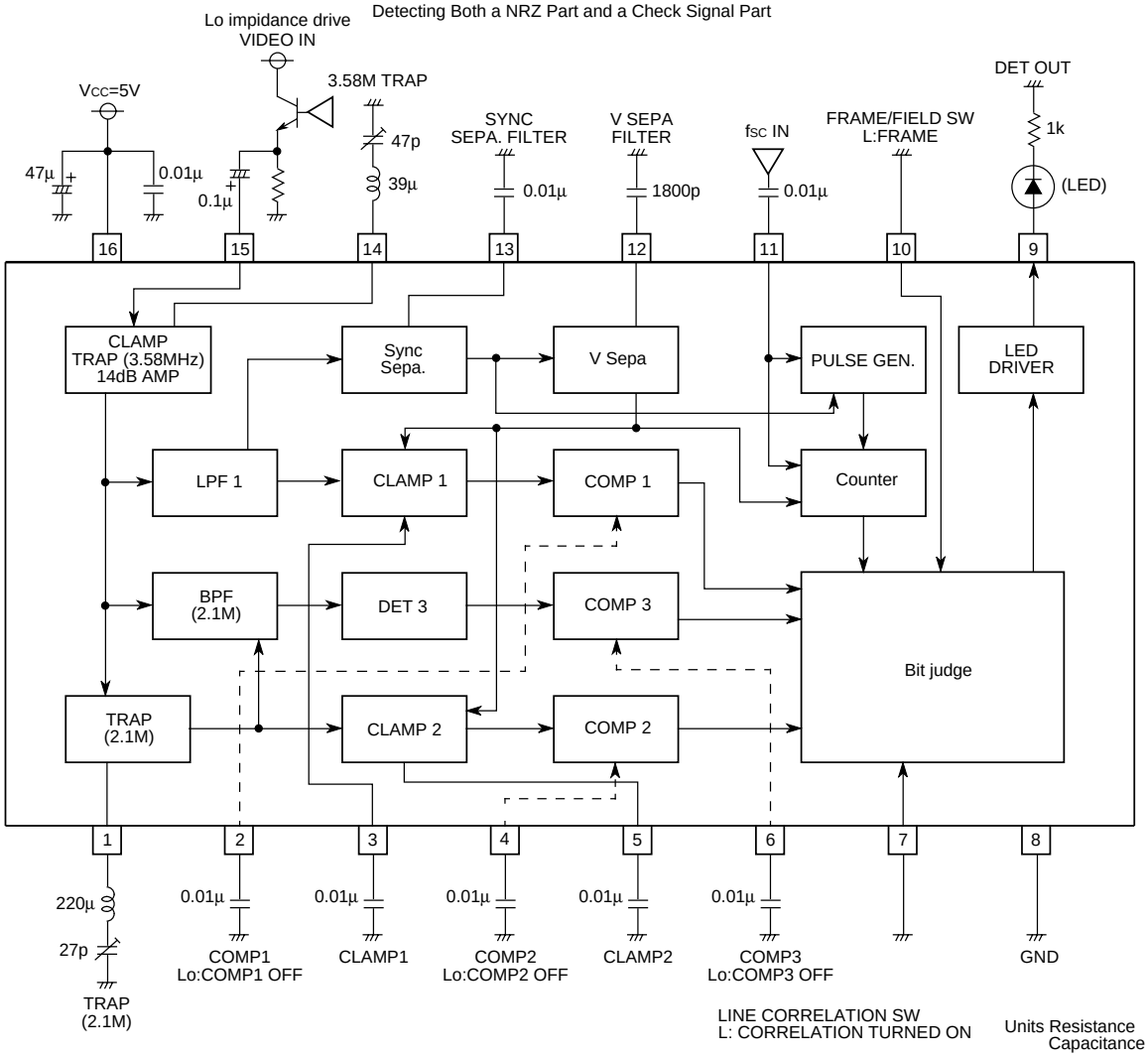


Thermal Derating Characteristic of the IC with mounting on the standard boad.
Values inside of round brackets correspond to FP.

Standard board
Material.....Glass epoxy (Cu film pattern on one side)
Size.....70mm□, 1.6mm thickness
Cu film thickness.....18µm

APPLICATION EXAMPLE 1

Detecting Both a NRZ Part and a Check Signal Part



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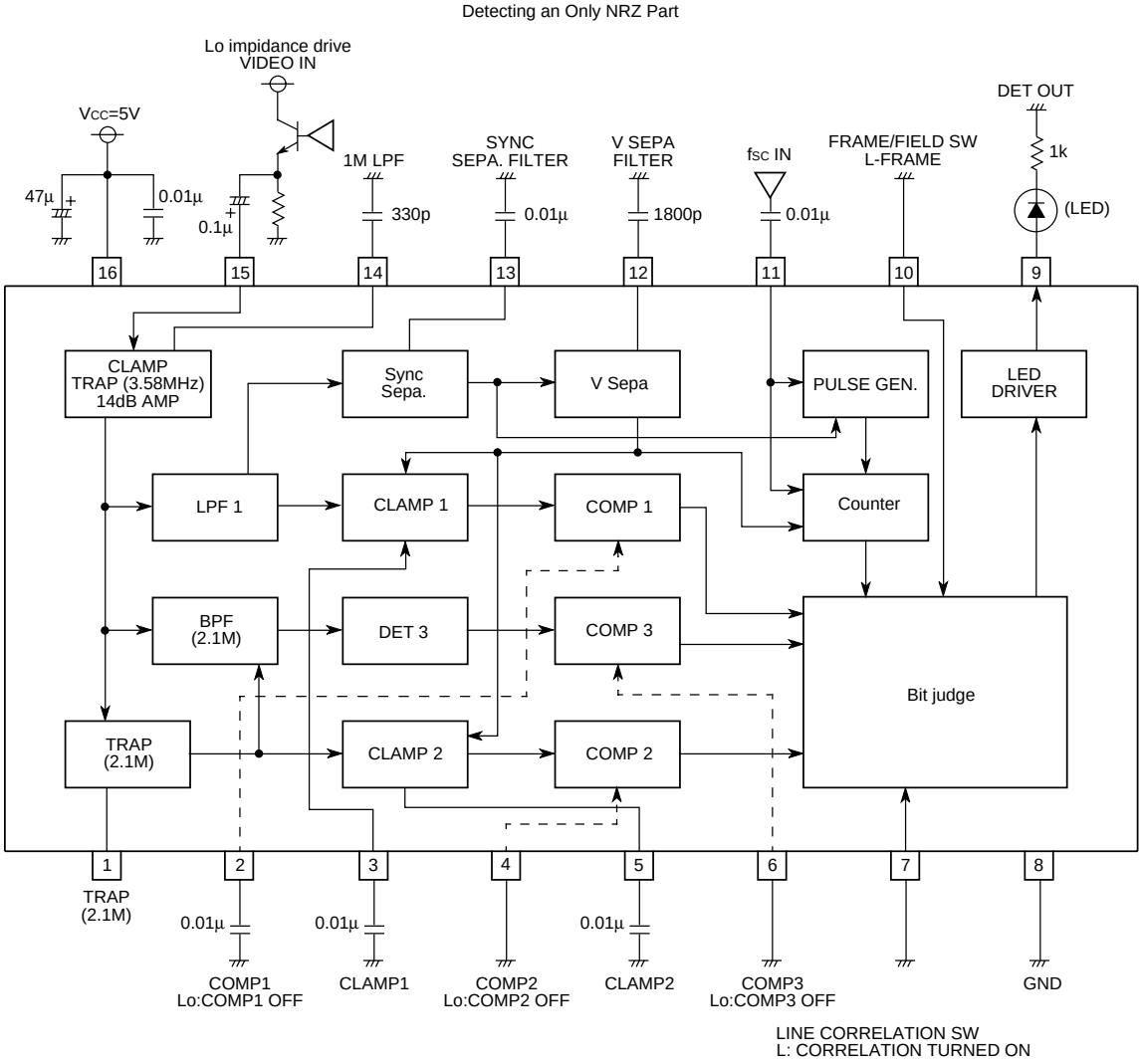
APPLICATION EXAMPLE 2



Units Resistance : Ω
Capacitance : F

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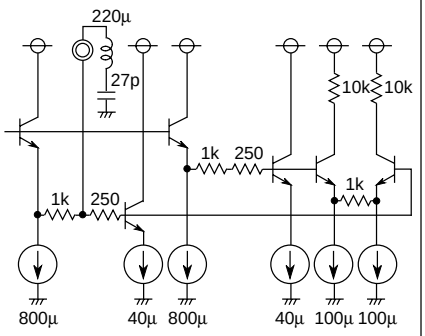
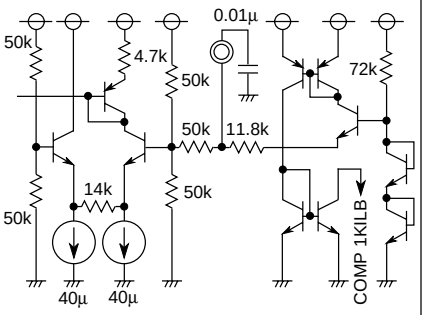
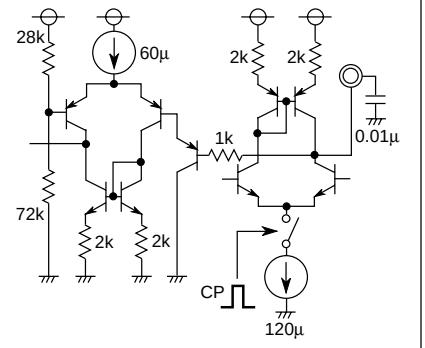
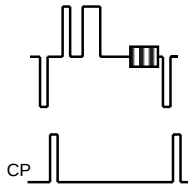
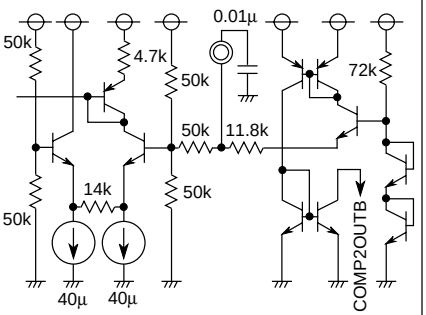
DESCRIPTION OF PIN

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Description of function
1	TRAP (2.1M)	3.2V 2.5V 1.8V		
2	COMP1 CONT.	2.5V		at 2.5V
3	CLAMP1	3.0V		
4	COMP2 CONT.	2.5V		at 2.5V

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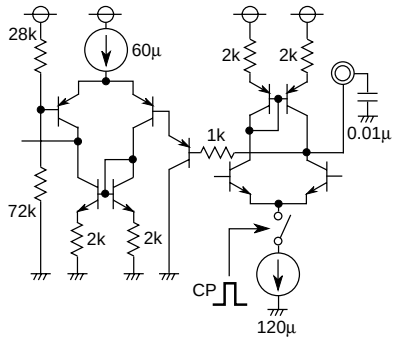
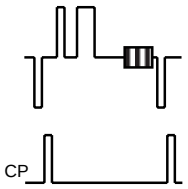
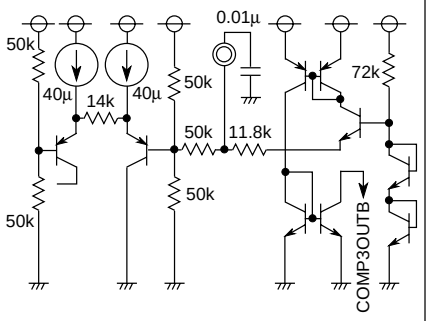
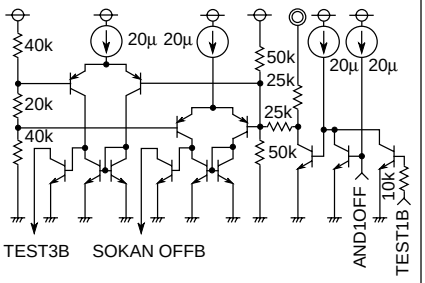
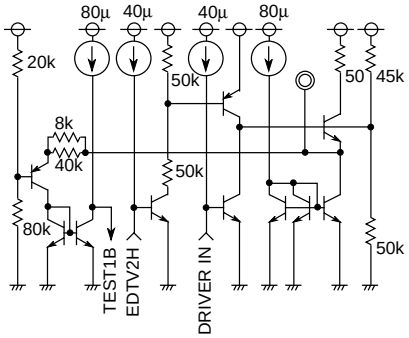
DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Description of function
5	CLAMP2	3.0V		
6	COMP3 CONT.	2.5V		at 2.5V
7	Line correlation SW	2.5V		H:TEST3 M:Correlation Detector OFF L:Correlation Detector ON
8	GND			
9	DET out	H:4.2V L:0.1V		pin9 5V:TEST1

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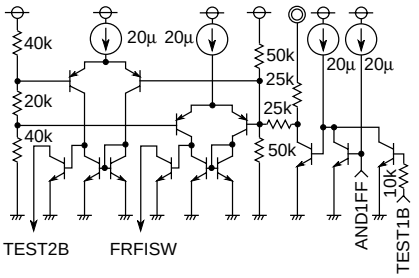
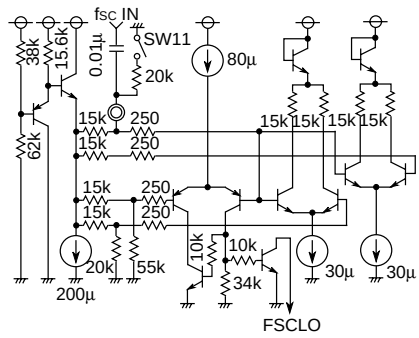
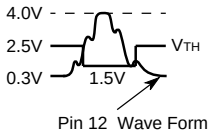
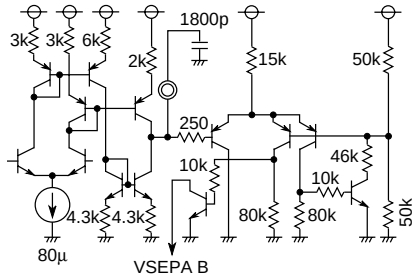
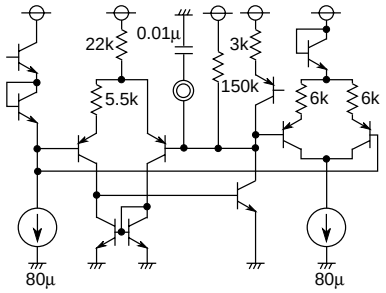
DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Description of function
10	Frame/ Field SW	2.5V		H:TEST2 M:8 Field Detector L:8 Frame Detector
11	fsc IN	3.0V Input 3.58MHz 0.3V$_{P-P}$		SW11:ON FSC Mode
12	V SEPA filter	 Pin 12 Wave Form		
13	Sync Sepa. filter	Sync Pin 13 Wave Form (3V)		

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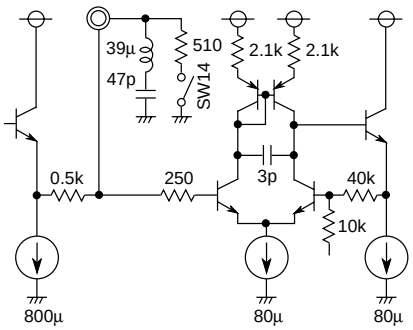
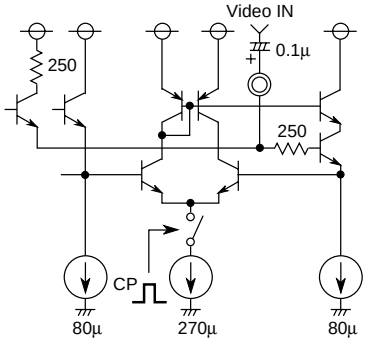
DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Description of function
14	3.58 TRAP	AC 2.2V 2.05V 1.9V		SW14:ON TRICK Mode
15	Video IN	Clamp In 2.65V CP		
16	Vcc	5V		

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