Thermal considerations for advanced logic families (Futurebus+, ABT and MULTIBYTE)

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INTRODUCTION

Thermal characteristics of integrated circuit packages have been and increasingly will be a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can adversely effect the long term operating life of an IC. The advantages realized by miniaturization often have trade–offs in terms of increased junction temperatures. Some of the variables affecting T_J are controlled by the IC manufacturer and others are controlled by the system designer. Depending on the environment in which the IC is placed, the user could control well over 75% of the current that flows through the device.

With the ever increasing use of Surface Mount Device (SMD) technology, management of thermal characteristics becomes a growing concern because not only are the SMD packages much smaller, but the thermal energy is concentrated more densely on the printed wiring board. For these reasons, designers and manufacturers of surface mount assemblies must be aware of all the variables affecting T_J.

POWER DISSIPATION

Power dissipation for the ABT (Advanced BiCMOS Technology), MULTIBYTE and Futurebus+ devices can be estimated using the same equation with the exception of Futurebus+ transceivers. Due to BTL OPEN–COLLECTOR outputs, BTL output swings and the large current driven on the BTL side (B side) of the transceivers the equation must be altered.

There are five major factors controlled by the user which contribute to increased BiCMOS power dissipation.

1. Frequency of operation (output switching frequency)
2. Input voltage levels
3. Output loading (capacitive and resistive)
4. V_{CC} level
5. Duty cycle

Each of these five factors are addressed in the estimating equation except duty cycle. Duty cycle can be addressed by “weighting” terms 2, 5, 6, 7 and 8 appropriately.

Conditions under which measurements were taken and upon which the Power Dissipation Equation is based are:

1 2 3 4

$$P_D = V_{CC}\left[C_P V_{CC}\sum_{i=1}^{s} F_{OUT_i}\right] + V_{CC}\left[\frac{I_{CCL} + I_{CCH}}{2n}s + \frac{I_{CCL}}{n}L + \Delta I_{CC} n_3\right]$$

5 6

$$+ (V_{CC} - V_{OH})\left[(V_{OH} - V_{OL})\sum_{i=1}^{s} C_{L_i} F_{OUT_i} K_{P_i} + \sum_{i=1}^{h}\frac{V_{OH}}{R_{D_i}}\right]$$

7 8

$$+ (V_{OL})\left[(V_{OH} - V_{OL})\sum_{i=1}^{s} C_{L_i} F_{OUT_i} + \sum_{i=1}^{l}\frac{(V_{CC} - V_{OL})}{R_{U_i}}\right]$$

Power Dissipation Equation

V_{CC} = 5V; 25°C; F_{OUT} = 1, 10, 20, 30, 40, and 50MHz; 50% duty cycle; C_L = 0, 15, 50, 100, and 200pF; also 1, 2, 4, and 8 outputs switching.

The first current term is due to I_{CC} with the device unloaded. It is caused by the internal switching of the device.

$$C_P V_{CC}\sum_{i=1}^{s} F_{OUT_i}$$

This term represents the I_{CC} current with absolutely no load. This measurement was taken without the output pins connected to the board. The C_P for a device is calculated by:

$$C_P = \frac{I_{CC}(@50MHz) - I_{CC}(@1MHz)}{V_{CC}(49MHz)s}$$

“s” is the number of outputs switching. C_P will be different for each product type.

The second term is current due to I_{CC} with the outputs unloaded. This I_{CC} is caused by switching the bipolar outputs.

$$(I_{CCL} + I_{CCH})\frac{s}{2n}$$

The I_{CCL} and I_{CCH} are the typical values found in the corresponding product data sheets. In the case of a 50% duty cycle an average of I_{CCL} and I_{CCH} will flow through the device. “n” is the number of outputs on the device.

The third term is I_{CCL} due to the outputs being held Low. The I_{CCH} current is in the µA range so if an output is held or forced High then there is no appreciable I_{CC} increase.

$$I_{CCL}\frac{L}{n}$$

“L” is the number of outputs held Low.

The fourth term is through current due to holding the CMOS inputs at 3.4V rather than at the rail voltages. This term becomes insignificant as load and frequency increase.

$$\Delta I_{CC} n_3$$

ΔI_{CC} is the through current when holding the input High of a device to 3.4V. This value is typically 300µA to 500µA. “n3” is the number of inputs at 3.4V.

The fifth term is current through the upper structure of the device. It is caused by the external capacitive load and the output

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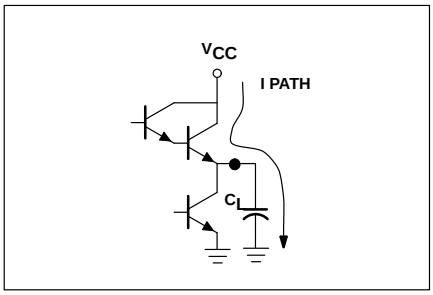
frequency. If a capacitive load exists then this term can become very significant.

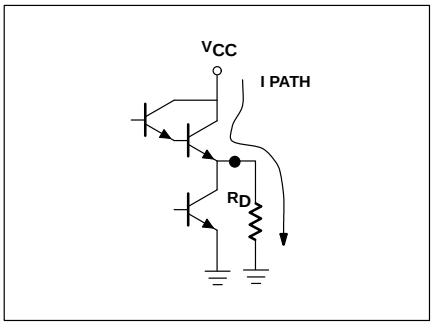


$$(V_{OH} - V_{OL}) \sum_{i=1}^{S} C_{L_i} F_{OUT_i} K_{P_i}$$

V_{OH}–V_{OL} is the voltage swing of the output. C_L is the output load (this can vary from output to output). F_{OUT} is the output frequency which can also vary from output to output.

K_P is a factor which best estimates the feedthrough current and variances in the "V_{OH}–V_{OL}" factor as C_L changes. K_P = f(C_L) = –2.5E– $5C_L^2$+4.3E–$3C_L$+1.4 (C_L is expressed in unitless terms, e.g. "15" for 15pF…).

The sixth term is current through the upper structure due to an external resistive load to ground. This term includes both switching outputs and static High outputs.



As the output frequency increases the measured current approaches that of static High outputs.

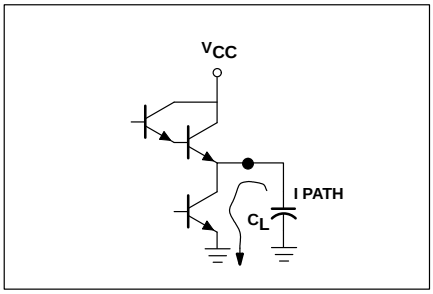
$$\sum_{i=1}^{h} \frac{V_{OH}}{R_{D_i}}$$

R_D is an external pull–down resistor. A different value load could be applied to each output.

The seventh current term is determined by the output capacitive load and the output frequency on the lower structure of the device.

If this load exists then this term is also significant.

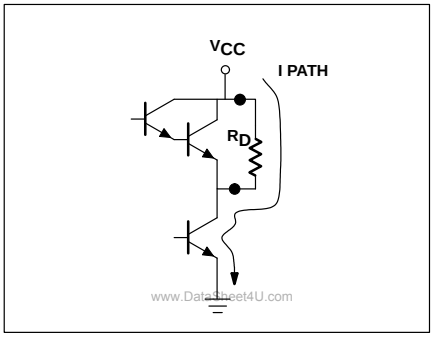
All variables are the same as with the fifth term with the exception that this is current flowing through the lower structure of the IC.



$$(V_{OH} - V_{OL}) \sum_{i=1}^{S} C_{L_i} F_{OUT_i}$$

This current is not I_{CC}, but rather current that is "sinked" from an external source.

The eighth and final term is due to an external load connected to V_{CC}.



This term includes both switching and static Low outputs.

$$\sum_{i=1}^{l} \frac{(V_{CC} - V_{OL})}{R_{U_i}}$$

As with term seven, this is current that flows through the lower structure of the IC. This current too is not I_{CC}.

Futurebus+ transceivers' power dissipation can be estimated in the same way as ABT devices, excepting terms 3, 5, 6 and 8 in the equation. An I_{CCH} term needs to be added to term 3. Term 3 would then read "I_{CCL}L/n+ I_{CCH}H/n". "H" is the number of outputs held static High. Since BTL outputs are open–collector, terms 5 and 6 do not apply and are discarded. Term 8 needs to be adjusted—replace "(V_{CC}–V_{OL})" with "(2.1V–V_{OL})". (If the level of the pull–up voltage is not 2.1V then the actual pull–up voltage would be substituted).

ABT C_P VALUES

Many of the ABT products have been characterized for their C_P values. The following table shows the products that have been tested along with their corresponding C_P numbers. Over time C_P for all ABT and MULTIBYTE products will be characterized. Refer to the individual product data sheets for their values if the values are not noted below.

74ABT125	6.0pF
74ABT126	6.5pF
74ABT240	7.0pF
74ABT240–1	7.0pF
74ABT244	4.5pF
74ABT244–1	5.5pF
74ABT540	7.0pF
74ABT543	11.0pF
74ABT544	11.0pF
74ABT620	9.0pF
74ABT640	8.5pF
74ABT646	11.0pF
74ABT648	11.5pF
74ABT651	11.5pF
74ABT652	11.5pF
74ABT657	9.0pF
74ABT821	16.0pF
74ABT823	17.0pF
74ABT827	6.0pF
74ABT833	7.5pF
74ABT841	9.0pF
74ABT843	9.5pF
74ABT861	7.0pF
74ABT863	7.5pF
74ABT899	11.0pF
74ABT2952	16.0pF
74ABT2953	16.0pF

THERMAL RESISTANCE

The ability of a package to conduct heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta JA (θ_{JA}). θ_{JA} is often separated into two components: thermal resistance from the junction to case, and the thermal resistance from the case to ambient. θ_{JA} represents the total resistance to heat flow from the chip to ambient and is expressed as follows:

$$\theta_{JC} + \theta_{CA} = \theta_{JA}$$

Detailed θ_{JA} and θ_{JC} graphs will be included in a later section of this note. For the ease of the user a table with θ_{JA} and θ_{JC} values for average die sizes is included here.

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θ_{JA} AND θ_{JC} CALCULATIONS FOR ABT, MULTIBYTE, AND FUTUREBUS+

θ_{JA}

	DIP		SO pkg		PLCC/PQFP	
# pins	Still air	300 lfpm	Still air	300 lfpm	Still air	300 lfpm
14	82	63	117	98	–	–
16	82	63	110	92	–	–
20	74	57	91	74	–	–
24	65	50	77	63	–	–
28	61	47	71	58	69	50
52	–	–	–	–	79	57
68	–	–	–	–	48	35
84	–	–	–	–	39	28
100	–	–	–	–	61	43

Preliminary θ_{JA} (new packages)

	SSOP		SQFP
# pins	Still air	200 lfpm	Still air
*20	143	119	–
*24	135	110	–
*100	–	–	68

θ_{JC}

# pins	DIP pkg	SO pkg	PLCC/PQFP
14	38	36	–
16	38	35	–
20	32	29	–
24	36	26	–
28	31	26	34
52	–	–	23
68	–	–	18
84	–	–	14
100	–	–	15

NOTES:

* Preliminary data only

- (for ABT use 1.8mm × 1.8mm (70mil × 70mil) average die size)
- (for MULTIBYTE and Futurebus+ transceivers use 3.0mm × 3.5mm (118mil × 138mil) average die size)
- (for 68/84–pin Futurebus+ use 3.8mm × 3.7mm (149mil × 146mil) average die size)
- (for 100–pin Futurebus+ use 6.0mm x 6.0mm (235mil × 235mil) average die size)

JUNCTION TEMPERATURE (T_J)

Junction temperature (T_J) is the temperature of a powered IC at the substrate diode. Signetics uses a technique known as the temperature sensitive parameter (TSP) method to measure the junction temperature of an IC. This method uses the linear relationship between forward voltage and temperature (at a constant forward current) of a diode to measure junction temperature. The change in junction temperature can be measured for a known power dissipation which then allows for the thermal resistance to be calculated using the expression shown for θ_{JA}:

$$_{JA} = \frac{\Delta T_J}{P_D} = \frac{(T_J - T_{amb})}{P_D}$$

where T_{amb} is the temperature of the ambient. For detailed information on the measurement techniques and the tools used, please refer to Signetics' Reliability Management Group Publication "IC Package Thermal Resistance Characteristics".

Once the value of θ_{JA} has been found then T_J can be calculated for varying P_Ds.

$$T_J = P_D \times \theta_{JA} + T_{amb}$$

For Signetics' Futurebus+, ABT, and MULTIBYTE the following criterion is used to warn customers about excessive T_J.

If the junction temperature (T_J) could exceed 125°C but not 150°C then a warning to the customer recommending thermal mounting must appear on the data sheet.

If the T_J could exceed 150°C but not 175°C then it is necessary to warn the customer and advise specific methods (to be found in the product data sheet) to reduce the T_J to 125°C. T_J may be reduced either by thermal mounting techniques or by the use of forced air.

If T_J could exceed 175°C then the product release will not occur and a redesign will be initiated or limit changes will be made in order to lower the T_J below the 175°C limit.

With the advent of multiple–byte products (MULTIBYTE) it may become possible to switch forty outputs simultaneously. When this occurs the system designer must be aware of the risks/dangers of rising T_J values. Eventually compromises must be made in order to keep T_J below damaging values.

FACTORS AFFECTING θ_{JA}

There are several factors which affect the thermal resistance of an IC package. Effective thermal management demands a sound understanding of these factors. Major package variables include the *leadframe design* and the *plastic* used to encapsulate the device. Other variables such as the *die size* and *die attach methods* also affect thermal resistance. Other factors that have a significant impact on the θ_{JA} include the *substrate* upon which the IC is mounted, the *layout density*, the *air–gap* between the package and the substrate, the number and length of *traces* on the board, *thermally conductive epoxies*, and *external cooling*.

PACKAGE CONSIDERATIONS

Following is a brief discussion on various package factors and their effect on thermal resistance. These items are inherent to the package design, and therefore are fixed by Signetics.

Die size has a large effect on thermal resistance. Smaller die sizes result in higher thermal resistances, given that other package parameters remain constant. This effect is reflected in the graphical data presented in this note. Die size is a function of device type and complexity.

Die attach methods used by Signetics have little effect on thermal resistance due to the thinness (typically less than 1 mil), the good thermal conductivity and the low power dissipation of the ICs (typically less than 2 watts). Die attach methods and material can have large effects on device reliability and die stress. These items along with high thermal conductivity control limit the selection of materials and processes. The copper leadframes of plastic packages require a compliant die attach. To meet this requirement, Signetics uses high thermal conductivity adhesives.

Leadframe material is one of the more important factors. The higher the conductivity, the lower the thermal resistance because of the heat spreading effect of the leadframe. For this reason all current Signetics plastic packages use high thermal conductivity copper alloy leadframes.

Leadframe design is important especially for plastic packages; large pad and pad support structures improve thermal resistance. Leadframe design is mainly controlled by die size and pad position layout, however, thermal dissipation is maximized whenever possible.

Bond wires, because of their small size, (1.0 to 1.3 mil diameter) do not provide a significant thermal path in Signetics' packages and thus have little effect on thermal resistance.

Package body material could have a large effect on thermal resistance, but package requirements such as reliability, manufacturing, etc. control the selection of these materials. Until new materials are developed there is no real opportunity for decreasing thermal resistance by increasing package body thermal conductivity while maintaining our high reliability standards.

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THERMAL RESISTANCE MEASUREMENTS

Thermal resistance values are presented as a function of die size for each package. All data was derived from tests carried out on devices run at a constant power dissipation (actual dissipation is given with each graph). Whether power dissipation is higher or lower, it will only slightly affect thermal resistance. The general trend is for decreasing thermal resistance with increasing power. This is common to all packages.

Thermal resistance can be affected by slight variation in internal leadframe design. For example a larger die pad gives slightly lower thermal resistance for the same size die. The data presented represents the typical Signetics leadframe/die combinations with large die on large pads and small die on small pads. There are many transition areas where a die could be placed differently depending on pad layout, aspect ratio, etc. The effect of leadframe design is within the ±15% accuracy of these graphs. Data is available with improved accuracy (±7.5%). For exact die/leadframe/power dissipation combinations, contact Philips Components–Signetics, Reliability Management Group Publications, MS 35, 811 E. Arques Avenue, Sunnyvale, CA 94088–3409 or call (408) 991–2000.

Data is also available in the form of a computer program (SIGTHERM) which runs on IBM or compatible PCs in BASIC. SIGTHERM provides estimates for θ_{JA} and θ_{JC} using exact die/leadframe/power dissipation combinations resulting in more accurate (±7.5%) data than in the graphs in this note. SIGTHERM also gives θ_{JA} estimates at different air flow rates between 100–800 LFPM. The program requires the user to input package type, die size, power dissipation and leadframe code. Contact Philips Components–Signetics Reliability Management Group Publications, MS 35, for more information on SIGTHERM.

EXAMPLES OF THERMAL CALCULATIONS

Junction temperature can be estimated using the following equation:

$$T_J = (\theta_{JA} \times P_D) + T_{amb}$$

Where:

T_J = Junction Temperature (°C)

θ_{JA} = Thermal Resistance Junction–to–Ambient

P_D = Power Dissipation at a T_J

T_{amb} = Temperature of Ambient (°C)

EXAMPLE OF ABT T_J CALCULATION

1. Calculate Current Consumption:

For example the ABT244's C_P is 4.5pF. Let V_{CC} = 5V; operating temperature = 25°C; F_{OUT} = 50MHz for 4 outputs switching; hold 2 inputs Low and 2 inputs High (at 3.4V); C_L = 100pF; 500Ω pull–down; no pull–up.

$$\underset{1}{\left[4.5\text{pF} \quad 5\text{V}\sum_{i=1}^{4} 50\text{MHz}\right]} = 4.5\text{mA}$$

$$+$$

$$\underset{2}{\left[\frac{24\text{mA} + 0.5\text{mA}}{2(8)}4\right]} + \underset{3}{\left[\frac{24\text{mA}}{8}2\right]} + \underset{4}{\left[.5\text{mA}(2)\right]}$$

$$= 6.125\text{mA} + 6\text{mA} + 1\text{mA} = 13.125\text{mA}$$

These unloaded terms contribute only 9% of the total I_{CC} current.

$$+$$

$$\underset{5}{(4\text{V} - 0.2\text{V})\sum_{i=1}^{4} 100\text{pF}50\text{MHz}1.58} + \underset{6}{\sum_{i=1}^{6}\frac{4\text{V}}{500}}$$

where: K_P = –2.5E–5(100^2) + 4.3E–3(100) + 1.4 = 1.58

In this example terms five and six contribute over 90% of the total I_{CC} current . This part of I_{CC} is entirely due to external loading.

$$\underset{7}{(4\text{V} - 0.2\text{V})\sum_{i=1}^{4} 100\text{pF}50\text{MHz}} + \underset{8}{\sum_{i=1}^{6}(5\text{V} - 02\text{V})}$$

$$= 76\text{mA} + 0 = 76\text{mA}$$

These terms are not I_{CC} currents, but rather currents "sinked" by the lower structure of the device.

Term	Predicted	Measured
1 & 2	10.63mA	10.2mA
3	6mA	6mA
4	1mA	1.5mA
5	120.1mA	117.8mA
6	48mA	53mA
7	76mA	—
8	0mA	—
Total 1–6	**185.7mA**	**188.4mA**

For this example the equation estimate is within 1% of the actual I_{CC} current!! This is not a claim of 1% accuracy, but the equation is quite accurate. (Terms 7 and 8 are not included in the comparison.)

2. Finding P_D (V × I)

When calculating the total power dissipation of the device, the first four terms are multiplied by V_{CC}, which in this example is 5V.

5V(17.625mA) = 88.1mW

The fifth and sixth terms are multiplied by the voltage drop across the upper structure of the device, V_{CC}–V_{OH}. This is approximately 1V.

1V(168.1mA) = 168.1mW

The seventh and eighth terms are multiplied by the voltage drop across the lower structure of the device, V_{OL}.

0.2V(76mA) = 15.2mW

The total estimated power dissipation of an ABT244 with 4 outputs switching, at 25°C, with V_{CC} = 5V, with 2 outputs held static Low, and 2 inputs at 3.4V, with 100pF capacitive loads, 500Ω pull–downs, and 50MHz switching frequency is:

271.4mW

3. Determine θ_{JA}

The θ_{JA} for a 20–pin SOL package using the average die size for ABT is 91°C/W @ 0.7W.

4. Determine θ_{JA} @ 271mW P_D

Using the AVERAGE EFFECT of POWER DISSIPATION on θ_{JA} graph calculate the percentage change in power = (.271W – .7W)/.7W = –.61 (–61% change) then check the graph and see that θ_{JA} increases by 8.5%. So θ_{JA} increases to 91 + 91 × .085 = 98.7°C/W.

5. Assume 200 LFPM Air Flow

Calculate the effects of air flow by referring to the graph AVERAGE EFFECT of AIR FLOW on θ_{JA}. The θ_{JA} is decreased by 14% leaving a θ_{JA} of 98.7 – (.14 × 98.7) = 84.9°C/W.

6. Final Calculations for T_J for the ABT244

$T_J = (P_D \times \theta_{JA}) + T_{amb}$ = (.271W × 84.9°C/W) + 70°C = 93°C. Referring to the warnings in the JUNCTION TEMPERATURE section, a 93°C T_J would constitute absolutely no junction temperature worries.

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EXAMPLE OF FUTUREBUS+ TRANSCEIVER T_J FOR BTL SIDE ("A" side can be treated like ABT)

1. Calculate Current Consumption

For example let the FB2031's C_P be 16pF. Let V_{CC} = 5V; operating temperature = 25°C; F_{OUT} = 50MHz for 5 outputs switching; hold 2 inputs Low and 2 inputs High (at 3.4V); C_L = 100pF; no pull–down; 16.5Ω pull–up.

1

16pF(5V(5)50MHz) = 20mA

+

2

(17mA + 17mA)/2(9) × 5 = 9.44mA

+

3

17mA/9 × 2 + 17mA/9 × 2 = 15.1mA

+

4

.5mA × 2 = 1mA

+

7

1.1V(5)100pF50MHz = 27.5mA

+

8

7(2.1V–1.0V)/16.5Ω = 466.7mA

2. Finding P_D (V × I)

The first four current terms are multiplied by V_{CC}.

5V(20mA + 9.44mA + 15.1mA + 1mA) = 227.7mW

Term seven is multiplied by 1V (V_{OL}).

1V(27.5mA) = 27.5mW

Term eight is also multiplied 1V (V_{OL}).

1V(466.7mA) = 466.7mW

The total estimated power dissipation of an FB2031 with 5 outputs switching, at 25°C, with V_{CC} = 5V, with 2 outputs held static Low, and 2 inputs at 3.4V, with 100pF capacitive loads, no pull–downs, 16.5Ω pull–ups and 50MHz switching frequency is:

227.7 + 27.5 + 466.7 = 721.9mW

Term eight contributed over 65% of the power dissipated by the FB2031 in this example. The power dissipated by the IC with no external loading totals only 32% of the power.

3. Determine θ_{JA}

The FB2031 is packaged in the 52–pin PQFP. Using an average die size of 118 × 138 yields a θ_{JA} of 79°C/W @ 1W power dissipation (see θ_{JA} graph).

4. Determine θ_{JA} @ 721.9mW P_D

Using the AVERAGE EFFECT of POWER DISSIPATION on θ_{JA} graph calculate the percentage change in power = (0.7219W – 1W)/1W = –.28 (–28% change) then check the graph and see that θ_{JA} increases by 3.4%. So θ_{JA} increases to 79 + 79 × .034 = 81.7°C/W.

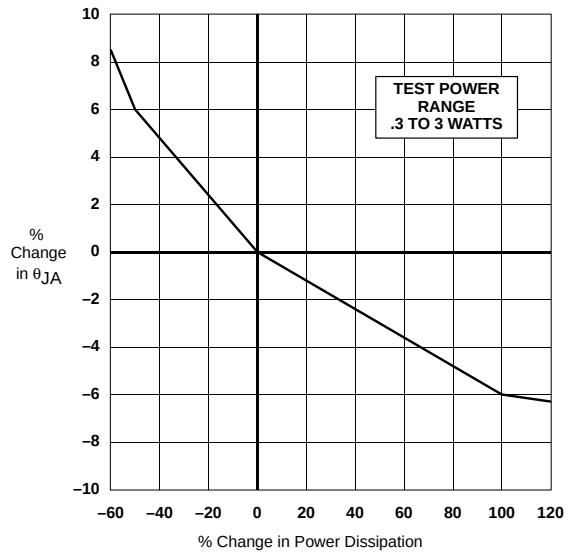
5. Assume 200 LFPM Air Flow

Calculate the effects of air flow by referring to the graph AVERAGE EFFECT of AIR FLOW on θ_{JA}. The θ_{JA} is decreased by 22.5% leaving a θ_{JA} of 81.7 – (.225 × 81.7) = 63.3°C/W.

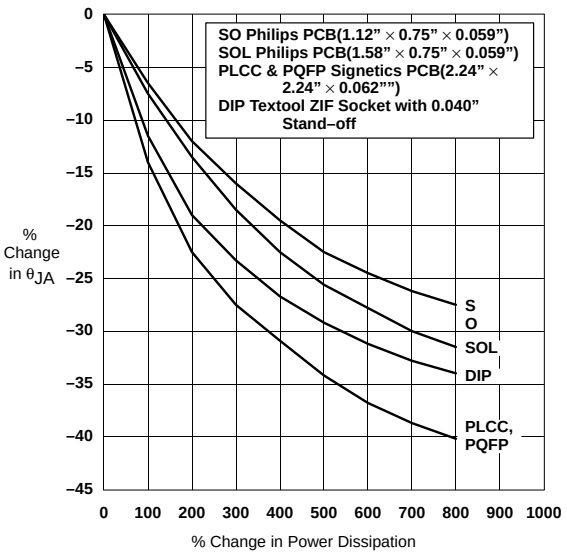
6. Final Calculations for T_J for the FB2031

$T_J = (P_D \times \theta_{JA}) + T_{amb}$ = (0.7219W × 63.3°C/W) + 70°C = 115.1°C. Referring to the warnings in the JUNCTION TEMPERATURE section, a 115.1°C T_J would constitute no temperature worries.

MODIFYING θ_{JA} FOR POWER DISSIPATION AND AIRFLOW



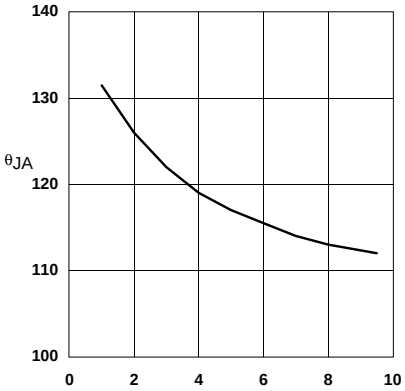
Average Effect of Power Dissipation on θ_{JA}



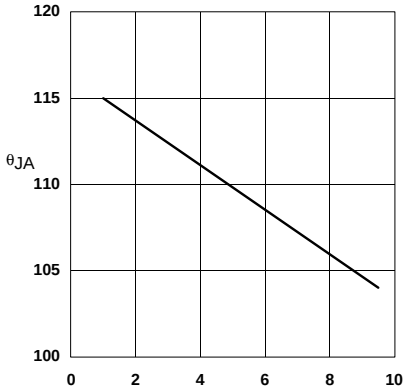
Average Effect of Air Flow on θ_{JA}

TYPICAL THERMAL RESISTANCE (θ_{JA}) in °C/W

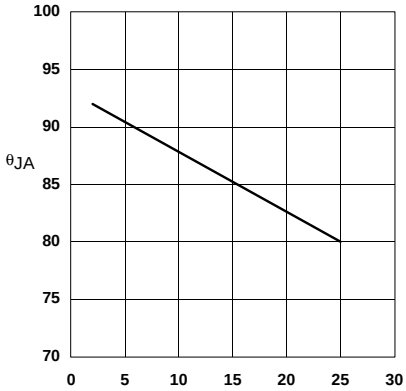
Typical θ_{JA} Data SO–14[1]



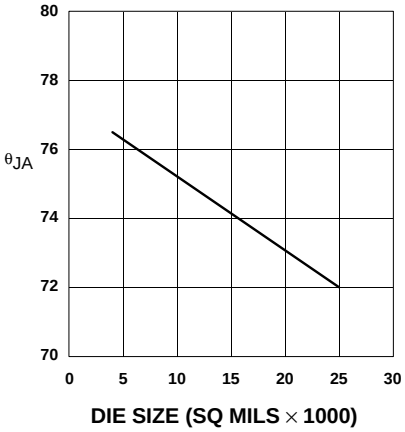
Typical θ_{JA} Data SO–16[1]



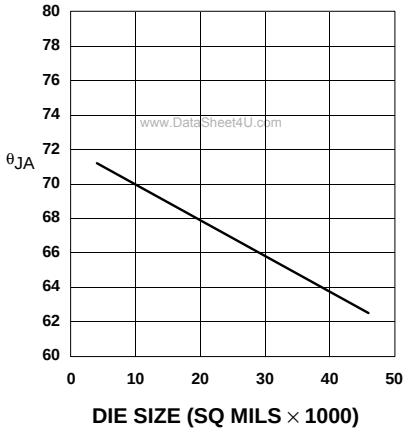
Typical θ_{JA} Data SOL–20[2]



Typical θ_{JA} Data SOL–24[2]



Typical θ_{JA} Data SOL–28[2]

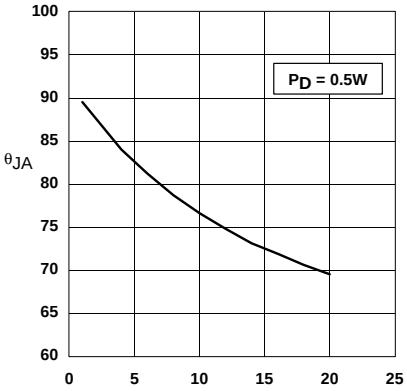


NOTES

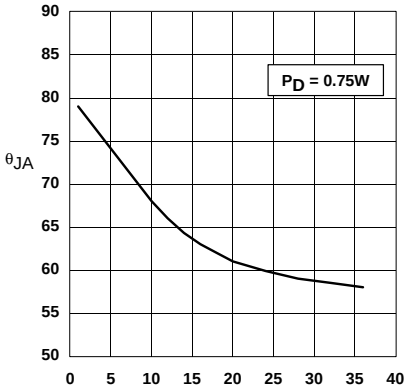
1. Power Dissipation 0.5W
   Test Ambiant Still Air
   Test Fixture Philips PCB (1.12” × 0.75” × 0.059”)
   Accuracy ±15%
2. Power Dissipation 0.7W
   Test Ambiant Still Air
   Test Fixture Philips PCB (1.58” × 0.75” × 0.059”)
   Accuracy ±15%

TYPICAL THERMAL RESISTANCE (θ_{JA}) in °C/W

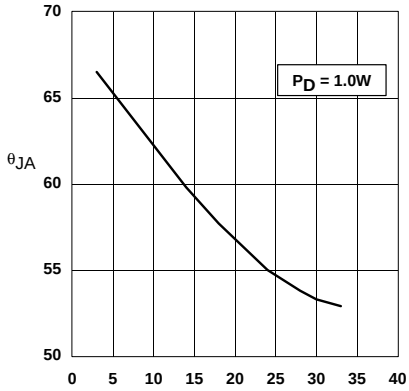
Typical θ_{JA} Data DIP–14 & 16



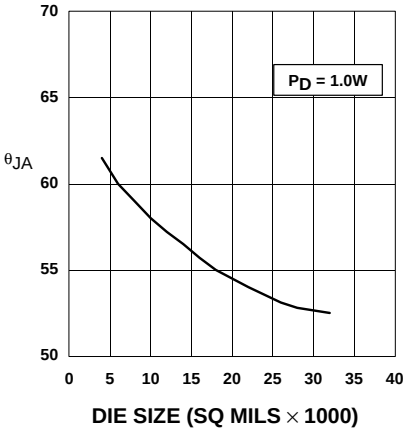
Typical θ_{JA} Data DIP–20



Typical θ_{JA} Data DIP–24



Typical θ_{JA} Data DIP–28



NOTE

Test Ambiant	Still Air
Test Fixture	Textool ZIF Socket .040” Stand–Off)
Accuracy	±15%

Thermal considerations for advanced logic families (Futurebus+, ABT and MULTIBYTE)

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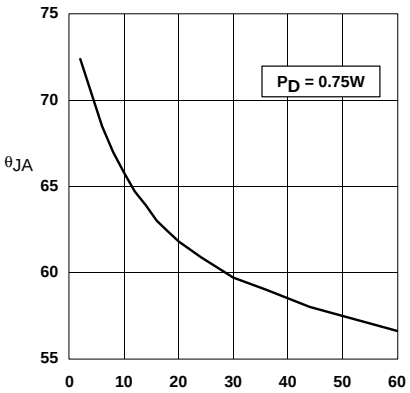
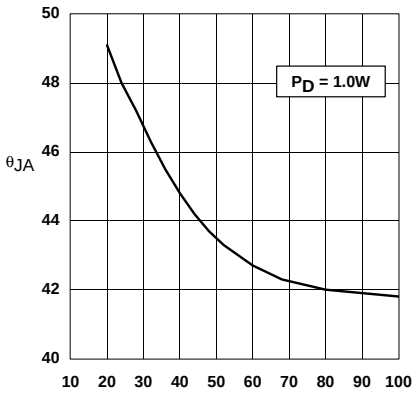
TYPICAL THERMAL RESISTANCE (θ_{JA}) in °C/W

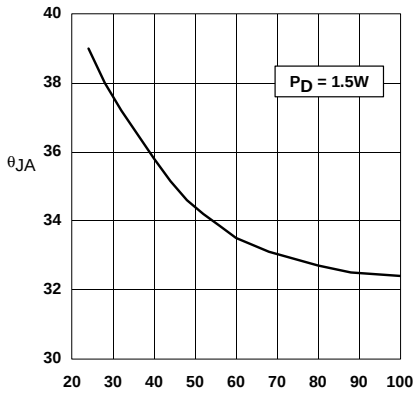
Typical θ_{JA} Data PLCC–28



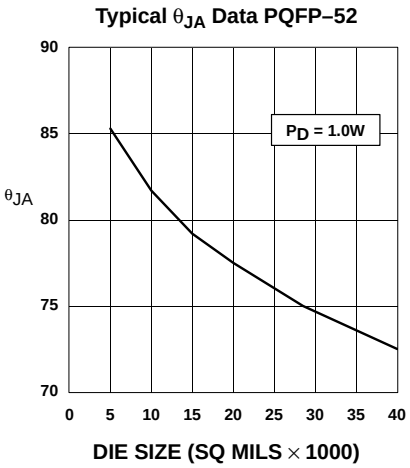
Typical θ_{JA} Data PLCC–68



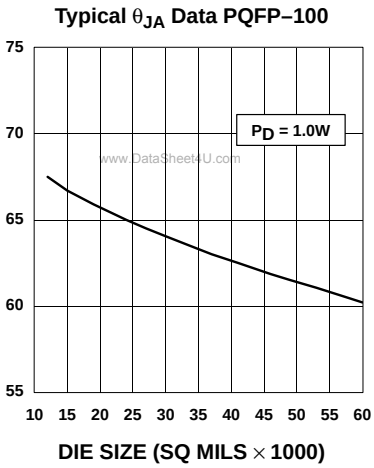
Typical θ_{JA} Data PLCC–84



Typical θ_{JA} Data PQFP–52



Typical θ_{JA} Data PQFP–100

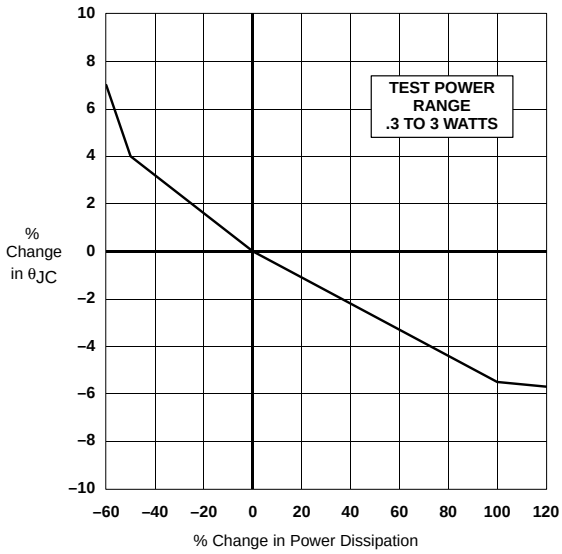


NOTES:

Test Ambiant	Still Air
Test Fixture	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy	±15%

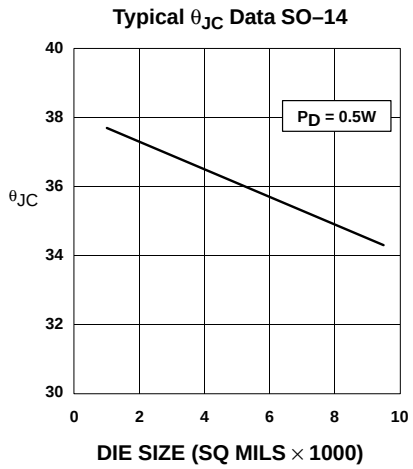
Data for the 20/24–pin SSOP is preliminary. Graphs are not yet available. Please see the table, "θ_{JA} AND θ_{JC} CALCULATIONS FOR ABT, MULTIBYTE, AND FUTUREBUS+" for the preliminary values.

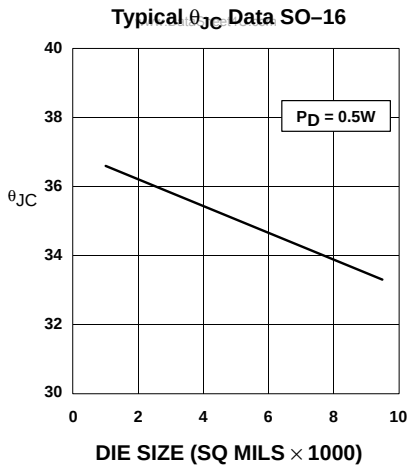
MODIFYING θ_{JC} FOR POWER DISSIPATION

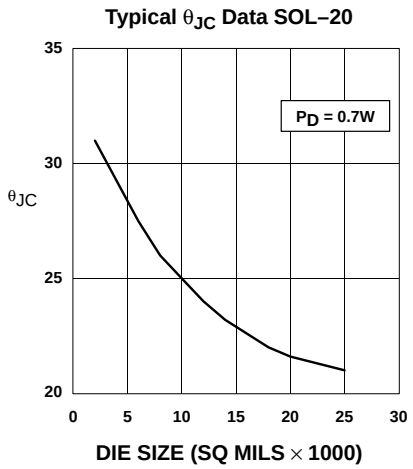


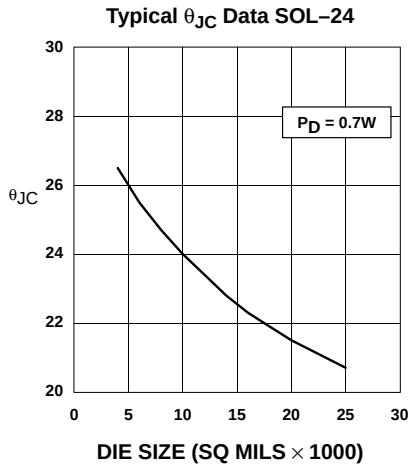
Average Effect of Power Dissipation on θ_{JC}

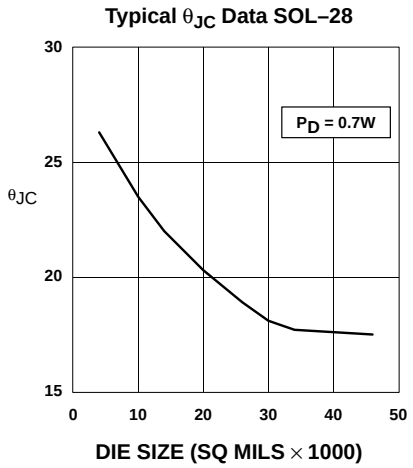
TYPICAL THERMAL RESISTANCE (θ_{JC}) in °C/W









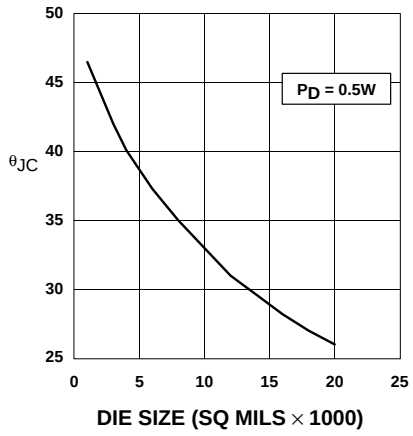


NOTE:

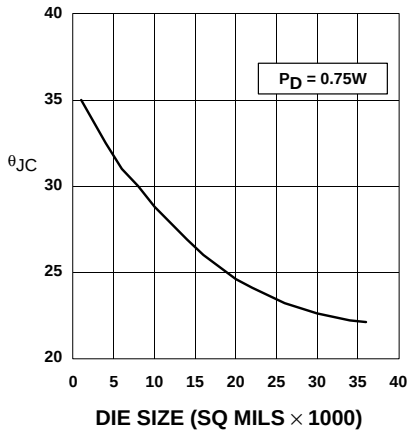
Test Fixture	Infinite Heat Sink
Accuracy	±15%

TYPICAL THERMAL RESISTANCE (θ_{JC}) in °C/W

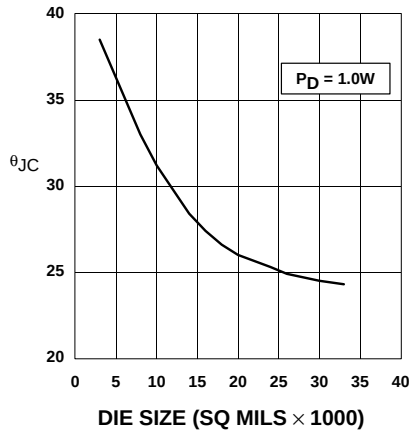
Typical θ_{JC} Data DIP–14 & 16



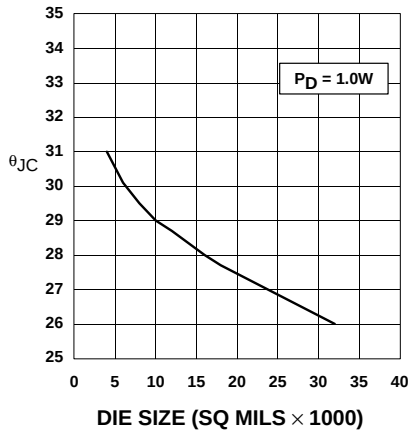
Typical θ_{JC} Data DIP–20



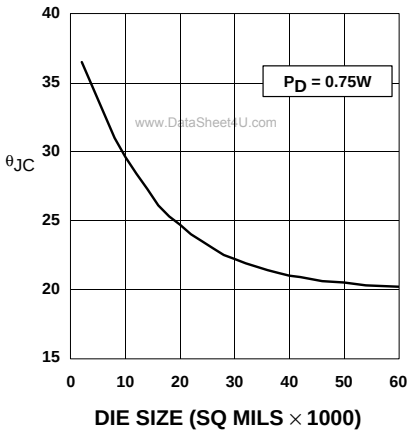
Typical θ_{JC} Data DIP–24



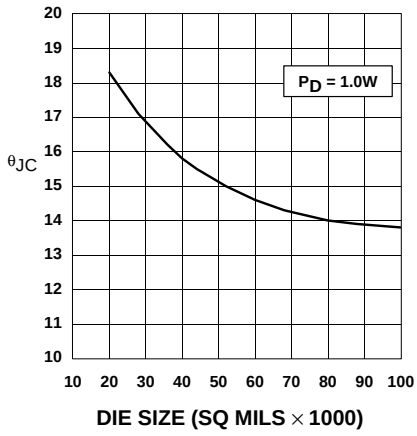
Typical θ_{JC} Data DIP–28



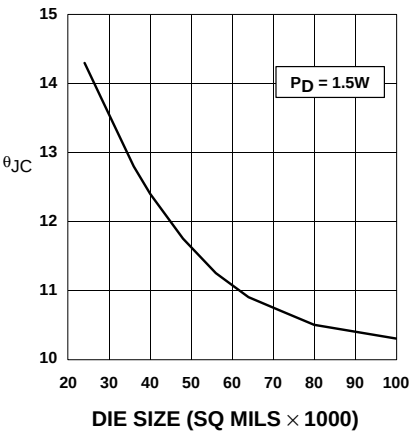
Typical θ_{JC} Data PLCC–28



Typical θ_{JC} Data PLCC–68



Typical θ_{JC} Data PLCC–84



NOTE:

Test Fixture	Infinite Heat Sink
Accuracy	±15%

Thermal considerations for advanced logic families (Futurebus+, ABT and MULTIBYTE)

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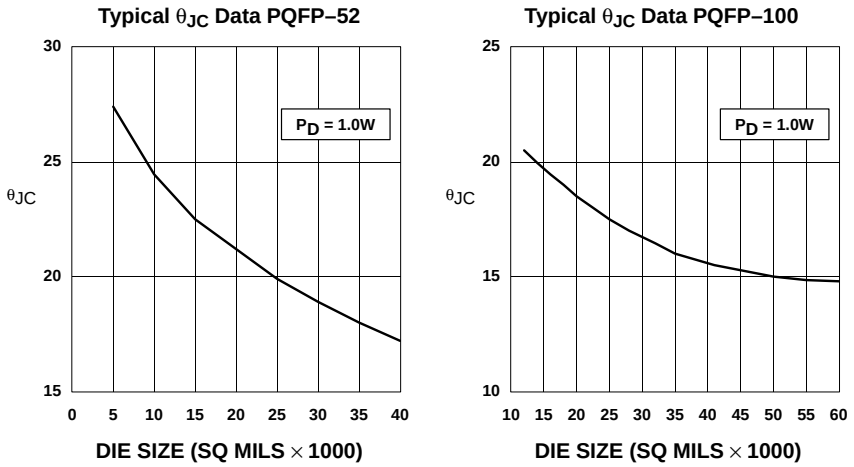
TYPICAL THERMAL RESISTANCE (θ_{JC}) in °C/W



NOTES:

Test Fixture	Infinite Heat Sink
Accuracy	±15%

Data for the 20/24–pin SSOP is preliminary. Graphs are not yet available. Please see the table, "θ_{JA} AND θ_{JC} CALCULATIONS FOR ABT, MULTIBYTE, AND FUTUREBUS+" for the preliminary values.

SYSTEM CONSIDERATIONS

The manner in which an IC package is mounted and positioned in its surrounding environment will have significant effects on operating junction temperatures. These conditions are under the control of the system designer and are worthy of serious consideration in PC board layout and system ventilation and airflow features.

Forced–air cooling will significantly reduce θ_{JA}. The figure entitled "AVERAGE EFFECT OF AIR FLOW ON θ_{JA}" provides curves resulting from Signetics evolution of the effect of air flow on each of the fundamental package families. These data are for approximate linear flow across the long dimension of the package. Air flow parallel to the long dimension of the package is generally a few percent more effective than air flow perpendicular to the long dimension of the package. In actual board layouts, other components can provide air flow blocking and flow turbulence, which may reflect the net reduction of θ_{JA} of a specific component. These issues should be carefully evaluated when using the data presented.

External heat sinks applied to an IC package can improve thermal resistance by increasing heat flow to the ambient environment. Heat sink performance will vary by size, material, design, and system air flow. Heat sinks can provide a substantial improvement.

Package mounting can affect thermal resistance. The data given herein relates to specific test environments; however, the general data holds true for other applications. Surface mount packages dissipate significant amounts of heat through the leads. Improving heat flow from package leads to ambient will decrease thermal resistance. The following factors have been investigated.

The *metal (copper) traces* on PC boards conduct heat away from the package and dissipate it to the ambient; thus the larger the trace area the lower the thermal resistance.

Package stand–off has a small effect on θ_{JA}. Boards with higher thermal conductivity (ceramic) may show the most pronounced benefit.

The use of *thermally conductive adhesive* under SO packages can lower thermal resistance by providing a direct heat flow path from the package to board. Naturally high thermal conductivity board material and/or cool board temperatures amplify this effect.

High thermal conductive board material will decrease thermal resistance. Data from Philips indicates that a change in board material from epoxy laminate to ceramic reduces thermal resistance.

CONCLUSION

Thermal management remains a major concern of producers and users of ICs. With the advent of SMD technology, a thorough understanding of the thermal characteristics of both the devices and the systems is very important. The smaller SMD package does have a higher θ_{JA} than its standard DIP counterpart — even with copper leadframes. The increased θ_{JA} is the major trade–off one must accept for package miniaturization. When the user considers all of the variables that affect the IC junction temperature, he is then prepared to take the maximum advantage of the tools, materials and data that are available.