



AM26LS32

QUAD EIA-422/423 Line Receiver with Three-State Outputs

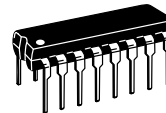
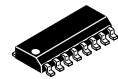
Motorola's Quad EIA-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when Pin 4 is a Logic "0" and Pin 12 is a Logic "1." A PNP device buffers each output control pin to assure minimum loading for either Logic "1" or Logic "0" inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of AM26LS32 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis – 30 mV (Typical) @ Zero Volts Common Mode
- Fast Propagation Times – 25 ns (Typical)
- TTL Compatible
- Single 5.0 V Supply Voltage
- Fail-Safe Input-Output Relationship. Output Always High When Inputs Are Open, Terminated or Shorted
- 6.0 k Minimum Input Impedance

QUAD EIA-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

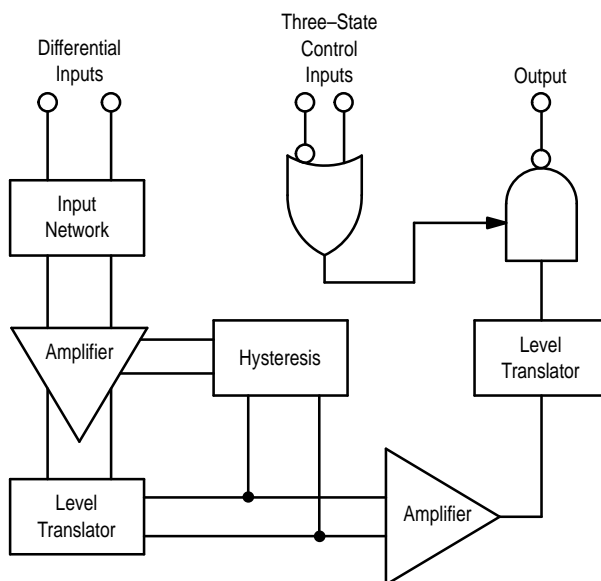
SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

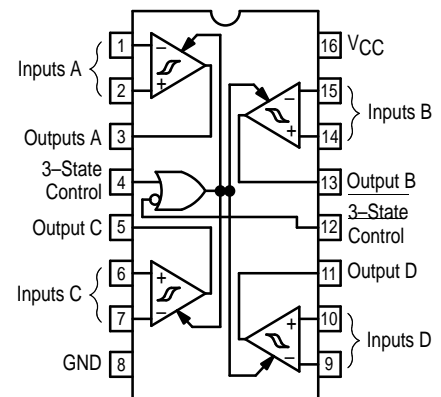


PC SUFFIX
PLASTIC PACKAGE
CASE 648

Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|------------|-----------------------------|-------------|
| AM26LS32PC | T _A = 0 to 70°C | Plastic DIP |
| MC26LS32D* | | SO-16 |

* Note that the surface mount MC26LS32D device uses the same die as in the plastic DIP AM26LS32DC device, but with an MC prefix to prevent confusion with the package suffix.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|-----------------------------------|-----------|---------------|------|
| Power Supply Voltage | V_{CC} | 7.0 | Vdc |
| Input Common Mode Voltage | V_{ICM} | ± 25 | Vdc |
| Input Differential Voltage | V_{ID} | ± 25 | Vdc |
| Three-State Control Input Voltage | V_I | 7.0 | Vdc |
| Output Sink Current | I_O | 50 | mA |
| Storage Temperature | T_{stg} | - 65 to + 150 | °C |
| Operating Junction Temperature | T_J | + 150 | °C |

RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Value | Unit |
|----------------------------------|-----------|----------------|------|
| Power Supply Voltage | V_{CC} | 4.75 to 5.25 | Vdc |
| Operating Ambient Temperature | T_A | 0 to + 70 | °C |
| Input Common Mode Voltage Range | V_{ICR} | - 7.0 to + 7.0 | Vdc |
| Input Differential Voltage Range | V_{IDR} | 6.0 | Vdc |

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$ and $V_{IC} = 0\text{ V}$. See Note 1.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------------------|----------|--------|-------------|---------------|
| Input Voltage – High Logic State (Three-State Control) | V_{IH} | 2.0 | – | – | V |
| Input Voltage – Low Logic State (Three-State Control) | V_{IL} | – | – | 0.8 | V |
| Differential Input Threshold Voltage (Note 2) ($-7.0\text{ V} \leq V_{IC} \leq 7.0\text{ V}$, $V_{IH} = 2.0\text{ V}$) ($I_O = -0.4\text{ mA}$, $V_{OH} \geq 2.7\text{ V}$) ($I_O = 8.0\text{ mA}$, $V_{OL} \leq 0.45\text{ V}$) | $V_{TH(D)}$ | – | – | 0.2 –0.2 | V |
| Input Bias Current ($V_{CC} = 0\text{ V}$ or 5.25) (Other Inputs at $-15\text{ V} \leq V_{in} \leq +15\text{ V}$) $V_{in} = +15\text{ V}$ $V_{in} = -15\text{ V}$ | $I_{IB(D)}$ | – | – | 2.3 –2.8 | mA |
| Input Resistance ($-15\text{ V} \leq V_{in} \leq +15\text{ V}$) | R_{in} | 6.0 K | – | – | Ohms |
| Input Balance and Output Level ($-7.0\text{ V} \leq V_{IC} \leq 7.0\text{ V}$, $V_{IH} = 2.0\text{ V}$, See Note 3) ($I_O = -0.4\text{ mA}$, $V_{ID} = 0.4\text{ V}$) ($I_O = 8.0\text{ mA}$, $V_{ID} = -0.4\text{ V}$) | V_{OH} V_{OL} | 2.7 – | – – | – 0.45 | V |
| Output Third State Leakage Current ($V_{I(D)} = +3.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_O = 0.4\text{ V}$) ($V_{I(D)} = -3.0\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_O = 2.4\text{ V}$) | I_{OZ} | – | – | –20 20 | μA |
| Output Short Circuit Current ($V_{I(D)} = 3.0\text{ V}$, $V_{IH} = 2.0\text{ V}$, $V_O = 0\text{ V}$, See Note 4) | I_{OS} | –15 | – | –85 | mA |
| Input Current – Low Logic State (Three-State Control) ($V_{IL} = 0.4\text{ V}$) | I_{IL} | – | – | –360 | μA |
| Input Current – High Logic State (Three-State Control) ($V_{IH} = 2.7\text{ V}$) ($V_{IH} = 5.5\text{ V}$) | I_{IH} | – | – | 20 100 | μA |
| Input Clamp Diode Voltage (Three-State Control) ($I_{IC} = -18\text{ mA}$) | V_{IK} | – | – | –1.5 | V |
| Power Supply Current ($V_{IL} = 0\text{ V}$) (All Inputs Grounded) | I_{CC} | – | – | 70 | mA |

- NOTES:**
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
 2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
 3. Refer to EIA-422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
 4. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|--------------|-----|-----|-----|------|
| Propagation Delay Time – Differential Inputs to Output (Output High to Low) (Output Low to High) | $t_{PHL(D)}$ | – | – | 30 | ns |
| | $t_{PLH(D)}$ | – | – | 30 | ns |
| Propagation Delay Time – Three–State Control to Output (Output Low to Third State) (Output High to Third State) (Output Third State to High) (Output Third State to Low) | t_{PLZ} | – | – | 35 | ns |
| | t_{PHZ} | – | – | 35 | ns |
| | t_{PZH} | – | – | 30 | ns |
| | t_{PZL} | – | – | 30 | ns |

Figure 1. Switching Test Circuit and Wave for Propagation Delay Differential Input to Output

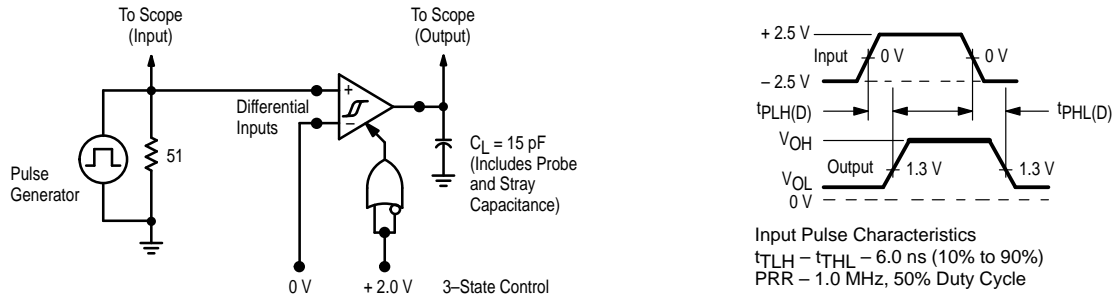
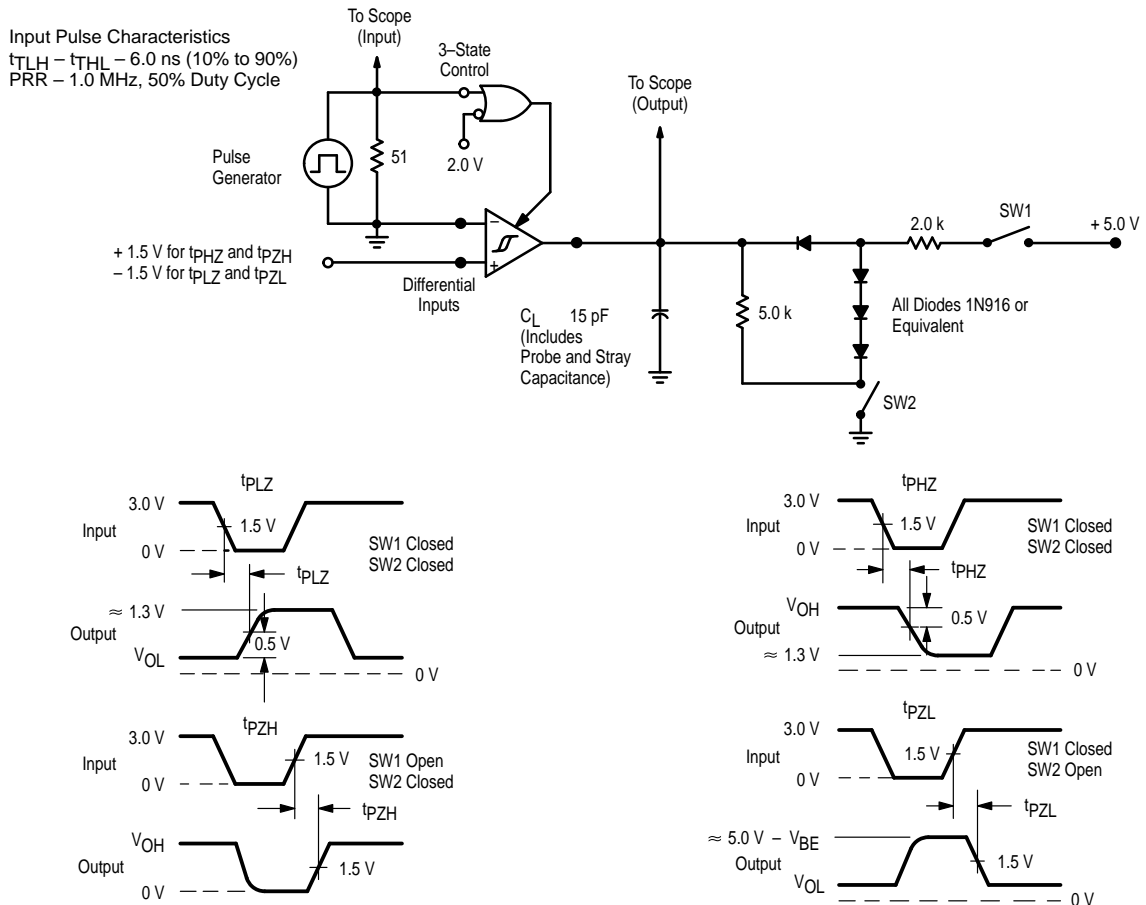


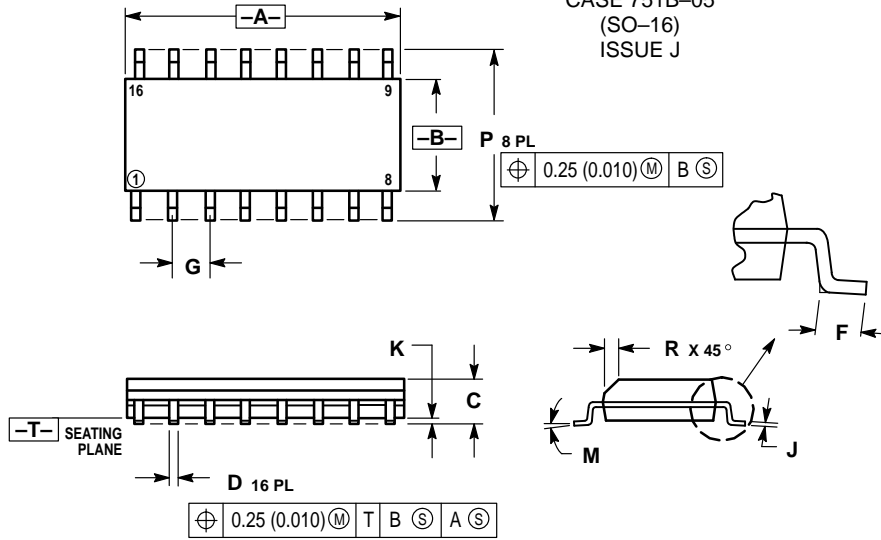
Figure 2. Propagation Delay Three–State Control Input to Output



AM26LS32

OUTLINE DIMENSIONS

D SUFFIX PLASTIC PACKAGE CASE 751B-05 (SO-16) ISSUE J

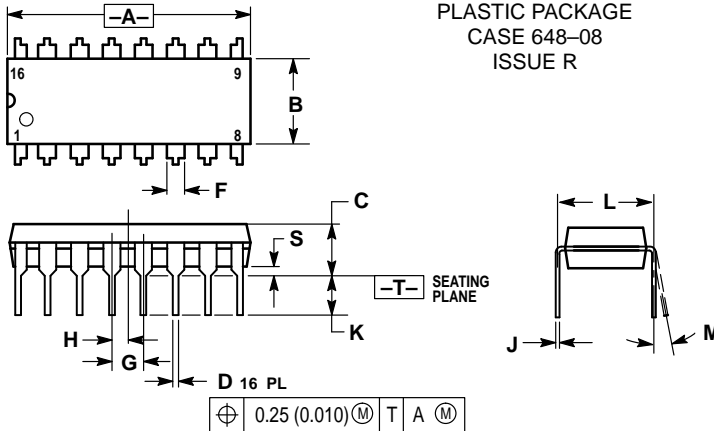


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

PC SUFFIX PLASTIC PACKAGE CASE 648-08 ISSUE R



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

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How to reach us:

USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609
INTERNET: http://Design-NET.com

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



AM26LS32/D

