Monolithic Digital IC

# LB1924

## Power Brushless Motor Driver IC for Office Automation Equipment

## Overview

The LB1924 is a direct PWM drive output driver IC appropriate for the power brushless motors used in office automation equipment. It includes a speed control circuit, an FG amplifier, and other peripheral circuits and allows a drive circuit to be implemented with a single IC. It allows the number of external components to be reduced by including a lock protection circuit, a kickback absorption diode for the lower output side, and other components on chip.
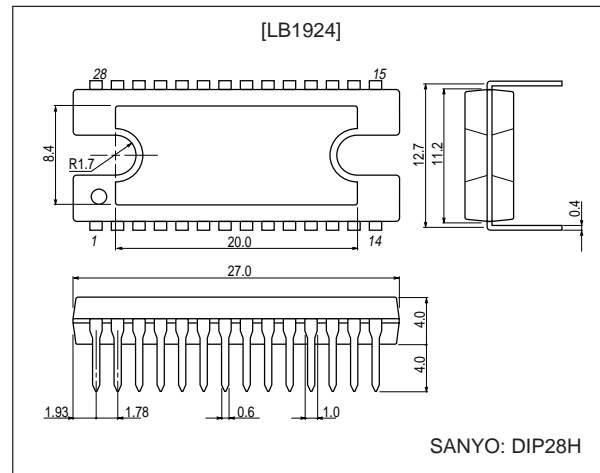
## Functions

• Breakdown voltage: 30 V, output current: 3.1 A
• Direct PWM drive output
• Speed discriminator + PLL speed control technique
• Crystal oscillator circuit
• Built-in FG and integrating amplifiers
• Forward/reverse switching circuit
• Speed lock detection output
• On-chip lower output side kickback absorption diode
• Full complement of built-in protection circuits, including lock protection, current limiter, and thermal protection circuits

## Package Dimension

unit: mm

### 3147B-DIP28H



SANYO: DIP28H

## SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

# Specifications

## Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$ max | | 30 | V |
| | $V_M$ max | $V_{CC} \geq V_M$ | 30 | V |
| Output current | $I_O$ max | t ≤ 500 ms | 3.1 | A |
| Allowable power dissipation | Pd max1 | Independent IC | 3 | W |
| | Pd max2 | With an arbitrarily large heat sink | 20 | W |
| Operating temperature | Topr | | −20 to +80 | °C |
| Storage temperature | Tstg | | −55 to +150 | °C |

## Allowable Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | | 9.5 to 28 | V |
| | $V_M$ | $V_{CC} \geq V_M$ | 9 to 28 | V |
| Regulated voltage output current | $I_{REG}$ | | 0 to −20 | mA |
| Lock detection output current | $I_{LD}$ | | 0 to 15 | mA |

## Electrical Characteristics at Ta = 25°C, $V_{CC} = V_M$ = 24 V

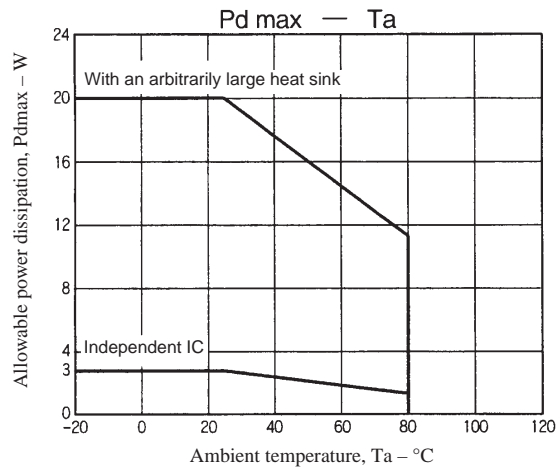| Parameter | Symbol | Conditions | Ratings min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Current drain | $I_{CC}1$ | | | 31 | 40 | mA |
| | $I_{CC}2$ | When stopped | | 5.5 | 8.0 | mA |
| Output saturated voltage | $V_O$ sat1 | $I_O$ = 1A, $V_O$ (Sink) + $V_O$ (Source) | | 2.0 | 2.5 | V |
| | $V_O$ sat2 | $I_O$ = 2A, $V_O$ (Sink) + $V_O$ (Source) | | 2.6 | 3.2 | V |
| Output leakage current | $I_O$ leak | | | | 100 | µA |
| [5-V Regulated Voltage Output] | | | | | | |
| Output voltage | $V_{REG}$ | $I_O$ = −5 mA | 4.65 | 5.00 | 5.35 | V |
| Line regulation | $\Delta V_{REG}1$ | $V_{CC}$ = 9.5 to 28 V | | 30 | 100 | mV |
| Load regulation | $\Delta V_{REG}2$ | $I_O$ = −5 to −20 mA | | 20 | 100 | mV |
| [Hall Amplifier] | | | | | | |
| Input bias current | $I_{HB}$ | | −4 | −1 | | µA |
| Common-mode input voltage range | $V_{ICM}$ | | 1.5 | | $V_{REG}$−1.5 | V |
| Hall input sensitivity | | | 60 | | | mVp-p |
| Hysteresis | $\Delta V_{IN}$ | | 8 | 14 | 24 | mV |
| Input voltage (low to high) | $V_{SLH}$ | | | 7 | | mV |
| Input voltage (high to low) | $V_{SHL}$ | | | −7 | | mV |
| [RC Oscillator] | | | | | | |
| Output high-level voltage | $V_{OH(CR)}$ | | 2.4 | 2.7 | 3.0 | V |
| Output low-level voltage | $V_{OL(CR)}$ | | 1.1 | 1.4 | 1.7 | V |
| Oscillator frequency | $f_{(CR)}$ | R = 22 kΩ, C = 4700 pF | | 19 | | kHz |
| Amplitude | $V_{(CR)}$ | | 1.0 | 1.25 | 1.5 | Vp-p |
| [CROCK Oscillator] | | | | | | |
| Output high-level voltage | $V_{OH(RK)}$ | | 2.5 | 2.8 | 3.1 | V |
| Output low-level voltage | $V_{OL(RK)}$ | | 0.5 | 0.8 | 1.1 | V |
| External capacitor charging current | $I_{CHG}1$ | | −10 | −8 | −6 | µA |
| | $I_{CHG}2$ | | 6 | 8 | 10 | µA |
| Oscillator frequency | $f_{(RK)}$ | C = 0.047 µF | | 44 | | Hz |
| Amplitude | $V_{(RK)}$ | | 1.75 | 1.95 | 2.25 | V |
| [Current Limiter Operation] | | | | | | |
| Limiter | $V_{CC}$-$V_M$ | | 0.45 | 0.5 | 0.55 | V |
| [Thermal Shutdown Operation] | | | | | | |
| Thermal shutdown temperature | TSD | Design target value (junction temperature) | 150 | 180 | | °C |
| Hysteresis | ΔTSD | Design target value (junction temperature) | | 40 | | °C |

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| Parameter | Symbol | Conditions | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|
| **[FG Amplifier]** | | | | | | |
| Input offset voltage | $V_{IO(FG)}$ | | −10 | | +10 | mV |
| Input bias current | $I_{B(FG)}$ | | −1 | | +1 | µA |
| Output high-level voltage | $V_{OH(FG)}$ | $I_{FGO}$ = −0.2 mA | $V_{REG}$−1.2 | $V_{REG}$−0.8 | | V |
| Output low-level voltage | $V_{OL(FG)}$ | $I_{FGO}$ = 0.2 mA | | 0.8 | 1.2 | V |
| FG input sensitivity | | Gain times 100 | 3 | | | mV |
| Schmitt sensitivity for the next stage | | Design target value | 100 | 180 | 250 | mV |
| Operating frequency range | | | | | 2 | kHz |
| Open loop gain | | f $_{(FG)}$ = 2 kHz | 45 | 51 | | dB |
| **[Speed Discriminator]** | | | | | | |
| Output high-level voltage | $V_{OH(D)}$ | $I_{DO}$ = −0.1 mA | $V_{REG}$−1.0 | $V_{REG}$−0.7 | | V |
| Output low-level voltage | $V_{OL(D)}$ | $I_{DO}$ = 0.1 mA | | 0.8 | 1.1 | V |
| Number of counts | | | | 512 | | |
| **[PLL Output]** | | | | | | |
| Output high-level voltage | $V_{OH(P)}$ | $I_{PO}$ = −0.1 mA | $V_{REG}$−1.8 | $V_{REG}$−1.5 | $V_{REG}$−1.2 | V |
| Output low-level voltage | $V_{OL(P)}$ | $I_{PO}$ = 0.1 mA | 1.2 | 1.5 | 1.8 | V |
| **[Lock Detector]** | | | | | | |
| Output low-level voltage | $V_{OL(LD)}$ | $I_{LD}$ = 10 mA | | 0.15 | 0.5 | V |
| Lock range | | | | 6.25 | | % |
| **[Integrator]** | | | | | | |
| Input bias current | $I_{B(INT)}$ | | −0.4 | | +0.4 | µA |
| Output high-level voltage | $V_{OH(INT)}$ | $I_{INTO}$ = −0.2 mA | $V_{REG}$−1.2 | $V_{REG}$−0.8 | | V |
| Output low-level voltage | $V_{OL(INT)}$ | $I_{INTO}$ = 0.2 mA | | 0.8 | 1.2 | V |
| Open-loop gain | | f (INT) = 1 kHz | 45 | 51 | | dB |
| Gain-bandwidth product | | Design target value | | 450 | | kHz |
| Reference voltage | | Design target value | −5% | $V_{REG}$/2 | 5% | V |
| **[Crystal Oscillator]** | | | | | | |
| Operating frequency range | $f_{OSC}$ | | 1 | | 10 | MHz |
| Low-level pin voltage | $V_{OSCL}$ | $I_{OSC}$ = −0.5 mA | | 1.7 | | V |
| High-level pin current | $I_{OSCH}$ | $V_{OSC}$ = $V_{OSCL}$ +0.3 V | | 0.5 | | mA |
| **[Start/Stop Pin]** | | | | | | |
| High-level input voltage range | $V_{IH(S/S)}$ | | 3.5 | | $V_{REG}$ | V |
| Low-level input voltage range | $V_{IL(S/S)}$ | | 0 | | 1.5 | V |
| Input open voltage | $V_{IO(S/S)}$ | | $V_{REG}$−0.5 | | $V_{REG}$ | V |
| Hysteresis | $\Delta V_{IN}$ | | 0.35 | 0.50 | 0.65 | V |
| High-level input current | $I_{IH(S/S)}$ | $V_{(S/S)}$ = $V_{REG}$ | −10 | 0 | +10 | µA |
| Low-level input current | $I_{IL(S/S)}$ | $V_{(S/S)}$ = 0 V | −280 | −210 | | µA |
| **[Forward/Reverse Pin]** | | | | | | |
| Output high-level voltage | $V_{IH(F/R)}$ | | 3.5 | | $V_{REG}$ | V |
| Output low-level voltage | $V_{IL(F/R)}$ | | 0 | | 1.5 | V |
| Input open voltage | $V_{IO(F/R)}$ | | $V_{REG}$−0.5 | | $V_{REG}$ | V |
| Hysteresis | $\Delta V_{IN}$ | | 0.35 | 0.50 | 0.65 | V |
| Output high-level voltage | $I_{IH(F/R)}$ | $V_{(F/R)}$ = $V_{REG}$ | −10 | 0 | +10 | µA |
| Output low-level voltage | $I_{IL(F/R)}$ | $V_{(F/R)}$ = 0 V | −280 | −210 | | µA |

## Pd max — Ta



Graph: Allowable power dissipation, Pdmax – W (y-axis, values 0, 3, 4, 8, 12, 16, 20, 24) vs Ambient temperature, Ta – °C (x-axis, values −20, 0, 20, 40, 60, 80, 100, 120). Curves labeled "With an arbitrarily large heat sink" and "Independent IC".

## Pin Assignment



Top pins (left to right): OUT1 [28], IN3− [27], IN3+ [26], IN2− [25], IN2+ [24], IN1− [23], IN1+ [22], GND1 [21], CR [20], CROCK [19], FG$_{IN}$+ [18], FG$_{IN}$− [17], FG$_{OUT}$ [16], LD [15]

LB1924

Bottom pins (left to right): [1] OUT2, [2] OUT3, [3] GND2, [4] V$_{CC}$, [5] V$_M$, [6] V$_{REG}$, [7] F/R, [8] S/S, [9] XO, [10] XI, [11] INT$_{OUT}$, [12] INT$_{IN}$, [13] P$_{OUT}$, [14] D$_{OUT}$

Top view

## Truth Table

| | Source | F/R = L | | | F / R = H | | |
|---|---|---|---|---|---|---|---|
| | Sink | IN 1 | IN2 | IN 3 | IN 1 | IN 2 | IN 3 |
| 1 | OUT2 → OUT1 | H | L | H | L | H | L |
| 2 | OUT3 → OUT1 | H | L | L | L | H | H |
| 3 | OUT3 → OUT2 | H | H | L | L | L | H |
| 4 | OUT1 → OUT2 | L | H | L | H | L | H |
| 5 | OUT1 → OUT3 | L | H | H | H | L | L |
| 6 | OUT2 → OUT3 | L | L | H | H | H | L |

## Equivalent Circuit Block Diagram
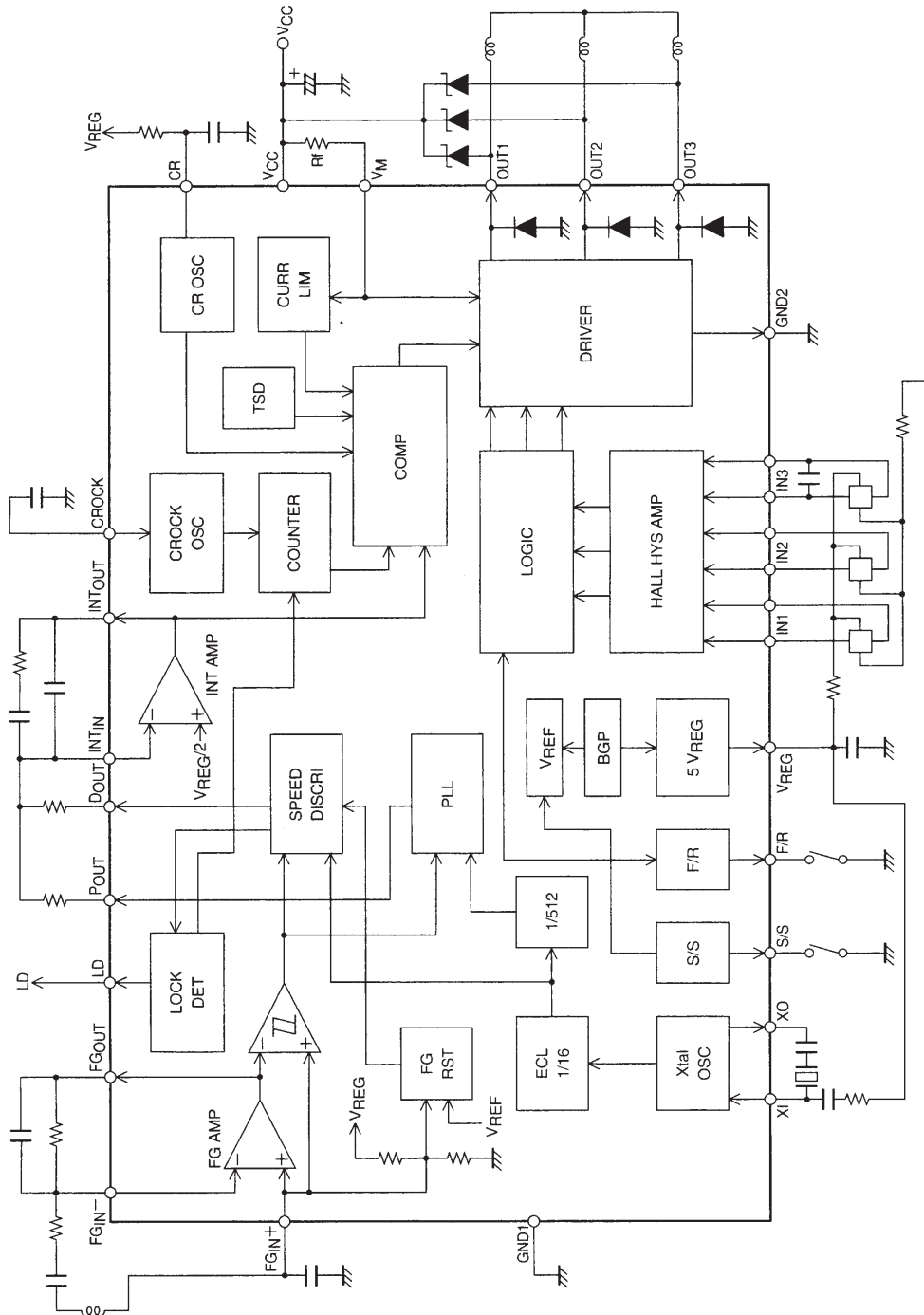


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**Functional Description**

1. Speed control circuit

   This IC uses a speed discriminator circuit and a PLL circuit in combination for speed control. The speed control circuit outputs an error signal once every two FG periods (a charge pump technique). The PLL circuit outputs a phase error signal once every FG period (also a charge pump technique). As compared with the earlier speed control technique of using only a speed discriminator, the combined speed discriminator/PLL circuit technique is better able to suppress speed fluctuations when used with motors with large load variations. The FG servo frequency is determined by the following equation, which means that the motor speed is determined by the number of FG pulses and the crystal oscillator frequency.

   $$f_{FG}(servo) = f_{OSC}/8192$$

   $f_{OSC}$: Crystal oscillator frequency

2. Output drive circuit

   This IC adopts a direct PWM drive technique to minimize the power loss in the output. The output transistor is always saturated when on, and the motor drive power is adjusted by varying the duty with which the output is on. Since the lower side output transistor is used for output switching, a Schottky diode or similar device must be connected between OUT and $V_{CC}$. (This is because a through current will flow at the instant the lower side transistor turns on unless a diode with a short reverse recovery time is used.) The diode between OUT and ground is included on chip in this device. If this becomes a problem for large output currents, (e.g. if the output waveform is disturbed during lower side kickback) attach an external rectifying (or Schottky) diode.
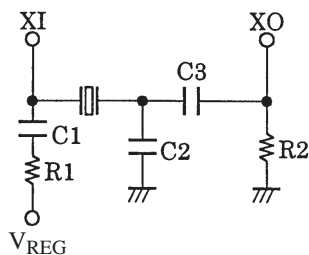
3. Current limiter

   The current limiter circuit limits the output to a current determined by the equation $I = V_{RF}/R_f$, where $V_{RF} = 0.5$ V (typical) and $R_f$ is the current detection resistor. The current limiting operation consists of reducing the output on duty to lower the current.

4. Reference clock

   Either of the two following input methods can be used for the speed control clock
   • Using a crystal oscillator element
   — When using a crystal oscillator element, connect the crystal, capacitors, and resistors as shown in the figure below to form an oscillator circuit.



Sample External Circuit Constants (Reference values)

| Oscillator frequency (MHz) | C1 (µF) | C2 (µF) | C3 (µF) | R1 (Ω) | R2 (Ω) |
|---|---|---|---|---|---|
| 1 to 3 | 0.1 | 47 | 220 | 220 K | — |
| 3 to 5 | 0.1 | 18 | 100 | 100 K | — |
| 5 to 7 | 0.1 | — | 47 | 47 K | — |
| 7 to 10 | 0.1 | — | 33 | 10 K | 4.7 K |

C1, R1:  Oscillator stabilization
C3:       Oscillator coupling
C2:       Overtone prevention
R2:       Oscillator operating margin improvement

This circuit and these circuit constant values are provided for reference only. Always verify application circuits with the supplier of the oscillator element to assure that the effects of the characteristics of the oscillator element itself, the printed circuit board wiring, floating capacitances, and other aspects are accounted for appropriately.
(Notes on printed circuit board lines)
Floating capacitances on the printed circuit board can easily affect crystal oscillator circuits, since these are high-speed circuits. The printed circuit board lines connecting these components should be kept as short and as narrow as possible and other measures to reduce floating capacitances should be considered as well.
In this external circuit, the line between the oscillator element and C3 (C2) is particularly subject to floating capacitance problems and requires special care.

- External clock (A frequency equivalent to the crystal oscillator frequency: 1 to 10 MHz)
  — If a frequency equivalent to a crystal oscillator frequency is input from an external source, input that signal through a series resistor of about 13 kΩ to the XI pin. The XO pin should be left open.
    Input signal levels:
      Low-level voltage: 0 to 0.8 V
      High-level voltage: 2.5 to 5.0 V

5. Speed lock range
   The speed lock range is ±6.25% of the set speed. When the motor speed is in the lock range the LD pin will go low (open collector output). The IC controls the motor speed by changing the motor drive output on duty according to the speed error signal if the motor speed goes outside the lock range.

6. PWM frequency
   The PWM frequency is determined by the capacitor and resistor connected to the CR pin.
   $$f_{PWM} \approx 1/(0.5 \times C \times R)$$
   A PWM frequency in the range 15 to 25 kHz is desirable. If the PWM frequency is too low, the motor may resonate at the PWM frequency when locked resulting in noise, since that frequency will be in the audible range. If the PWM frequency is too high, the switching loss in the output transistor will increase. The value of the resistor must be over 5 kΩ.

7. Hall input signals
   The signals input as the Hall inputs must have amplitudes that exceed the hysteresis, which has a maximum value of 24 mV. Considering noise, inputs with amplitudes of at least 100 mV are desirable. Attach a noise rejection capacitor (around 0.001 to 0.01 μF) across the IN3 Hall input (pins 26 and 27). Since these pins are adjacent to the OUT1 output pin, noise in this input may cause disturbances in the output waveforms.

8. F/R switching
   The F/R pin can be used to change the direction of motor rotation. However the following points must be observed when designing applications that will change the motor direction while the motor is turning.
   • Application circuit must be designed to handle the through current that occurs when the direction is switched. However, increases in the $V_{CC}$ voltage during switching due to motor current flowing into the power supply system instantaneously, must not exceed the rated voltage (30 V) of the device. Increase the value of the capacitor between power supply and ground if this is a problem.
   • If the motor current after switching exceeds the current limiter upper limit, the lower side transistor will be turned off. However, the high side transistor will go to the short braking state, and a current determined by the motor reverse voltage and the coil resistance will flow in this transistor. Applications must be designed so that this current does not exceed the rated current, 3.1 A. In general, switching the direction with the F/R pin at high motor speeds is dangerous.

9. Lock protection circuit
   This IC includes a built-in lock protection circuit to protect the IC and the motor when the motor is locked. In the start state, if the LD output remains high for a fixed period (the unlocked state), the lower side transistor is turned off. The capacitance of the capacitor connected to the CROCK pin sets this time. A time of a few seconds can be set with a capacitance under 0.1 μF.
   Set time (seconds) $\approx 52 \times C$ (μF)
   To release the lock protection state, the IC must be set to the stopped state or the power must be turned off and reapplied. The CROCK pin must be connected to ground if the lock protection circuit is not used.

10. Power supply stabilization
    The large currents drawn by this IC can adversely affect the power supply voltage. Therefore a capacitor with a sufficiently large value must be inserted between the $V_{CC}$ pin and ground. If a diode is inserted in the power supply line to protect against destruction due to accidentally connecting the power supply with the polarity reversed, the power supply line voltage will be even more easily affected and an even larger capacitor will be required.

## Pin Functions

| Pin No. | Pin | Pin function | Equivalent circuit |
|---|---|---|---|
| 28<br>1<br>2 | OUT1<br>OUT2<br>OUT3 | Motor drive outputs<br>Connect Schottky diodes between these outputs and $V_{CC}$. |  |
| 3 | GND2 | Output block ground | |
| 5 | $V_M$ | Output block power supply and output current detection.<br>Connect a resistor ($R_f$) with a small resistance between this pin and $V_{CC}$.<br>The output current is limited to a current set according to the equation $I_{OUT} = V_{RF}/R_f$. | |
| 4 | $V_{CC}$ | Power supply (blocks other than the output block) | |
| 6 | $V_{REG}$ | Regulated power supply output (5-V output)<br>Insert a capacitor (about 0.1 µF) between this pin and ground for regulation. |  |
| 7 | F/R | Forward/reverse control<br>Low: 0 to 1.5 V<br>High: 3.5 to $V_{REG}$<br>The open state functions as a high-level input.<br>Has a hysteresis of about 0.5 V.<br>Low: Forward<br>High or open: Reverse |  |
| 8 | S/S | Start/stop control<br>Low: 0 to 1.5 V<br>High: 3.5 to $V_{REG}$<br>The open state functions as a high-level input.<br>Has a hysteresis of about 0.5 V.<br>Low: Start<br>High or open: Stop |  |

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| Pin No. | Pin | Pin function | Equivalent circuit |
|---|---|---|---|
| 9<br>10 | XO<br>XI | Crystal oscillator connection.<br>The reference clock signal is generated by connecting a crystal oscillator element to these pins.<br>If an external clock (with a frequency of a few MHz) is used, connect that signal to the XI pin through a series resistor of about 13 kΩ, and leave the XO pin open. | <br>A07267 |
| 11 | INT$_{OUT}$ | Integrator amplifier output (speed control output) | <br>A07268 |
| 12 | INT$_{IN}$ | Integrator amplifier input | <br>A07269 |
| 13 | P$_{OUT}$ | PLL circuit output | <br>A07270 |

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| Pin No. | Pin | Pin function | Equivalent circuit |
|---------|-----|--------------|--------------------|
| 14 | D$_{OUT}$ | Speed discriminator output.<br>High: Acceleration<br>Low: Deceleration | <br>A07271 |
| 15 | LD | Speed lock detection output<br>Outputs a low level when the motor speed is in the lock range (±6.25%). | <br>A07272 |
| 16 | FG$_{OUT}$ | FG amplifier output | <br>A07273 |
| 17 | FG$_{IN}$− | FG amplifier input | <br>A07274 |
| 18 | FG$_{IN}$+ | FG amplifier input (bias input).<br>The logic block initial reset is applied by connecting a capacitor (of about 0.1 µF) between FG$_{IN}$+ and ground. | |
| 19 | CROCK | Setting for the lock protection circuit operating time.<br>An operating time of about 2.5 seconds can be set by connecting a capacitor of about 0.047 µF between the CROCK pin and ground. | <br>A07275 |

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| Pin No. | Pin | Pin function | Equivalent circuit |
|---|---|---|---|
| 20 | CR | PWM oscillator frequency setting.<br>Connect a resistor (R) between this pin and $V_{REG}$ and a capacitor (C) between this pin and ground. Values of R = 22 kΩ, and C = 4700 pF set a frequency of about 19 kHz. |  |
| 21 | GND1 | Ground (blocks other than the output block) | |
| 22<br>23<br>24<br>25<br>26<br>27 | IN1⁺<br>IN1⁻<br>IN2⁺<br>IN2⁻<br>IN3⁺<br>IN3⁻ | Hall inputs<br>An input with IN⁺ > IN⁻ is taken to be a high level, and the opposite state is taken to be a low level. Hall signals with amplitudes greater that 100 mVp-p (differential) are desirable. If noise on the Hall signals is a problem, connect capacitors between the IN⁺ and IN⁻ pins. |  |