LB1924



Power Brushless Motor Driver IC for Office Automation Equipment

Overview

The LB1924 is a direct PWM drive output driver IC appropriate for the power brushless motors used in office automation equipment. It includes a speed control circuit, an FG amplifier, and other peripheral circuits and allows a drive circuit to be implemented with a single IC. It allows the number of external components to be reduced by including a lock protection circuit, a kickback absorption diode for the lower output side, and other components on chip.

Functions

- Breakdown voltage: 30 V, output current: 3.1 A
- Direct PWM drive output
- Speed discriminator + PLL speed control technique
- · Crystal oscillator circuit
- Built-in FG and integrating amplifiers
- · Forward/reverse switching circuit
- Speed lock detection output
- On-chip lower output side kickback absorption diode
- Full complement of built-in protection circuits, including lock protection, current limiter, and thermal protection circuits

Package Dimension

unit: mm

3147B-DIP28H



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Specifications Absolute Maximum Ratings at $Ta=25^{\circ}\mathrm{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Mandana and Kanada and	V _{CC} max		30	V
Maximum supply voltage	V _M max	$V_{CC} \ge V_{M}$	30	V
Output current	I _O max	$t \le 500 \text{ ms}$	3.1	А
	Pd max1	Independent IC	3	W
Allowable power dissipation	Pd max2	With an arbitrarily large heat sink	20	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

Allowable Operating Conditions at $Ta=25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Our all and the second	V _{CC}		9.5 to 28	V
Supply voltage range	VM	$V_{CC} \ge V_M$	9 to 28	V
Regulated voltage output current	I _{REG}		0 to -20	mA
Lock detection output current	I _{LD}		0 to 15	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = V_M = 24 V

Paramotor	Symbol	Conditions		Linit		
Faidhleter	Symbol	Conditions	min	typ	max	Unit
	I _{CC} 1			31	40	mA
Current drain	I _{CC} 2	When stopped		5.5	8.0	mA
	V _O sat1	$I_O = 1A, V_O (Sink) + V_O (Source)$		2.0	2.5	V
Output saturated voltage	V _O sat2	$I_O = 2A, V_O (Sink) + V_O (Source)$		2.6	3.2	V
Output leakage current	I _O leak				100	μA
[5-V Regulated Voltage Output]						
Output voltage	V _{REG}	$I_{O} = -5 \text{ mA}$	4.65	5.00	5.35	V
Line regulation	$\Delta V_{REG}1$	V _{CC} = 9.5 to 28 V		30	100	mV
Load regulation	$\Delta V_{REG}2$	$I_{O} = -5$ to -20 mA		20	100	mV
[Hall Amplifier]		•				
Input bias current	I _{HB}		-4	-1		μA
Common-mode input voltage range	VICM		1.5		V _{REG} -1.5	V
Hall input sensitivity			60			mVp-p
Hysteresis	ΔV_{IN}		8	14	24	mV
Input voltage (low to high)	V _{SLH}			7		mV
Input voltage (high to low)	V _{SHL}			-7		mV
[RC Oscillator]		•				
Output high-level voltage	V _{OH(CR)}		2.4	2.7	3.0	V
Output low-level voltage	V _{OL(CR)}		1.1	1.4	1.7	V
Oscillator frequency	f (CR)	$R = 22 \text{ k}\Omega, C = 4700 \text{ pF}$		19		kHz
Amplitude	V (CR)		1.0	1.25	1.5	Vp-p
[CROCK Oscillator]						
Output high-level voltage	V _{OH(RK)}		2.5	2.8	3.1	V
Output low-level voltage	V _{OL(RK)}		0.5	0.8	1.1	V
Education alternation and	I _{CHG} 1		-10	-8	-6	μA
External capacitor charging current	I _{CHG} 2		6	8	10	μA
Oscillator frequency	f (RK)	C = 0.047 µF		44		Hz
Amplitude	V _(RK)		1.75	1.95	2.25	V
[Current Limiter Operation]						
Limiter	V _{CC} -V _M		0.45	0.5	0.55	V
[Thermal Shutdown Operation]	-					
Thermal shutdown temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis	ΔTSD	Design target value (junction temperature)		40		°C

ParameterSymbolCondutionsmintypmaxUnit[FG Amplifier]-10-10410M2Input diffex voltageVol(FG)Irco = 0.2 mA-10410MAOutput low-level voltageVol(FG)Irco = 0.2 mA0.81.2VGin times 10030.81.2VVFG input sensitivityGain times 10030.81.2WOpen loop gain1 fc() = 2 M24551W86Speed Discriminator]0.91.11VVVOutput low-level voltageVol(F)Ioo = -0.1 mAVscc-0.7IVOutput low-level voltageVol(F)Ioo = -0.1 mAVscc-1.0Vscc-0.7VVOutput low-level voltageVol(F)Ioo = -0.1 mAVscc-1.0Vscc-0.7VVOutput low-level voltageVol(F)Ioo = -0.1 mAVscc-1.2Vscc-1.2VVOutput low-level voltageVol(F)Ioo = -0.1 mAVscc-1.2Vscc-1.2Vscc-1.2VOutput low-level voltageVol(F)Ioo = -0.1 mAVscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2Vscc-1.2			Querta la Quertitiana				
IPG Amplified IPG Amplified IPG Not Notage Vio(PG) IPG	Parameter	Parameter Symbol Conditions		min	typ	max	Unit
Input Disa current Vic(FG) Incl -10 +10 mV Imput Dias current $l_{B(FG)}$ Inco = -0.2 mA VREC-12 VREC-12 <td>[FG Amplifier]</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	[FG Amplifier]						
Input base current Ig(FG) Proce = -0.2 mA V kgen - 1.2 V μA Output low-level voltage VO(HFG) IreG0 = -0.2 mA 0.8 1.2 V FG input sensitivity Gain times 100 3 1.80 2.0 mV Schmitt sensitivity for the next stage Design target value 1.00 1.80 2.20 MV Operating frequency range Design target value 1.00 1.80 2.2 KHz Operating frequency range Image Image 1.00 1.80 2.0 MV Operating frequency range Output tigh-level voltage Vol(D) Ino = -0.1 mA Vgec -1.0 Vgec -0.7 V Output tigh-level voltage Vol(D) Ino = -0.1 mA Vgec -1.8 Vgec -1.5 Vgec -1.2 V Output tigh-level voltage Vol(D) Ino = -0.1 mA Vgec -1.8 Vgec -1.2 V Output tigh-level voltage Vol(D) Igo = 0.1 mA Ima - 0.15 0.5 V Output tigh-level voltage Vol(D) Igo = 0.1 mA Ima - 0.15	Input offset voltage	V _{IO(FG)}		-10		+10	mV
	Input bias current	I _{B(FG)}		-1		+1	μA
	Output high-level voltage	V _{OH(FG)}	I _{FGO} = -0.2 mA	V _{REG} -1.2	V _{REG} -0.8		V
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Output low-level voltage	VOL(FG)	I _{FGO} = 0.2 mA		0.8	1.2	V
Schmitt sensitivity for the next stage Design target value 100 180 250 mV Open loop gain r_{FG} = 2 kHz 45 5 1 dB Speed Discriminator r_{FG} = 2 kHz 45 551 V dB Output Indiversel voltage V _{OL(D)} $l_{D0} = 0.1 mA$ V_ReC-0.7 V V Number of counts 0 512 V V V Output Indiversel voltage V _{OL(D)} $l_{D0} = 0.1 mA$ VREC-0.8 VREc-1.8 VREc-1.2 V Output Indiversel voltage V _{OL(D)} $l_{D0} = 0.1 mA$ 1.2 1.5 1.8 V Clock totarge V _{OL(D)} $l_{D0} = 10 mA$ 0.15 0.5 V Lock trange V $l_{D0} = 0.1 mA$ 0.15 0.5 V Lock trange V _{OL(D0} $l_{D0} = 10 mA$ 0.45 0.4 μ A Output indiversel voltage V _{OL(D1} $l_{D0} = -0.2 mA$ 0.4 0.4 μ A Output indiversel vo	FG input sensitivity		Gain times 100	3			mV
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Schmitt sensitivity for the next stage		Design target value	100	180	250	mV
Open loop gain I I dB [Speed Discriminator]	Operating frequency range					2	kHz
	Open loop gain		f _(FG) = 2 kHz	45	51		dB
	[Speed Discriminator]						
	Output high-level voltage	V _{OH(D)}	I _{DO} = -0.1 mA	V _{REG} -1.0	V _{REG} -0.7		V
Number of counts 512 Image: constraint of counts (PLL Output)	Output low-level voltage	V _{OL(D)}	I _{DO} = 0.1 mA		0.8	1.1	V
	Number of counts	- ()			512		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	[PLL Output]			1			
Output low-level voltage Vol.(P) Iso = 0.1 mA 1.2 1.5 1.8 V Output low-level voltage Vol.(P) Iso = 0.1 mA 0.15 0.5 V Output low-level voltage Vol.(D) It_D = 10 mA 0.15 0.5 V Integrator 6.25 % % % % % Integrator -0.4 4.0.4 µA 0.45 V % Output high-level voltage VOH(NT) INTO = -0.2 mA 0.8 1.2 V Output low-level voltage VOH(NT) INTO = -0.2 mA 0.8 1.2 V Output low-level voltage VOH(NT) INTO = 0.2 mA 0.8 1.2 V Output low-level voltage VOL(NT) INTO = 0.2 mA 0.8 1.2 V Open-loop gain ft (INT) = 1 kHz 45 51 dB Gain-bandwidth product Design target value -5% VReco/2 5% V [Crystal Oscillator] Ooscillardset value -5% VReco/2	Output high-level voltage	V _{OH(P)}	I _{PO} = -0.1 mA	V _{RFG} -1.8	V _{REG} -1.5	V _{REG} -1.2	V
Lock Detector] Volution Iso 0.15 0.5 V Output low-level voltage Volution Iso 0.15 0.5 V Lock range -0.4 6.25 0.8 % [Integrator] -0.4 +0.4 μ A Output high-level voltage Volt(NT) I _{INTO} = -0.2 mA VREG-1.2 VREG-0.8 V Output high-level voltage Volt(NT) I _{INTO} = 0.2 mA 0.8 1.2 V Output low-level voltage Volt(NT) I _{INTO} = 0.2 mA 0.8 1.2 V Open-loop gain f (INT) = 1 KHz 45 51 dB dB Gain-bandwidth product Design target value -5% VREG/2 5% KHz Reference voltage Dosch Vosc = 0.5 mA 1 10 MHz Low-level pin voltage range Vosc = Vosc + 0.3 V 0.5 mA Sitart/Stop Pin] - - 5 V High-level input voltage range V _{IL(SS)} S V V	Output low-level voltage	VOL(P)	$I_{PO} = 0.1 \text{ mA}$	1.2	1.5	1.8	V
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	[Lock Detector]			1			
Lock range Lock range <thlock range<="" th=""> Lock range Lock ra</thlock>	Output low-level voltage		I _{LD} = 10 mA		0.15	0.5	V
$\begin{tabular}{ c $	Lock range				6.25		%
Input bias currentIB(INT)Image of the second	[Integrator]	I	I		1		
Output high-level voltageVORMIT VORMITINTO = -0.2 mAVREG-1.2VREG-0.8VOutput low-level voltageVOL(INT) INTO = 0.2 mAINTO = 0.2 mA0.81.2VOpen-loop gainf (INT) = 1 kHz4551dBGain-bandwidth productDesign target value-5%VREG/25%VReference voltageDesign target value-5%VREG/25%V[Crystal Oscillator]T10MHzDoprating frequency rangefosc0.81.7VHigh-level pin voltageVOSCLIOSC = -0.5 mA1.7VHigh-level pin currentIOSCHVOSC = VOSCL +0.3 V0.5mA[Start/Stop Pin]ISSVREGVVVLow-level input voltage rangeVIL(S/S)VISS = VREG01.5VInput open voltageVIL(S/S)VISS) = VREG-100+10 μA Low-level input voltage rangeVIL(S/S)V(S/S) = VREG-100+10 μA Input open voltageVIL(S/S)V(S/S) = VREG-100+10 μA Low-level input currentII _H (S/S)V(S/S) = VREG-0-280-210 μA Input open voltageVIL(F/R)V(S/S) = VREG01.5VUdupt inpin-level voltageVIL(F/R)V(F/R) = VREG-01.5VOutput high-level voltageVIL(F/R)V(F/R) = VREG-1001.5VUput open voltage<	Input bias current	B(INT)		-0.4		+0.4	uА
Dutput low-level voltageVol.(INT)INTO = 0.2 mANo.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.No.	Output high-level voltage	VOH(INT)	$I_{INTO} = -0.2 \text{ mA}$	V _{REG} -1.2	V _{REG} -0.8		V
Open-loop gainf(INT) = 1 kHz4551dBGain-bandwidth productDesign target value450kHzReference voltageDesign target value-5% $V_{REG}/2$ 5%V[Crystal Oscillator]Operating frequency rangefosc110MHzLow-level pin voltageVoscL $losc = -0.5 \text{ mA}$ 1.7VHigh-level pin current $losc = -0.5 \text{ mA}$ 0.5mA[Start/Stop Pin] $V_{OSC} = V_{OSCL} + 0.3 V$ 0.5MA[Start/Stop Pin] $V_{IL(S/S)}$ 01.5VInput open voltage range $V_{IL(S/S)}$ 01.5VInput open voltage range $V_{IL(S/S)}$ 0.350.500.65VHigh-level input voltage range $V_{IL(S/S)}$ 01.10 μA Input open voltage $V_{IO(S/S)}$ V_{REG} 01.5VInput open voltage $V_{IO(S/S)}$ V_{REG} -100+10 μA [Forward/Reverse Pin] $U_{IL(S/S)}$ $V_{(S/S)} = 0 V$ -280 -210 μA Output high-level voltage $V_{IL(F/R)}$ $V_{(S/S)} = V_{REG}$ 01.5VInput open voltage $V_{IL(F/R)}$ $V_{(F/R)} = V_{REG}$ 0.350.500.65VOutput high-level voltage $V_{IL(F/R)}$ $V_{(F/R)} = V_{REG}$ 01.5VOutput high-level voltage $V_{IL(F/R)}$ $V_{(F/R)} = V_{REG}$ 0.350.500.65VOutput high-le	Output low-level voltage		$I_{\rm INTO} = 0.2 \rm mA$	INEO	0.8	1.2	V
Gain-bandwidth productDesign target value450kHzReference voltageDesign target value-5% $V_{REG}/2$ 5%V[Crystal Oscillator]Operating frequency range f_{OSC} 110MHzLow-level pin voltage V_{OSCL} $l_{OSC} = -0.5 \text{ mA}$ 1.7VHigh-level pin current l_{OSCH} $V_{OSCL} + 0.3 V$ 0.5mA[Start/Stop Pin](Start/Stop Pin]01.5VHigh-level input voltage range $V_{IH(S/S)}$ 01.5VInput open voltage $V_{IL(S/S)}$ 01.5VInput open voltage $V_{IO(S/S)}$ $V_{REG} - 0.5$ V_{REG} VHigh-level input voltage range $V_{IL(S/S)}$ 01.5VInput open voltage $V_{IO(S/S)}$ $V_{REG} - 0.5$ V_{REG} VHigh-level input current $I_{IH(S/S)}$ $V_{(S/S)} = V_{REG}$ -100+10High-level input current $I_{IH(S/S)}$ $V_{(S/S)} = 0 V$ -280-210 μ A[Forward/Reverse Pin]01.5VVUUUOutput high-level voltage $V_{IL(F/R)}$ 01.5VVInput open voltage $V_{IL(F/R)}$ $V_{VREG} - 0.5$ V_{REG} VOutput high-level voltage $V_{IL(F/R)}$ $V_{CF(R)} = V_{REG}$ 01.5VOutput high-level voltage $V_{IL(F/R)}$ $V_{(F/R)} = V_{REG}$ 01.5VOutput high-le	Open-loop gain		f (INT) = 1 kHz	45	51		dB
Reference voltageDesign target value-5% $V_{REG}/2$ 5% V [Crystal Oscillator]Operating frequency rangefosc110MHzLow-level pin voltage V_{OSCL} $l_{OSC} = -0.5 \text{ mA}$ 1.7 V High-level pin current l_{OSCH} $V_{OSC} = V_{OSCL} + 0.3 V$ 0.5mA[Start/Stop Pin] $V_{IH(S/S)}$ 0.5 V_{REG} V High-level input voltage range $V_{IL(S/S)}$ 0 1.5 V Input open voltage $V_{IL(S/S)}$ 0 1.5 V Input open voltage $V_{OS(S)} = V_{REG}$ 0.35 0.50 0.65 High-level input current $I_{IH(S/S)}$ $V_{(S/S)} = V_{REG}$ -10 0 $+10$ Hysteresis ΔV_{IN} 0.35 0.50 0.65 V High-level input current $I_{IL(S/S)}$ $V_{(S/S)} = 0 V$ -280 -210 μA [Forward/Reverse Pin] $U_{IL(F/R)}$ V_{OS} V_{REG} V V_{REG} V Output high-level voltage $V_{IL(F/R)}$ V_{REG} V_{REG} V V_{REG} V Input open voltage $V_{IL(F/R)}$ V_{REG} V_{REG} V V_{REG} V Output high-level voltage $V_{IL(F/R)}$ V_{REG} V_{REG} V V_{REG} V Input open voltage $V_{IL(F/R)}$ V_{REG} V_{REG} V_{IL} V_{IL} Output high-level voltage $V_{IL(F/R)}$ V_{REG} V	Gain-bandwidth product		Design target value		450		kHz
$\begin{array}{ c c c c c c } \hline Crystal Oscillator] \\ \hline Crystal Oscillator] \\ \hline Operating frequency range & f_{OSC} & l_{OSC} = -0.5 \text{ mA} & 1 & 10 & MHz \\ \hline Low-level pin voltage & V_{OSCL} & l_{OSC} = -0.5 \text{ mA} & 1.7 & V \\ \hline High-level pin current & l_{OSCH} & V_{OSC} = V_{OSCL} + 0.3 V & 0.5 & mA \\ \hline Istart/Stop Pin] \\ \hline High-level input voltage range & V_{IH(S/S)} & 3.5 & V_{REG} & V \\ \hline Low-level input voltage range & V_{IL(S/S)} & 0 & 1.5 & V \\ Input open voltage & V_{IO(S/S)} & V_{REG} - 0.5 & V_{REG} & V \\ \hline Hysteresis & \Delta V_{IN} & 0.35 & 0.50 & 0.65 & V \\ \hline High-level input current & I_{IH(S/S)} & V_{(S/S)} = V_{REG} & -10 & 0 & +10 & \muA \\ \hline Low-level input current & I_{IL(S/S)} & V_{(S/S)} = 0 & -280 & -210 & \muA \\ \hline Forward/Reverse Pin] & & & & & \\ \hline Output high-level voltage & V_{IL(F/R)} & 0 & 1.5 & V \\ \hline Input open voltage & V_{IL(F/R)} & 0 & 1.5 & V \\ \hline Input open voltage & V_{IL(F/R)} & 0 & 1.5 & V \\ \hline Output low-level voltage & V_{IL(F/R)} & V_{REG} - 0.5 & V_{REG} & V \\ \hline Output high-level voltage & V_{IL(F/R)} & 0 & 1.5 & V \\ \hline Input open voltage & V_{IL(F/R)} & 0 & 0 & 1.5 & V \\ \hline Input open voltage & V_{IL(F/R)} & 0 & 0 & 1.5 & V \\ \hline Output high-level voltage & V_{IL(F/R)} & 0 & 0 & 0 & 1.5 & V \\ \hline Output high-level voltage & V_{IL(F/R)} & V_{REG} - 0.5 & V_{REG} & V \\ \hline Output high-level voltage & V_{IL(F/R)} & 0 & 0 & 1.5 & V \\ \hline Input open voltage & V_{IL(F/R)} & V_{REG} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & $	Reference voltage		Design target value	-5%	V _{REG} /2	5%	V
Operating frequency range f_{OSC} 110MHzLow-level pin voltage V_{OSCL} $l_{OSC} = -0.5 \text{ mA}$ 1.7VHigh-level pin current l_{OSCH} $V_{OSC} = V_{OSCL} + 0.3 \text{ V}$ 0.5mA[Start/Stop Pin]3.5 V_{REG} VHigh-level input voltage range $V_{IL(S/S)}$ 01.5VLow-level input voltage range $V_{IL(S/S)}$ 01.5VInput open voltage $V_{IO(S/S)}$ $V_{REG} - 0.5$ V_{REG} VHysteresis ΔV_{IN} 0.350.500.65VHigh-level input current $I_{IL(S/S)}$ $V_{(S/S)} = V_{REG}$ -100+10Low-level input current $I_{IL(S/S)}$ $V_{(S/S)} = 0 \text{ V}$ -280-210 μA [Forward/Reverse Pin] $V_{IL(F/R)}$ $V_{IL(F/R)}$ 01.5VOutput high-level voltage $V_{IL(F/R)}$ $V_{REG} - 0.5$ V_{REG} VInput open voltage $V_{IL(F/R)}$ $V_{CF/R} = V_{REG}$ 01.5VOutput high-level voltage $V_{IL(F/R)}$ $V_{REG} - 0.5$ V_{REG} VOutput high-level voltage $V_{IL(F/R)}$ $V_{REG} - 0.5$ V_{REG} VInput open voltage $V_{ID(F/R)}$ $V_{REG} - 0.5$ V_{REG} VOutput high-level voltage $V_{IL(F/R)}$ $V_{REG} - 0.5$ V_{REG} VOutput high-level voltage $V_{IL(F/R)}$ $V_{REG} - 0.5$ V_{REG} VOutput high-level	[Crystal Oscillator]			1			
Low-level pin voltage V_{OSCL} $I_{OSC} = -0.5 \text{ mA}$ 1.7VHigh-level pin current I_{OSCH} $V_{OSC} = V_{OSCL} + 0.3 \text{ V}$ 0.5mA[Start/Stop Pin]3.5 V_{REG} VHigh-level input voltage range $V_{IL(S/S)}$ 01.5VLow-level input voltage range $V_{IL(S/S)}$ 01.5VInput open voltage $V_{IL(S/S)}$ 001.5VHysteresis ΔV_{IN} 0.350.500.65VHigh-level input current $I_{IH(S/S)}$ $V_{(S/S)} = V_{REG}$ -100+10Low-level input current $I_{IL(S/S)}$ $V_{(S/S)} = 0 V$ -280-210 μA [Forward/Reverse Pin]01.5VVOutput high-level voltage $V_{IL(F/R)}$ 01.5VInput open voltage $V_{IL(F/R)}$ 01.5VOutput high-level voltage $V_{IL(F/R)}$ 01.5VOutput high-level voltage $V_{IL(F/R)}$ 01.5VInput open voltage $V_{IL(F/R)}$ 01.5VInput open voltage $V_{IL(F/R)}$ 0.350.500.65VOutput high-level voltage $V_{IL(F/R)}$ 01.5VInput open voltage $V_{IL(F/R)}$ 001.5VOutput high-level voltage $V_{IL(F/R)}$ $V_{F/R} = V_{REG}$ 0.1004.10Output high-level voltage $I_{IH(F/R)}$ $V_{(F/R)} = V$	Operating frequency range	fosc		1		10	MHz
High-level pin currentI OSCH $V_{OSC} = V_{OSCL} + 0.3 V$ 0.5mA[Start/Stop Pin]	Low-level pin voltage	Vosci	$I_{OSC} = -0.5 \text{ mA}$		1.7		V
[Start/Stop Pin]Source of the second of the se	High-level pin current	I _{OSCH}	$V_{OSC} = V_{OSCI} + 0.3 V$		0.5		mA
High-level input voltage range $V_{IH(S/S)}$ 3.5 V_{REG} V Low-level input voltage range $V_{IL(S/S)}$ 01.5 V Input open voltage $V_{IO(S/S)}$ V_{REG} V V_{REG} V Hysteresis ΔV_{IN} 0.350.500.65 V High-level input current $I_{IH(S/S)}$ $V_{(S/S)} = V_{REG}$ -100+10 μA Low-level input current $I_{IL(S/S)}$ $V_{(S/S)} = 0$ -280-210 μA [Forward/Reverse Pin]01.5 V V Output high-level voltage $V_{IL(F/R)}$ 01.5 V Input open voltage $V_{IL(F/R)}$ 01.5 V Output low-level voltage $V_{IL(F/R)}$ V_{REG} 001.5Output low-level voltage $V_{IL(F/R)}$ $V_{C/R} = V_{REG}$ V_{REG} V Input open voltage $V_{IL(F/R)}$ $V_{C/R} = V_{REG}$ V_{REG} V Output high-level voltage $V_{IL(F/R)}$ $V_{C/R} = V_{REG}$ V_{REG} V Output high-level voltage $V_{IL(F/R)}$ $V_{C/R} = V_{REG}$ V_{REG} V Output high-level voltage $V_{IO(F/R)}$ $V_{C/R} = V_{REG}$ V_{IO} V_{IO} V_{IO}	[Start/Stop Pin]						
Low-level input voltage range $V_{IL(S/S)}$ 01.5VInput open voltage $V_{I0(S/S)}$ V_{REG} V_{REG} VHysteresis ΔV_{IN} 0.350.500.65VHigh-level input current $I_{IL(S/S)}$ $V_{(S/S)} = V_{REG}$ -100+10 μA Low-level input current $I_{IL(S/S)}$ $V_{(S/S)} = V_{REG}$ -100+10 μA Low-level input current $I_{IL(S/S)}$ $V_{(S/S)} = 0 V$ -280-210 μA [Forward/Reverse Pin] $V_{IH(F/R)}$ 0 1.5 V Output high-level voltage $V_{IL(F/R)}$ 01.5 V Input open voltage $V_{IL(F/R)}$ 0.35 0.50 0.65 V Output low-level voltage $V_{IL(F/R)}$ V_{REG} 0 1.5 V Input open voltage $V_{IO(F/R)}$ $V_{CF(R)} = V_{REG}$ 0.35 0.50 0.65 V Hysteresis ΔV_{IN} 0.35 0.50 0.65 V Output high-level voltage $I_{IH(F/R)}$ $V(F/R) = V_{REG}$ -10 0 $+10$ μA	High-level input voltage range	VIH(S/S)		3.5		V _{REG}	V
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Low-level input voltage range	V _{IL(S/S)}		0		1.5	V
Hysteresis ΔV_{IN} 0.350.500.65VHigh-level input current $I_{IH}(S)S$ $V_{(S/S)} = V_{REG}$ -100+10 μA Low-level input current $I_{IL}(S)S$ $V_{(S/S)} = 0 V$ -280-210 μA [Forward/Reverse Pin]0UIH(F/R)3.5 V_{REG} VOutput high-level voltage $V_{IH(F/R)}$ 01.5VInput open voltage $V_{IL(F/R)}$ 01.5VHysteresis ΔV_{IN} 0.350.500.65VOutput high-level voltage $V_{IO(F/R)}$ V0.350.500.65VInput open voltage $V_{IO(F/R)}$ $V_{F/R} = V_{REG}$ 01.15VVOutput high-level voltage $V_{IO(F/R)}$ $V_{C/R} = V_{REG}$ 0.350.500.65VOutput high-level voltage $V_{II}(F/R)$ $V_{VF/R} = V_{REG}$ -100+10 μA	Input open voltage	V _{IO(S/S)}		V _{REG} -0.5		V _{REG}	V
High-level input currentIIV(S/S) = VREG-100+10 μ ALow-level input currentIIV(S/S) = 0 V-280-210 μ A[Forward/Reverse Pin]Output high-level voltageVIH(F/R)3.5VREGVOutput low-level voltageVIL(F/R)01.5VInput open voltageVIO(F/R)VREG-0.5VREGVHysteresis Δ VIN0.350.500.65VOutput high-level voltageIIV(F/R) = VREG-100+10 μ A	Hysteresis	ΔV _{IN}		0.35	0.50	0.65	V
Low-level input currentIIL(S/S)V(S/S) = 0 V-280-210 μ A[Forward/Reverse Pin]Output high-level voltageVIH(F/R)3.5VREGVOutput low-level voltageVIL(F/R)01.5VInput open voltageVIO(F/R)VREGVREGVHysteresis ΔV_{IN} 0.350.500.65VOutput high-level voltageIIH(F/R)V(F/R) = VREG-100+10 μ A	High-level input current	I _{IH(S/S)}	$V_{(S/S)} = V_{REG}$	-10	0	+10	μA
$\begin{tabular}{ c c c c c c } \hline \hline [Forward/Reverse Pin] & \hline & $	Low-level input current	I _{IL(S/S)}	$V_{(S/S)} = 0 V$	-280	-210		μA
	[Forward/Reverse Pin]	(0, 0)					
	Output high-level voltage	V _{IH(F/R)}		3.5		V _{REG}	V
Input open voltage $V_{IO(F/R)}$ V_{REG} V_{REG} V_{REG} V_{REG} Hysteresis ΔV_{IN} 0.350.500.65 V Output high-level voltage $I_{IH(F/R)}$ $V_{(F/R)} = V_{REG}$ -100+10 μA	Output low-level voltage	V _{II (F/R)}		0		1.5	V
Hysteresis ΔV_{IN} $\Lambda C = V_{REG}$ $\Lambda L = V_{REG}$ Output high-level voltage $I_{IH}(F/R)$ $V(F/R) = V_{REG}$ -10 0 $+10$ μA	Input open voltage	VIO(F/R)		V _{REG} -0.5		VRFG	V
Output high-level voltage $I_{IH(F/R)}$ $V_{(F/R)} = V_{REG}$ -10 0 $+10$ μA	Hysteresis	ΔVIN		0.35	0.50	0.65	V
	Output high-level voltage	IIH(F/R)	$V_{(F/R)} = V_{REG}$	-10	0	+10	μA
Output low-level voltage $ I_{ L(F/R)} V_{(F/R)} = 0 V$ $ -280 -210 $ μA	Output low-level voltage	I _{IL(F/R)}	V _(F/R) = 0 V	-280	-210		μΑ



Pin Assignment



Truth Table

	Source	F/R = L		F / R = H		Н	
	Sink	IN 1	IN2	IN 3	IN 1	IN 2	IN 3
1	$OUT2 \rightarrow OUT1$	Н	L	Н	L	Н	L
2	$\text{OUT3} \rightarrow \text{OUT1}$	н	L	L	L	Н	н
3	$OUT3 \rightarrow OUT2$	н	н	L	L	L	н
4	$OUT1 \rightarrow OUT2$	L	н	L	Н	L	н
5	$OUT1 \rightarrow OUT3$	L	н	н	Н	L	L
6	$OUT2 \rightarrow OUT3$	L	L	н	н	н	L

Equivalent Circuit Block Diagram



Functional Description

1. Speed control circuit

This IC uses a speed discriminator circuit and a PLL circuit in combination for speed control. The speed control circuit outputs an error signal once every two FG periods (a charge pump technique). The PLL circuit outputs a phase error signal once every FG period (also a charge pump technique). As compared with the earlier speed control technique of using only a speed discriminator, the combined speed discriminator/PLL circuit technique is better able to suppress speed fluctuations when used with motors with large load variations. The FG servo frequency is determined by the following equation, which means that the motor speed is determined by the number of FG pulses and the crystal oscillator frequency.

 $f_{FG}(servo) = f_{OSC}/8192$

f_{OSC}: Crystal oscillator frequency

2. Output drive circuit

This IC adopts a direct PWM drive technique to minimize the power loss in the output. The output transistor is always saturated when on, and the motor drive power is adjusted by varying the duty with which the output is on. Since the lower side output transistor is used for output switching, a Schottky diode or similar device must be connected between OUT and V_{CC} . (This is because a through current will flow at the instant the lower side transistor turns on unless a diode with a short reverse recovery time is used.) The diode between OUT and ground is included on chip in this device. If this becomes a problem for large output currents, (e.g. if the output waveform is disturbed during lower side kickback) attach an external rectifying (or Schottky) diode.

3. Current limiter

The current limiter circuit limits the output to a current determined by the equation $I = V_{RF}/R_f$, where $V_{RF} = 0.5$ V (typical) and R_f is the current detection resistor. The current limiting operation consists of reducing the output on duty to lower the current.

4. Reference clock

Either of the two following input methods can be used for the speed control clock

• Using a crystal oscillator element

 When using a crystal oscillator element, connect the crystal, capacitors, and resistors as shown in the figure below to form an oscillator circuit.



Sample External Circuit Constants (Reference values)

Oscillator frequency (MHz)	C1 (µF)	C2 (µF)	C3 (µF)	R1 (Ω)	R2 (Ω)
1 to 3	0.1	47	220	220 K	
3 to 5	0.1	18	100	100 K	_
5 to 7	0.1		47	47 K	
7 to 10	0.1		22	10 K	17K
7 10 10	0.1	_	33	IUK	4./ K

V_{REG}

C1, R1: Oscillator stabilization

C3: Oscillator coupling

C2: Overtone prevention R2: Oscillator operating ma

2: Oscillator operating margin improvement

This circuit and these circuit constant values are provided for reference only. Always verify application circuits with the supplier of the oscillator element to assure that the effects of the characteristics of the oscillator element itself, the printed circuit board wiring, floating capacitances, and other aspects are accounted for appropriately. (Notes on printed circuit board lines)

Floating capacitances on the printed circuit board can easily affect crystal oscillator circuits, since these are highspeed circuits. The printed circuit board lines connecting these components should be kept as short and as narrow as possible and other measures to reduce floating capacitances should be considered as well.

In this external circuit, the line between the oscillator element and C3 (C2) is particularly subject to floating capacitance problems and requires special care.

- External clock (A frequency equivalent to the crystal oscillator frequency: 1 to 10 MHz)
 - If a frequency equivalent to a crystal oscillator frequency is input from an external source, input that signal through a series resistor of about 13 k Ω to the XI pin. The XO pin should be left open.

Input signal levels:

Low-level voltage: 0 to 0.8 V

High-level voltage: 2.5 to 5.0 V

5. Speed lock range

The speed lock range is $\pm 6.25\%$ of the set speed. When the motor speed is in the lock range the LD pin will go low (open collector output). The IC controls the motor speed by changing the motor drive output on duty according to the speed error signal if the motor speed goes outside the lock range.

6. PWM frequency

The PWM frequency is determined by the capacitor and resistor connected to the CR pin.

 $f_{PWM} \approx 1/(0.5 \times C \times R)$

A PWM frequency in the range 15 to 25 kHz is desirable. If the PWM frequency is too low, the motor may resonate at the PWM frequency when locked resulting in noise, since that frequency will be in the audible range. If the PWM frequency is too high, the switching loss in the output transistor will increase. The value of the resistor must be over 5 k Ω .

7. Hall input signals

The signals input as the Hall inputs must have amplitudes that exceed the hysteresis, which has a maximum value of 24 mV. Considering noise, inputs with amplitudes of at least 100 mV are desirable. Attach a noise rejection capacitor (around 0.001 to 0.01 μ F) across the IN3 Hall input (pins 26 and 27). Since these pins are adjacent to the OUT1 output pin, noise in this input may cause disturbances in the output waveforms.

8. F/R switching

The F/R pin can be used to change the direction of motor rotation. However the following points must be observed when designing applications that will change the motor direction while the motor is turning.

• Application circuit must be designed to handle the through current that occurs when the direction is switched. However, increases in the V_{CC} voltage during switching due to motor current flowing into the power supply system instantaneously, must not exceed the rated voltage (30 V) of the device. Increase the value of the capacitor between power supply and ground if this is a problem.

• If the motor current after switching exceeds the current limiter upper limit, the lower side transistor will be turned off. However, the high side transistor will go to the short braking state, and a current determined by the motor reverse voltage and the coil resistance will flow in this transistor. Applications must be designed so that this current does not exceed the rated current, 3.1 A. In general, switching the direction with the F/R pin at high motor speeds is dangerous.

9. Lock protection circuit

This IC includes a built-in lock protection circuit to protect the IC and the motor when the motor is locked. In the start state, if the LD output remains high for a fixed period (the unlocked state), the lower side transistor is turned off. The capacitance of the capacitor connected to the CROCK pin sets this time. A time of a few seconds can be set with a capacitance under $0.1 \, \mu F$.

Set time (seconds) $\approx 52 \times C (\mu F)$

To release the lock protection state, the IC must be set to the stopped state or the power must be turned off and reapplied. The CROCK pin must be connected to ground if the lock protection circuit is not used.

10. Power supply stabilization

The large currents drawn by this IC can adversely affect the power supply voltage. Therefore a capacitor with a sufficiently large value must be inserted between the V_{CC} pin and ground. If a diode is inserted in the power supply line to protect against destruction due to accidentally connecting the power supply with the polarity reversed, the power supply line voltage will be even more easily affected and an even larger capacitor will be required.

Pin Functions

Pin No.	Pin	Pin function	Equivalent circuit
28	OUT1	Motor drive outputs	
1	OUT2	Connect Schottky diodes between these outputs and V_{CC} .	Vee
2	GND2	Output block groupd	<u>VCC</u> , 2000 VM
5	GNDZ	Output block ground	
5	VМ	Connect a resistor (R_f) with a small resistance between this	
		pin and V _{CC} .	
		The output current is limited to a current set according to the equation loss $= \sqrt{2\pi c/R}$	
			A07263
		Devery every her (the short the sector (the sector)	
4	V _{CC}	Power supply (blocks other than the output block)	
Ö	VREG	Insert a capacitor (about 0.1 µF) between this pin and ground	Vcc
		for regulation.	⊢ ₹
			(6)
			╵╹┓┛╹ ↓ · ♠
			A07264
7	F/R	Forward/reverse control	
		Low: 0 to 1.5 V	VREG
		The open state functions as a high-level input.	
		Has a hysteresis of about 0.5 V.	Ψ
		High or open: Reverse	
			4kΩ
			/// /// /// /// A07265
8	S/S	Start/stop control	
		High: 3.5 to V _{REG}	VREG
		The open state functions as a high-level input.	
		Low: Start	
		High or open: Stop	μ 20κΩ
			h h h h h h h A07266

Pin No.	Pin	Pin function	Equivalent circuit
9 10	XO XI	Crystal oscillator connection. The reference clock signal is generated by connecting a crystal oscillator element to these pins. If an external clock (with a frequency of a few MHz) is used, connect that signal to the XI pin through a series resistor of about 13 k Ω , and leave the XO pin open.	VREG VREG VREG V VREG V V V V V V V V V V V V V V V V V V V
11	INT _{OUT}	Integrator amplifier output (speed control output)	VREG
12	INT _{IN}	Integrator amplifier input	VREG
13	Pout	PLL circuit output	VREG (13) MOT270

Pin No.	Pin	Pin function	Equivalent circuit
14	D _{OUT}	Speed discriminator output. High: Acceleration Low: Deceleration	
			лл лл дот271
15	LD	Speed lock detection output Outputs a low level when the motor speed is in the lock range (±6.25%).	VREG (15) A07272
16	FG _{OUT}	FG amplifier output	VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG
17	FG _{IN} -	FG amplifier input	V _{REG} FG reset circuit (200 Ω) $(200 Ω)$
		The logic block initial reset is applied by connecting a capacitor (of about 0.1 µF) between FG _{IN+} and ground.	
19	CROCK	Setting for the lock protection circuit operating time. An operating time of about 2.5 seconds can be set by connecting a capacitor of about 0.047 μF between the CROCK pin and ground.	VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG VREG

Pin No.	Pin	Pin function	Equivalent circuit
20	CR	PWM oscillator frequency setting. Connect a resistor (R) between this pin and V _{REG} and a capacitor (C) between this pin and ground. Values of R = 22 k Ω , and C = 4700 pF set a frequency of about 19 kHz.	VREG
21	GND1	Ground (blocks other than the output block)	
22 23 24 25 26 27	IN1+ IN1- IN2+ IN3+ IN3-	Hall inputs An input with $IN^* > IN^-$ is taken to be a high level, and the opposite state is taken to be a low level. Hall signals with amplitudes greater that 100 mVp-p (differential) are desirable. If noise on the Hall signals is a problem, connect capacitors between the IN ⁺ and IN ⁻ pins.	VREG (23) (25) (27) + 200Ω (23) (25) (27) + (22) (24) (26) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓ (27) ↓

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