

## NMOS 4-BIT MICROCONTROLLER

## TMP4240P, TMP4260P

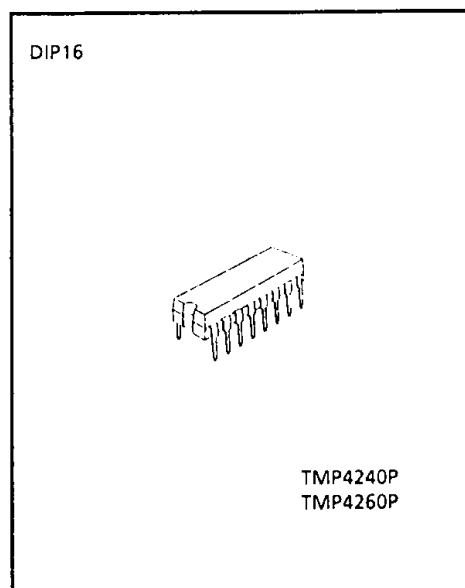
The 4240/60 are compact and high speed 4-bit single chip microcomputers integrating ROM, RAM, input/output ports, and interval timer. The 4240/60 are the standard type devices in the TLCS-42 NMOS series, and provide high current output capability for LED direct drive.

The 4240/60 are suitable for control of home appliances (such as fans, air-conditioners, refrigerators), audio equipments, games, and toys.

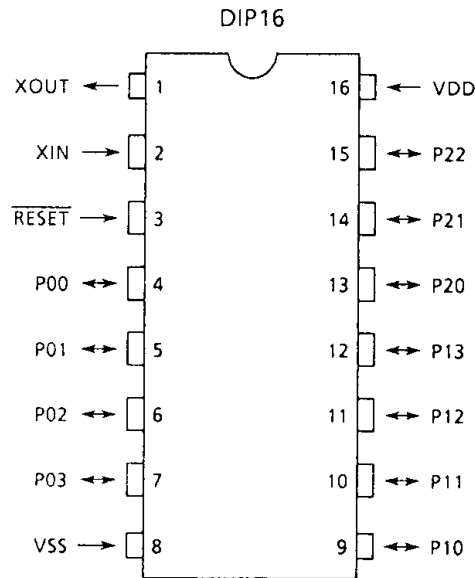
PART No.	ROM	RAM	PACKAGE	PIGGYBACK BOARD
TMP4240P	512 × 8-bit	32 × 4-bit	DIP16	BM4211B
TMP4260P	1024 × 8-bit			

## FEATURES

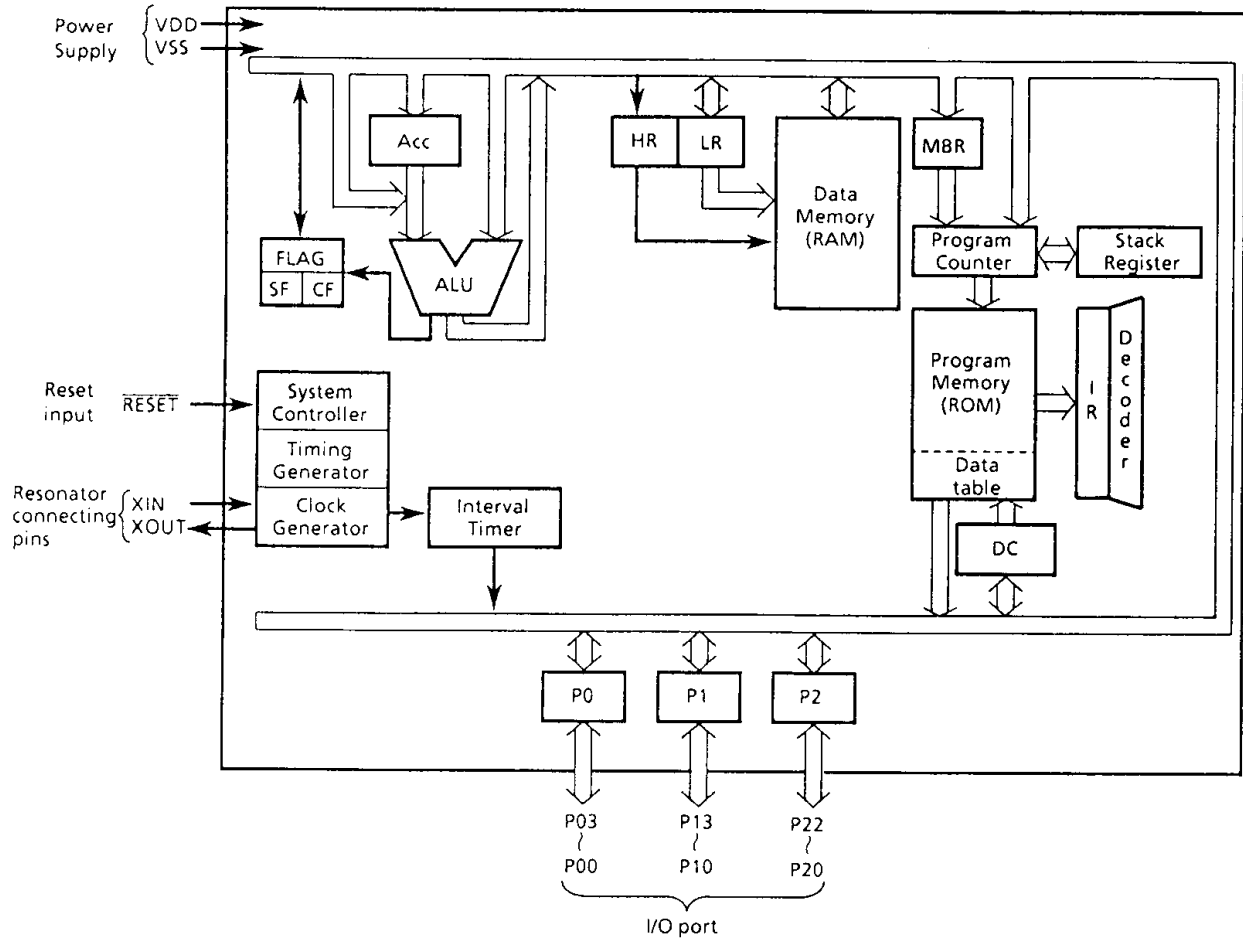
- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time : 2.5 $\mu$ s (at 2MHz)
- ◆ 42 basic instructions
  - All instructions are one byte object code
  - Table look-up instructions
- ◆ Stack for subroutine call : 1 level
- ◆ I/O port (11 pins)
  - I/O 3ports 11pins
- ◆ 11-stage Interval Timer (4260 only)
- ◆ High current outputs  
LED direct drive is available.
- ◆ Real Time Emulator : BM4221A



PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



## PIN FUNCTION

PIN NAME	INPUT/OUTPUT	FUNCTION
P03 - P00	I/O	4-bit programmable I/O ports with latch.
P13 - P10		When used as input port, the latch must be set to "1".
P22 - P20		3-bit programmable I/O port with latch. When used as input port, the latch must be set to "1".
XIN	INPUT	Resonator connecting pins.
XOUT	OUTPUT	For inputting external clock, XIN is used and XOUT is opened.
RESET	INPUT	Reset signal input
VDD	Power Supply	+ 5V
VSS		0V (GND)

## OPERATIONAL DESCRIPTION

The 4240/60 are standard devices in the TLC5-42 NMOS series and, except for the fact that they do not have hold functions and port registers, operate the same as the 42C40/60, standard devices in the TLC5-42 CMOS series. Refer to the 42C40/60 technical data sheets for details. Also, the 4240 does not have an interval timer.

## 1. PERIPHERAL HARDWARE FUNCTION

## 1.1 I/O Ports

The 4240/60 have 3 I/O ports (11 pins) each as follows :

- ① P0, P1 ; 4-bit input/output
- ② P2 ; 3-bit input/output

All of the ports have output latches, so output data are held by the latches. There is no input latch, so external input data are either held externally until read, or are read several times before processing, when necessary.

- (1) Ports P0 (P03 - P00), P1 (P13 - P10), P2 (P22 - P20)

These are input/output ports with latch. Ports P0 and P1 have 4 bits each, and P2 has 3 bits. When used as input ports, the latch should be set to "1".

Pull-up resistor can be specified for each bit by mask options.

In addition, the 4240 does not have an interval timer ; therefore, interval timer output (ITS) is permanently set to "1". Because of that, "1" is read to the MSB is executed.

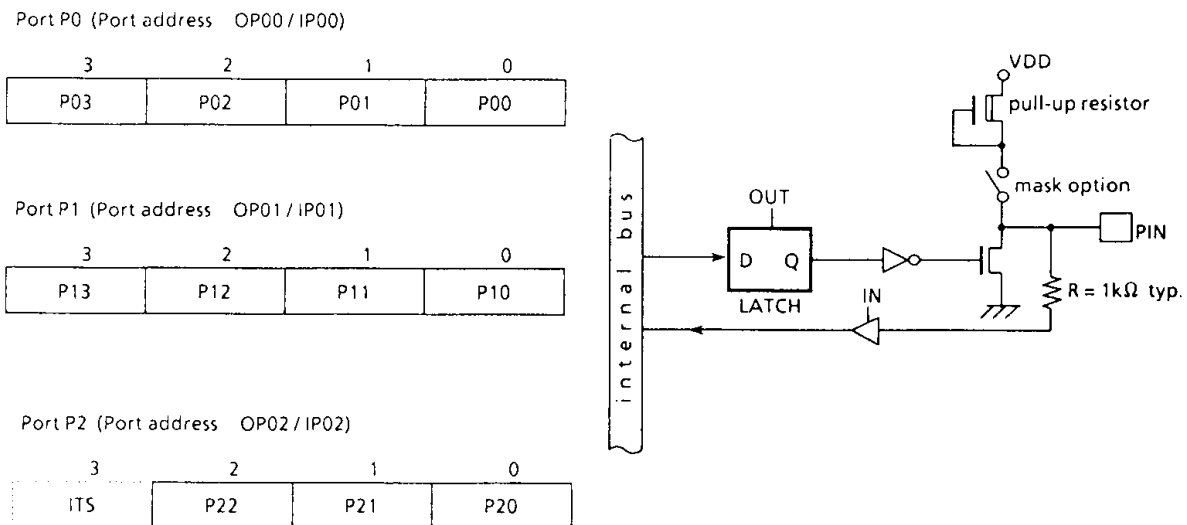


Figure 1-1. Ports P1, P2 and P2

## ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V<sub>SS</sub> = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V <sub>DD</sub>		- 0.5 to 7	V
Input Voltage	V <sub>IN</sub>		- 0.5 to 7	V
Output Voltage	V <sub>OUT1</sub>	Except sink open drain pin	- 0.5 to 7	V
	V <sub>OUT2</sub>	Sink open drain pin	- 0.5 to 15	
Output Current (total)	ΣI <sub>OUT</sub>		30	mA
Power Dissipation [T <sub>opr</sub> = 85°C]	PD		300	mW
Soldering Temperature (time)	T <sub>slid</sub>		260 (10sec)	°C
Storage Temperature	T <sub>stg</sub>		- 55 to 125	°C
Operating Temperature	T <sub>opr</sub>		- 40 to 85	°C

RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub> = 0V, T<sub>opr</sub> = - 40 to 85°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V <sub>DD</sub>			4.5	5.5	V
Input High Voltage	V <sub>IH1</sub>	Except RESET		2.2	V <sub>DD</sub>	V
	V <sub>IH2</sub>	RESET pin		3.0		
Input Low Voltage	V <sub>IL1</sub>	Except RESET pin		0	0.8	V
	V <sub>IL2</sub>	RESET pin			0.6	
Clock Frequency	f <sub>c</sub>			0.2	2.0	MHz

**D.C. CHARACTERISTICS** ( $V_{SS} = 0V, T_{opr} = -40 \text{ to } 85^{\circ}C$ )

PARAMETER	SYMBOL	PIN	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	$V_{HS}$	$\overline{RESET}$		—	0.3	—	V
Input Current	$I_{IN}$	Open drain pin	$V_{DD} = 5.5V, V_{IN} = 0.4V$	—	$-10 \sim -5$	-2.0	$\mu A$
Low Level Input Current	$I_{IL1}$	$\overline{RESET}$	$V_{DD} = 5.5V, V_{IN} = 0.6V$	—	-50	-100	$\mu A$
	$I_{IN2}$	Pin with pull-up resistor		—	—	-360	
Output Leakage Current	$I_{LO}$	Open drain pin	$V_{DD} = 5.5V, V_{OUT} = 5.5V$	—	$10 \sim 5$	2.0	$\mu A$
Output Level High Voltage	$V_{OH}$	Pin with pull-up resistor	$V_{DD} = 5V, I_{OH} = -5\mu A$	4.7	4.9	—	V
Output Level High Current	$I_{OH}$		$V_{DD} = 4.5V, V_{OH} = 2.4V$	-50	—	—	$\mu A$
Low Level Output Current	$I_{OL1}$	Ports P0, P1, P2	$V_{DD} = 4.5V, V_{OL} = 0.4V$	1.6	10.0	—	mA
	$I_{OL2}$		$V_{DD} = 4.5V, V_{OL} = 1.2V$	10	25	—	
Supply Current	$I_{DD}$		$V_{DD} = 5.5V$	—	13	28	mA

Note 1. Typ. values shows those at  $V_{DD} = 5V, T_{opr} = 25^{\circ}C$

Note 2. Supply Current :  $\overline{RESET}$  pin is 0V, and XOUT pin and ports are opened in the external clock operation.

**A.C. CHARACTERISTICS** ( $V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 5.5V, T_{opr} = -40 \text{ to } 85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITIONS		Min.	Typ.	Max.	UNIT
Instruction Cycle Time	$t_{cy}$			2.5	—	25	$\mu s$
High level Clock pulse Width	$t_{WCH}$	$V_{IN} = V_{IH}$	For external clock operation	100	—	—	ns
Low level Clock pulse Width	$t_{WCL}$	$V_{IN} = V_{IL}$					

**RECOMMENDED OSCILLATING CONDITIONS** ( $V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 5.5V, T_{opr} = -40 \text{ to } 85^{\circ}C$ )

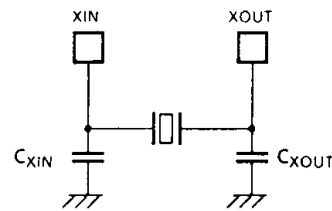
Ceramic Resonator

2MHz

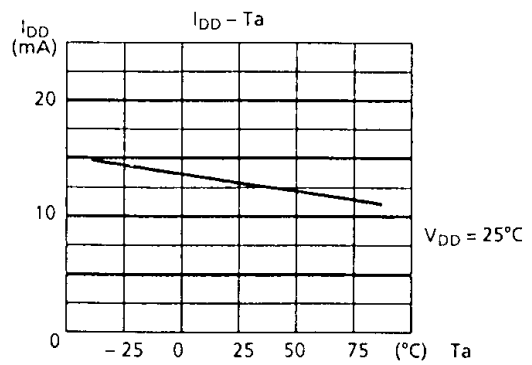
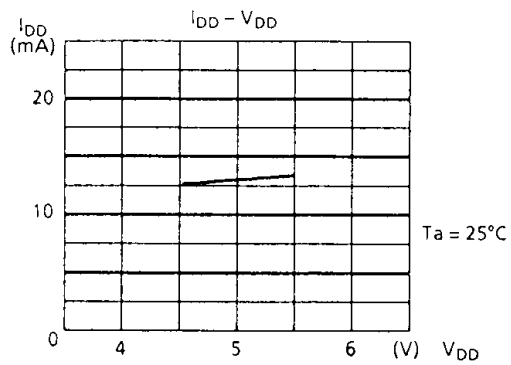
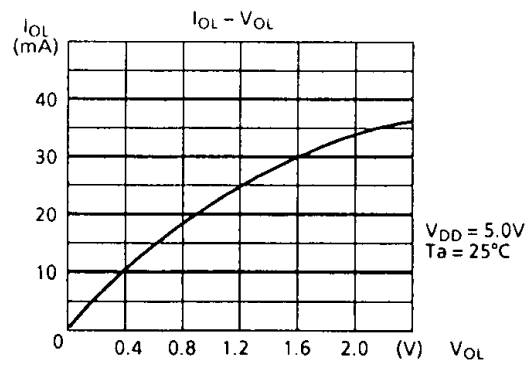
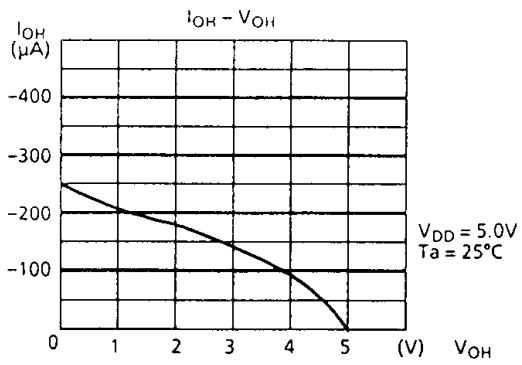
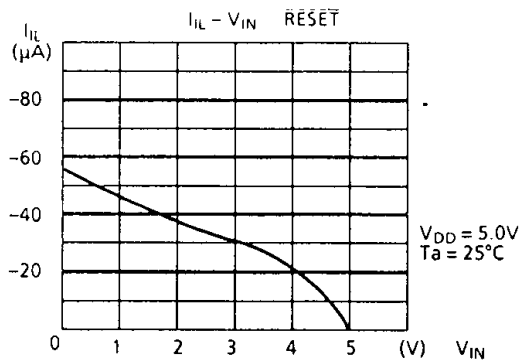
CSA2.00MG (MURATA)  $C_{XIN} = C_{XOUT} = 50pF$

400KHz

CSB400B (MURATA)  $C_{XIN} = C_{XOUT} = 220pF$



TYPICAL CHARACTERISTICS



INPUT/OUTPUT CIRCUITRY

(1) Control pins

Input/Output circuitries of the 42C40/60 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	INPUT OUTPUT		Resonator connecting pins $R = 1K\Omega$ (typ.) $R_f = 1M\Omega$ (typ.) $R_o = 0.5K\Omega$ (typ.)
$\overline{\text{RESET}}$	INPUT		Hysteresis input Pull-up resistor $R_{IN} = 90K\Omega$ (typ.) $R = 1K\Omega$ (typ.)

(2) I/O ports

Input/Output circuitries of the 42C40/60 I/O ports are shown below. Pull-up resistor can be specified for each bit by mask option.

PORT	I/O	CIRCUITRY	INITIAL STATE	REMARKS
P0 P1 P2	I/O	Option : open drain output 	Hi-Z (INPUT)	Sink open drain output $R = 1K\Omega$ (typ.)
		Option : open drain output with pull-up 	High (INPUT)	Pull-up resistor $R_L = 20K\Omega$ (typ.) $R = 1K\Omega$ (typ.)