

# KT3170

# LOW POWER DTMF RECEIVER

## INTRODUCTION

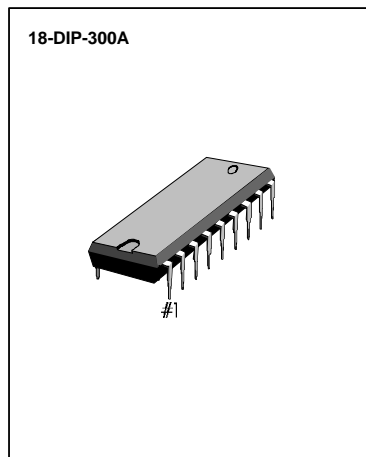
The KT3170 is a complete Dual Tone Multiple Frequency (DTMF) receiver that is fabricated by low power CMOS and the Switched-Capacitor Filter technology. This LSI consists of band split filters, which separates counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus. It decodes all 16 DTMF tone pairs into a 4bits digital code. The externally required components are minimized by on chip provision of a differential input AMP, clock oscillator and latched three state interface. The on chip clock generator requires only a low cost TV crystal as an external component.

## FEATURES

- Detects all 16 standard tones.
- Low power consumption : 15mW (Typ)
- Single power supply : 5V
- Uses inexpensive 3.58MHz crystal
- Three state outputs for microprocessor interface
- Good quality and performance for using in exchange system
- Power down mode/input inhibit

## APPLICATIONS

- PABX
- Central Office
- Paging Systems
- Remote Control
- Credit Card Systems
- Key Phone System
- Answering Phone
- Home Automation System
- Mobile Radio
- Remote Data Entry



## ORDERING INFORMATION

Device	Package	Operating
KT3170N	18-DIP-300A	- 25°C ~ + 75°C

## PIN CONFIGURATION

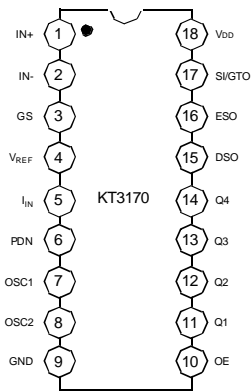


Fig. 1



## PIN DESCRIPTION

Pin No	Symbol	Description
1	IN +	Non inverting input of the op amp.
2	IN -	Inverting input of the op amp.
3	GS	Gain Select. The output used for gain adjustment of analog input signal with a feedback resistor.
4	V <sub>REF</sub>	Reference Voltage output (V <sub>DD</sub> /2, Typ) can be used to bias the op amp input of V <sub>DD</sub> /2.
5	I <sub>IN</sub>	Input inhibit. High input states inhibits the detection of tones. This pin is pulled down internally.
6	PDN	Control input for the stand-by power down mode. Power down occurs when the signal on this input is in high states. This pin is pulled down internally.
7, 8	OSC1 OSC2	Clock input/output. A inexpensive 3.579545MHz crystal connected between these pins completes internal oscillator. Also, external clock can be used.
9	GND	Ground pin.
10	OE	Output Enable input. Outputs Q1-Q4 are CMOS push pull when OE is High and open circuited (High impedance) when disabled by pulling OE low. Internal pull up resistor built in.
11 - 14	Q1 - Q4	Three state data output. When enabled by OE, these digital outputs provide the hexadecimal code corresponding to the last valid tone pair received.
15	DSO	Delayed Steering Output. Indicates that valid frequencies have been present for the required guard time, thus constituting a valid signal. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on SI/GTO falls below V <sub>TH</sub> .
16	ESO	Early Steering Outputs. Indicates detection of valid tone output a logic high immediately when the digital algorithm detects a recognizable tone pair. Any momentary loss of signal condition will cause ESO to return to low.
17	SI/GTO	Steering Input/Guard Time Output. A voltage greater the V <sub>TS</sub> detected at SI causes the device to register the detected tone pair and update the output latch. A voltage less than V <sub>TS</sub> frees the device to accept a new tone pair. The GTO output acts to reset the external steering time constant, and its state is a function of ESO and the voltage on SI
18	V <sub>DD</sub>	Power Supply (+5V, Typ)



## ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	$V_{DD}$	6	V
Analog Input Voltage Range	$V_{I(A)}$	- 0.3 ~ $V_{DD} + 0.3$	V
Digital Input Voltage Range	$V_{I(D)}$	- 0.3 ~ $V_{DD} + 0.3$	V
Output Voltage Range	$V_O$	- 0.3 ~ $V_{DD} + 0.3$	V
Current On Any Pin	$I_I$	10	mA
Operating Temperature	$T_{OPR}$	- 40 ~ + 85	°C
Storage Temperature	$T_{STG}$	-60 ~ + 150	°C

ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5V$ ,  $T_a = 25^\circ C$ , unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$	-	4.75	-	5.25	V
Operating Current	$I_{DD}$	-	-	3.0	9.0	mA
Power Dissipation	$P_D$	-	-	15	45	mW
Input Voltage Low	$V_{IL}$	-	-	-	1.5	V
Input Voltage High	$V_{IH}$	-	3.5	-	-	V
Input Leakage Current	$I_{I(LKG)}$	$V_{IN} = GND$ or $V_{DD}$	-	0.1	-	$\mu A$
Pull Up Current On OE Pin	$I_{PU}$	OE = GND	-	7.5	15	$\mu A$
Analog Input Impedance	$R_I$	$f_{IN} = 1KHz$	8	10	-	$M\Omega$
Steering Input Threshold Voltage	$V_{TH}$	-	2.2	-	2.5	V
Output Voltage Low	$V_{OL}$	No Load	-	-	0.03	V
Output Voltage High	$V_{OH}$	No Load	4.97	-	-	V
Output Current (Sink)	$I_{O(SINK)}$	$V_{OL} = 0.4V$	1	2.5	-	mA
Output Current (Source)	$I_{O(SOURCE)}$	$V_{OH} = 4.6V$	0.4	0.8	-	mA
$V_{REF}$ Output Voltage	$V_{O(REF)}$	-	2.4	-	2.8	V
$V_{REF}$ Output Resistance	$R_{O(REF)}$	-	-	10	-	$K\Omega$
Analog Input Offset Voltage	$V_{IO}$	-	-	25	-	mV
Power Supply Rejection Ratio	PSRR	Gain Setting Amp at 1KHz	-	60	-	dB
Common Mode Rejection Ratio	CMRR	- 3.0V < $V_{IN}$ < 3.0V	-	60	-	dB
Open Loop Voltage Gain	$G_V$	Gain Setting Amp at 1KHz	-	65	-	dB
Open Loop Unit Gain Bandwidth	BW	-	-	1.5	-	MHz
Analog Output Voltage Swing	$V_{O(P-P)}$	$R_L = 100K$	-	4.5	-	$V_{P-P}$
Acceptable Capacitive Load	$C_L$	GS	-	100	-	pF
Acceptable Resistive Load	$R_L$	GS	-	50	-	$K\Omega$
Analog Input Common Mode Voltage Range	$V_{CM}$	No Load	-	3.0	-	$V_{P-P}$



AC ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5V$ ,  $T_a = 25^\circ C$ ,  $f_{CK} = 3.579545MHz$ )

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Valid Input Signal Range (each tone of composite signal)	$V_{I(NAL)}$	-	-29	-	1.0	dBm
Dual Tone Twist Accept	TW	-	-	$\pm 10$	-	dB
Acceptable Frequency Deviation	$\Delta f$	-	-	-	$\pm 1.5\%$ $\pm 2Hz$	-
Frequency Deviation Reject	$\Delta f_R$	-	$\pm 3.5\%$	-	-	-
Third Tone Tolerance	T3rd	-	-25	-16	-	dB
Noise Tolerance	$T_N$	-	-	-12	-	dB
Dial Tolerance	DT	-	18	22	-	dB
Crystal Clock Frequency	$f_{CK}$	-	3.5759	3.5795	3.5831	MHz
Maximum Clock Input Rise Time	$t_{R(MAX)}$	External Clock	-	-	110	nS
Maximum Clock Input Fall Time	$t_{F(MAX)}$	External Clock	-	-	110	nS
Acceptable Clock Input Duty Cycle	$D_{CK}$	External Clock	40	50	60	%
Acceptable Capacitive Load	$C_L$	OSC2 PIN	-	-	30	pF
Tone Present Detect Time	$t_{DET(P)}$	-	5	11	14	mS
Tone Absent Detect Time	$t_{DET(A)}$	-	0.5	4	8.5	mS
Minimum Tone Duration Accept	$t_{TDA(MIN)}$	User Adjustable	-	-	40	mS
Maximum Tone Duration Reject	$t_{TDR(MAX)}$	User Adjustable	20	-	-	mS
Acceptable Interdigit Pause	$t_{IDP(A)}$	User Adjustable	-	-	40	mS
Rejectable Interdigit Pause	$t_{IDP(R)}$	User Adjustable	20	-	-	mS
Propagation Delay Time SI to Q	$t_{D(SI-Q)}$	OE = High	-	8	11	$\mu S$
Propagation Delay Time SI to DSO	$t_{D(SI-D)}$	OE = High	-	12	16	$\mu S$
Output Data Setup Q to DSO	$t_{SU}$	OE = High	-	3.4	-	$\mu S$
Propagation Delay Time OE to Q (Enable)	$t_{D(OE-Q)EN}$	$R_L = 10K, C_L = 50pF$	-	50	60	nS
Propagation Delay Time OE to Q (disable)	$t_{D(OE-Q)DIS}$	$R_L = 10K, C_L = 50pF$	-	300	-	nS

- Notes :
1. Digit sequence consists of all 16 DTMF tones.
  2. Tone duration = 40mS, Tone pause = 40mS.
  3. Nominal DTMF frequencies are used.
  4. Both tones in the composite signal have an equal amplitude.
  5. Tone pair is deviated by  $\pm 1.5\% \pm 2Hz$ .
  6. Bandwidth limited (3KHz) Gaussian Noise.
  7. The precise dial tone frequencies are (350Hz and 440Hz)  $\pm 2\%$ .
  8. For an error rate of better than 1 in 10000.
  9. Referenced to lowest level frequency component in DTMF signal.
  10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
  11. This item also applies to a third tone injected onto the power supply.
  12. Referenced to Fig. 1 Input DTMF tone level at -28dBm.



ELECTRONICS

# KT3170

# LOW POWER DTMF RECEIVER

## TEST CIRCUIT

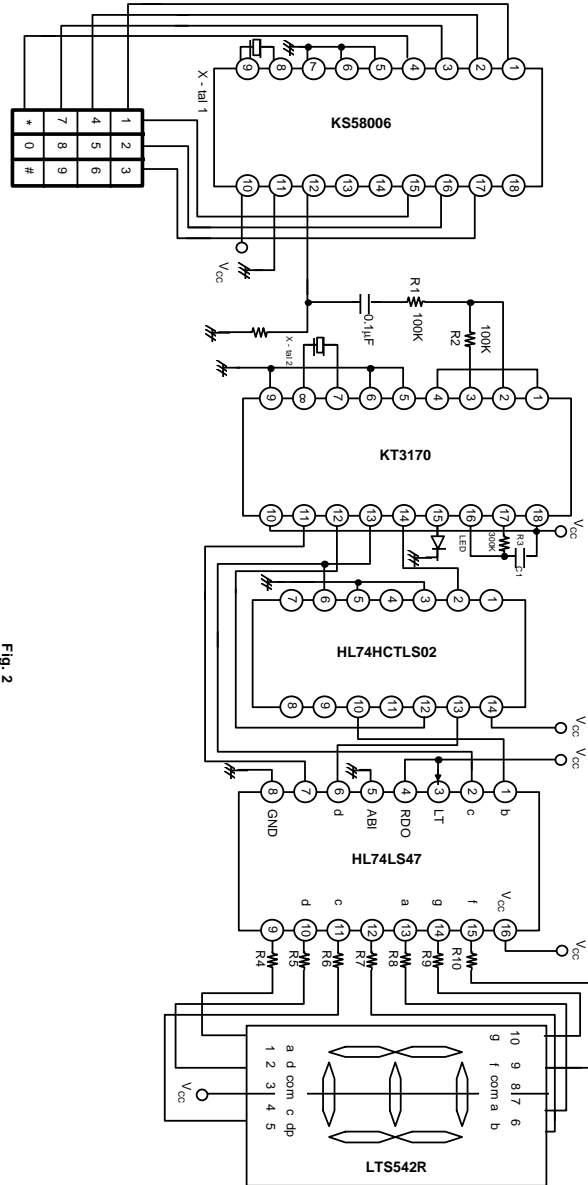


Fig. 2



**TIMING DIAGRAM**

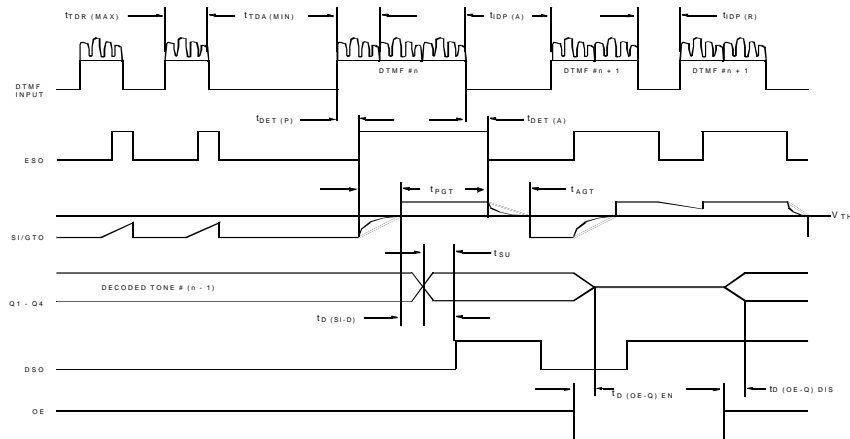


Fig. 3

**DIGITAL OUTPUT**

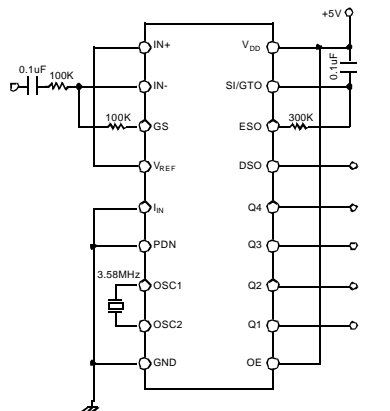
Outputs Q1-Q4 are CMOS push pull when enabled (EO = High) and open circuited (high impedance) when disabled by pulling EO = Low. These digital outputs provide the hexadecimal code corresponding to the DTMF signals. The table below describes the hexadecimal.

NO	LOW FREQUENCY	HIGH FREQUENCY	OE	Q4	Q3	Q2	Q1
1	697	1209	H	0	0	0	1
2	697	1336	H	0	0	1	0
3	697	1477	H	0	0	1	1
4	770	1209	H	0	1	0	0
5	770	1336	H	0	1	0	1
6	770	1477	H	0	1	1	0
7	852	1209	H	0	1	1	1
8	852	1336	H	1	0	0	0
9	852	1477	H	1	0	0	1
0	941	1336	H	1	0	1	0
*	941	1209	H	1	0	1	1
#	941	1477	H	1	1	0	0
A	697	1633	H	1	1	0	1
B	770	1633	H	1	1	1	0
C	852	1633	H	1	1	1	1
D	941	1633	H	0	0	0	0
ANY	-	-	L	Z	Z	Z	Z

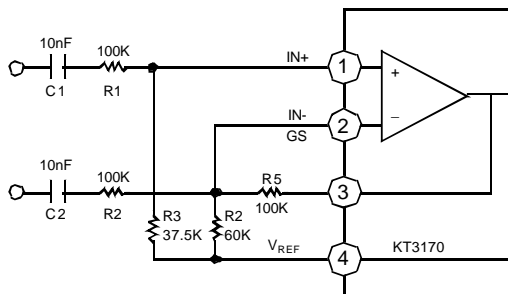
Z : High Impedance  
 H : High Logic Level  
 L : Low Logic Level



APPLICATION CIRCUIT



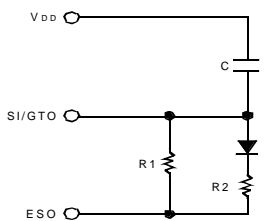
All resistors are 1% tolerance  
All capacitors are 5% tolerance



$R3 = R2R5/(R2+R5)$ , VOLTAGE GAIN =  $R5/R1$   
INPUT IMPEDANCE :  $2 \sqrt{R1^2 + (1/\omega C)^2}$   
All resistors are 1% tolerance  
All capacitors are 5% tolerance

Fig. 4 Single Ended Input Configuration

Fig. 5 Differential Ended Input Configuration

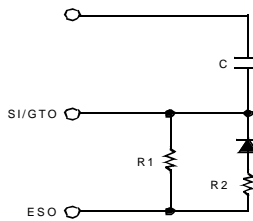


$$t_{PGT} = (R1C) \ln(V_{DD}/V_{DD}-V_{TH})$$

$$t_{AGT} = (RPC) \ln(V_{DD}/V_{TST})$$

$$R_P = R1R2/(R1 + R2)$$

(a) Decreasing  $t_{AGT}$  ( $t_{PGT} > t_{AGT}$ )



$$t_{PGT} = (RPC) \ln(V_{DD}/V_{DD}-V_{TH})$$

$$t_{AGT} = (R1C) \ln(V_{DD}/V_{TH})$$

$$R_P = R1R2/(R1 + R2)$$

(a) Decreasing  $t_{PGT}$  ( $t_{PGT} < t_{AGT}$ )

Fig. 6 Guard Time Adjustment

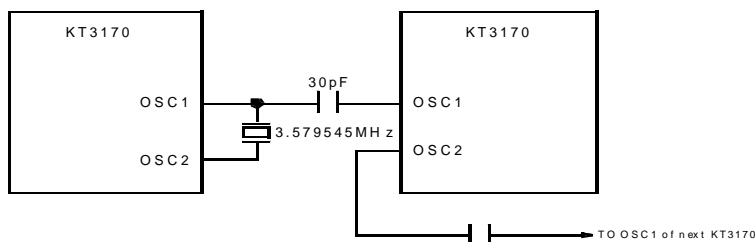


Fig. 7 Oscillator Connection

