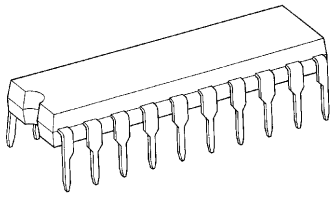
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD6359P, TD6359N

FREQUENCY SYNTHESIZER FOR TV / CATV

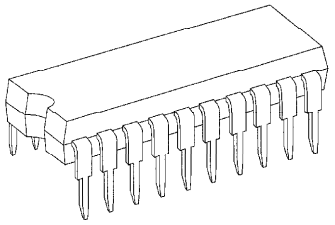
The TD6359P and TD6359N are single-chip frequency synthesizer ICs, which can organization high-performance frequency synthesizer systems in combination with a 4bit μCPU controller.
The TD6359P integrates high input sensitivity ECL prescaler, I^2L programmable counter, PLL logic and bandswitch drive decoder in a DIP 20-pin small package.
The TD6359N is packaged in a shrink 20 pin package even smaller than TD6359P.

TD6359P



DIP20-P-300-2.54A

TD6359N



SDIP20-P-300-1.78

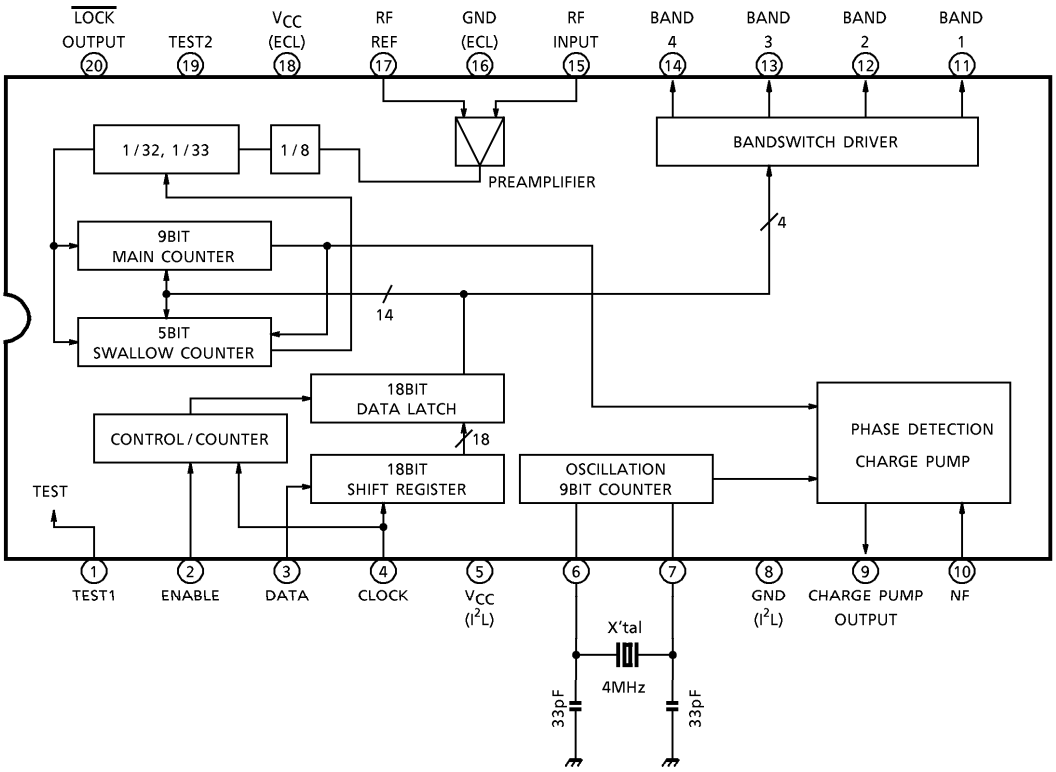
Weight
DIP20-P-300-2.54A : 2.25g (Typ.)
SDIP20-P-300-1.78 : 1.02g (Typ.)

FEATURES

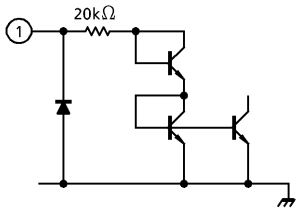
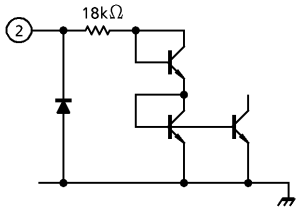
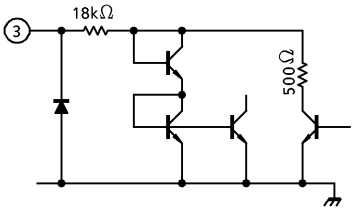
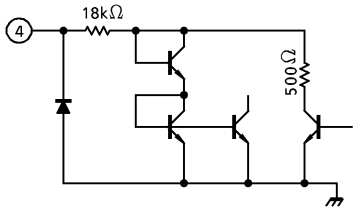
- High input sensitivity
  f_{in} = 80~100MHz : −24dBmW (50Ω) (Min.)
  f_{in} = 0.1~1GHz : −27dBmW (50Ω) (Min.)
- Wide operating frequency : 1GHz (Max.)
- Simple control bus : 18bit serial input
- 5V single power supply operation
- 4MHz basic oscillator and 62.5kHz frequency step
- Bandswitch driver : 4 channels

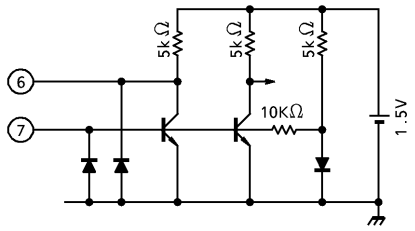
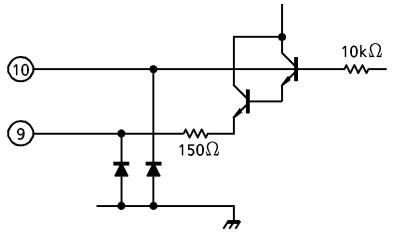
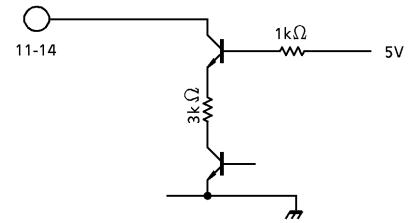
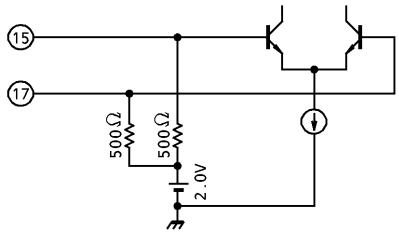
(Note) Handle with care as this product is weak at surge voltage.

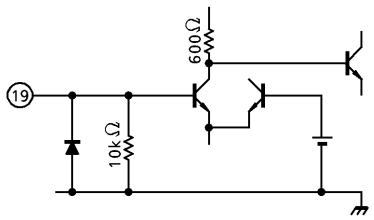
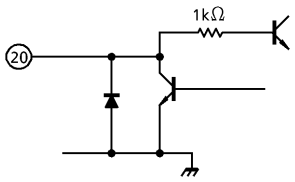
BLOCK DIAGRAM



TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	Test Pin 1	Low level : this will be in normal use operation mode when connected to GND or open. In order to prevent a static breakdown, it will be more effective to connect to GND. High level : this will be in test mode when connected to V_{CC}.	
2	Enable Input	This is an enable pulse input terminal at normal use operation. This will be a test mode select terminal of test mode by means of the pin 1 mode select pin. In order to prevent a static breakdown, it will be effective to connect in series a resistor of about 1kΩ. The pins 3 and 4 below are the same as this pin.	
3	Data Input	This is a data input terminal in normal mode. In test mode 1 or 2, this will be a main counter output terminal. In test mode 3, this can be an external input terminal of comparating signal of phase comparator (a counter output terminal in normal mode).	
4	Clock Input	This is a clock pulse input terminal in normal mode. In test mode 1 or 2, this will be an output terminal of reference signal whose crystal oscillator is divided by 2^9. In test mode 3, this can be an input terminal of external reference signal.	
5	Logic V_{CC}	This is logic circuit power-supply. Connect a bypass condenser between this pin and pin 8.	—

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
6 7	Crystal Oscillation	This is a crystal oscillation terminal to make the reference signal. Make sure to use the logic GND of pin 8 as this oscillates in a big amplitude (about 800mV$_{p-p}$).	
8	Logic GND	This is used for crystal oscillator GND as is logic GND. Never wire this pin close to the high frequency GND of pin 16.	—
9 10	Frequency Phase Comparator Output	In normal use, this compares a high frequency wave input with frequency data and feeds back its difference by means of the supply pump.	
11~ 14	Bandswitch	This can make the 4 band switching operate independently. The external driver can freely be operated anywhere between 1~4 pins. Connect an unused pin to the bandswitch power supply.	
15 17	Reference Bias By RF Input	This is an input terminal of local oscillation of tuner. In order to prevent disturbance or unwanted resonance, use the pattern of short distance or lead wire for pin 15. Also, connect a bypass condenser to pin 16 for pin 17 as well.	
16	High Frequency GND	This is mainly used for a bypass condenser of pins 17 and 18 as is high frequency GND. Also the pattern should be lay out so as to be separated from the logic GND of pin 8.	—

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
18	High Frequency V_{CC}	This is high frequency circuit power supply. Connect a bypass condenser between this pin and pin 8.	—
19	Test Pin 2	This is used only when in test mode 2. This terminal is possible to be input to the main counter without passing through a 1/8 prescaler. Leave this pin open in normal use.	
20	$\overline{\text{Lock}}$ Output	In normal use, a pull up resistor is connected to V_{CC}. It will be low level only when PLL is locked. In test mode, this will be the test 1 or 2 select terminal and in mode 3, this will be a 256 divided output terminal of high frequency input. This is used for measuring the input sensitivity of a prescaler.	

OPERATION WHEN IN TEST MODE

If the test 1 terminal (pin 1) is set to high level, this will be test mode.
There are three kinds of test modes as follows :

(1) Mode 1, Mode 2

In mode 1 and 2, a test to inspect the PLL lock condition is executed. After inputting data to the main counter and swallow counter by means of the method indicated in the diagram 2, the test 1 terminal (pin 1) will be set to high level while the enable terminal (pin 2) is held to low level. In this condition, a comparating frequency signal is output to the clock terminal (pin 4) and a main counter division signal to the data terminal (pin 3).
The method of inputting to a divider has two kinds : mode 1 and mode 2.

Mode 1. This is the method of inputting from the RF input terminal (pin 15) by setting the lock terminal (pin 20) to high level.
The lock condition in normal use operation can be inspected using this method.

Mode 2. This is the method of directly inputting to a 1/32 and 1/33 divider from the test 2 terminal (pin 19) without passing through a 1/8 prescaler by setting the lock terminal (pin 20) to low level.

(2) Mode 3

In mode 3, a prescaler, phase comparator, and charge pump will be tested.
If both test 1 terminal (pin 1) and enable terminal (pin 2) are set to high level, these will be in mode 3. The clock terminal (pin 4) will be comparison reference frequency signal input of phase comparator, the data terminal (pin 3) is a comparated frequency signal input, and the lock terminal (pin 20) is a prescaler output (the fixed dividing ratio of 1/256).

The output polarity of phase comparator is as follows :

INPUT FREQUENCY	CHARGE PUMP OUTPUT PIN (PIN 9)
Input frequency > Programmed frequency	High level
Input frequency < Programmed frequency	Low level

TEST MODE

PIN NAME	NORMAL	MODE 1	MODE 2	MODE 3
Test 1 (Pin 1)	L	H	H	H
Enable (Pin 2)	Enable	L	L	H
Lock (Pin 20)	$\overline{\text{Lock}}$	H (Pin 15 input)	L (Pin 19 input)	1/256 output (Pin 15 input)
Clock (Pin 4)	Clock input	Comparison reference signal output (7.8125kHz)	Comparison reference signal output (7.8125kHz)	P.D. Reference signal input
Data (Pin 3)	Data input	Main counter output	Main counter output	P.D. Comparison signal input
Test 2 (Pin 19)	Inhibit	Inhibit	Divider input	Inhibit
RF Input (Pin 15)	RF input	RF input	Inhibit	RF input

THE METHOD OF INPUTTING DATA

The method of inputting data will be indicated in the diagram 1.

LOCK FREQUENCY CALCULATION METHOD

The lock frequency can be calculated in the following formula :

$f_{OSC} = f_r \times 8 \times (32M + S)$

f_{OSC} : The oscillation frequency of V_{CO} (the input frequency of prescaler)
$64MHz \leqq f_{OSC}$ X'tal = 4MHz

f_r : Reference frequency ; it will be 1/512 of oscillation frequency of a crystal oscillator. When a 4MHz crystal oscillator is used, this will be $f_r = 7.8125kHz$ and the lock frequency step will be 62.5kHz.

M : Preset value of Main counter ; The 9 bits between MSB to MSB-8.
Input $32 \leqq M \leqq 511$ value in binary.

S : Preset value of Swallow counter ; The 5 bits between MSB-9 to LSB.
Input $0 \leqq S \leqq 31$ value in binary.

For example, when $f_{OSC} = 801MHz$ is received at the reference frequency of 7.8125kHz,

$801 \times 10^3 = 7.8125 \times 8 \times (32M + S)$

$32M + S = 12816$

$M = 400_{(10)} = 110010000_{(2)}$

$S = 16_{(10)} = 10000_{(2)}$

Further, if the band "4" is used, the received data will be as follows :

1000 | 1100100000 | 10000

BAND — MAIN COUNTER — SWALLOW COUNTER

DIAGRAM 1. Normal use

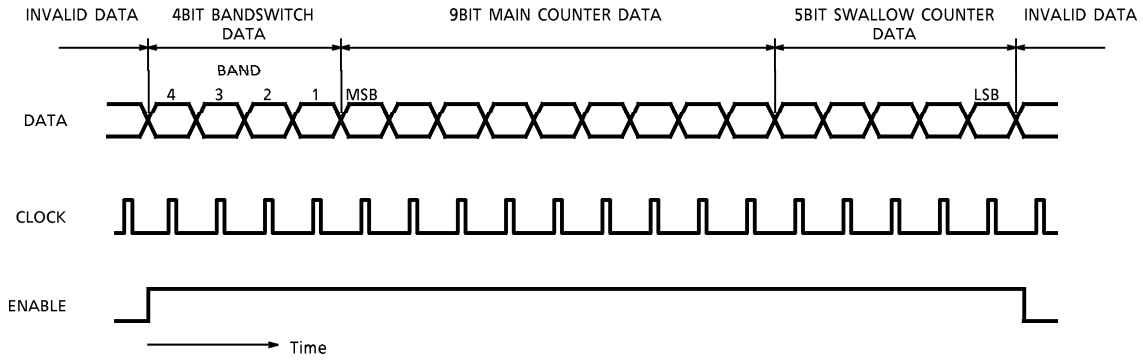


DIAGRAM 2. Test mode (Mode 1, 2)

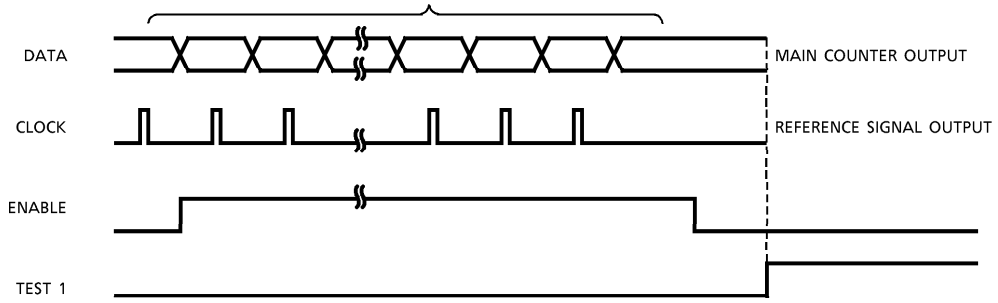
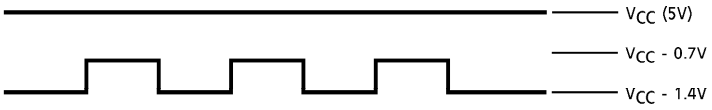


DIAGRAM 3. 1/32, 1/33 input level



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	6.5	V
ECL Input Voltage	V_{in1}	2.0	V_{p-p}
Logic Input Voltage	V_{in2}	−0.3~V_{CC}	V
Power Dissipation	P_D	(Note 1)	W
Operating Temperature	T_{opr}	−20~75	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note 1) P-type : 1.4W, N-type : 1.7W

(Note 2) When using the device at above Ta = 25°C, decrease the power dissipation by 11.2mW for P-type and 9.5mW for N-type each increase of 1°C.

(Note 3) Handle with care as this product is weak at surge voltage.

RECOMMENDED SUPPLY VOLTAGE

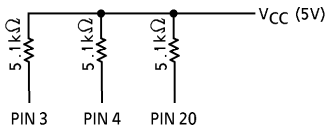
PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
5	ECL V_{CC}	4.5	5	5.5	V
18	I^2L V_{CC}	4.5	5	5.5	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C)

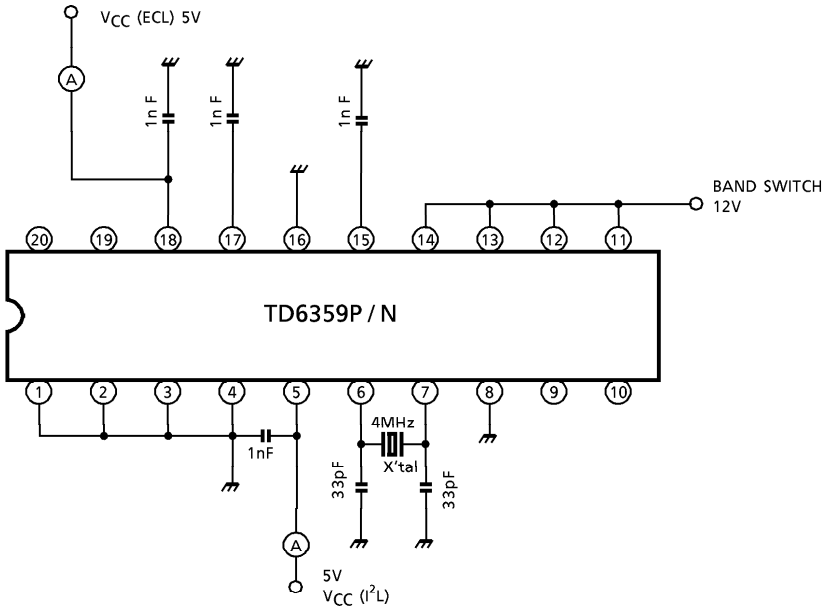
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	(ECL)	I_{CC1}	2		40	60	80	mA
	(I^2L)	I_{CC2}	2		15	25	35	
Bandswitch Max. Voltage		V_B MAX.	—	Band 1~4	12	—	15	V
Bandswitch Inflow Current		I_B MAX.	—	V_{CC} = 5V	0.7	—	2.2	mA
DC Voltage		V_{15}	—	—	1.7	2.0	2.3	V
		V_{17}	—	—	1.7	2.0	2.3	
DC Current High Level		I_{IH}	—	V_{in} = 5V (Note 1)	—	180	300	μA
Input Voltage	"H" Level	V_{IH}	—	(Note 1)	3.0	—	—	V
	"L" Level	V_{IL}	—		—	—	0.8	
Output Voltage	"H" Level	V_{OH}	1	(Note 2)	3.8	—	—	V
	"L" Level	V_{OL}	1		—	—	0.5	
N/F Leak Current		I_L	—	(Note 3)	−0.2	—	0.2	μA
RF Input Sensitivity		V_{in1}	3	f_{in} = 80 – 100MHz	−24	—	3	dBmW (50Ω)
		V_{in2}	3	f_{in} = 100 – 1000MHz	−27	—	3	
Setup Time		T_S	—	Data timing chart	2	—	—	μs
Enable Hold Time		T_{SL}	—		2	—	—	
Enable Inhibit Time		T_{NE}	—		6	—	—	
Clock Inhibit Time		T_{NC}	—		6	—	—	
Clock Width		T_C	—		2	—	—	
Enable Setup Time		T_L	—		10	—	—	
Data Hold Time		T_H	—		2	—	—	

(Note 1) TEST 1, Enable, Clock, $\overline{Lock}$: applied to input mode.
(Note 2) Data, Clock, $\overline{Lock}$: applied to output mode.
(Note 3) Pin 10 : 2.1V, Pin 9 : Open

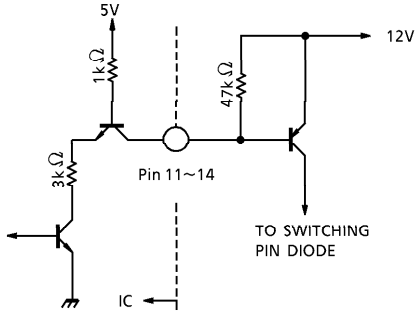
TEST CIRCUIT 1. Test mode



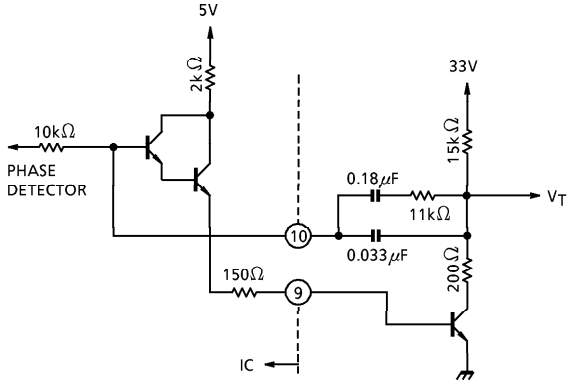
TEST CIRCUIT 2. Power supply test circuit



Bandswitch output circuit



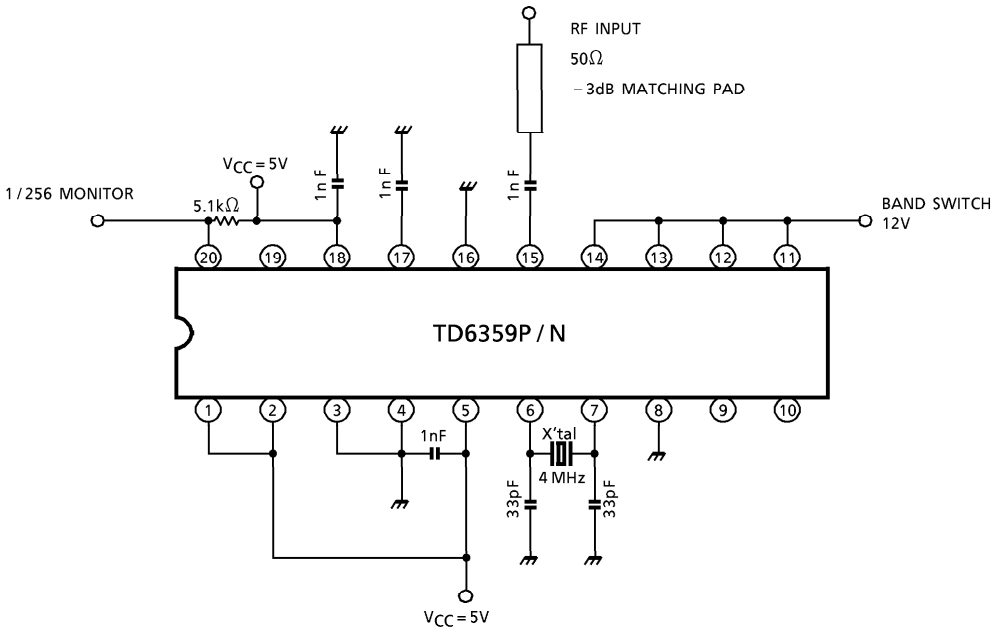
Phase detection output circuit



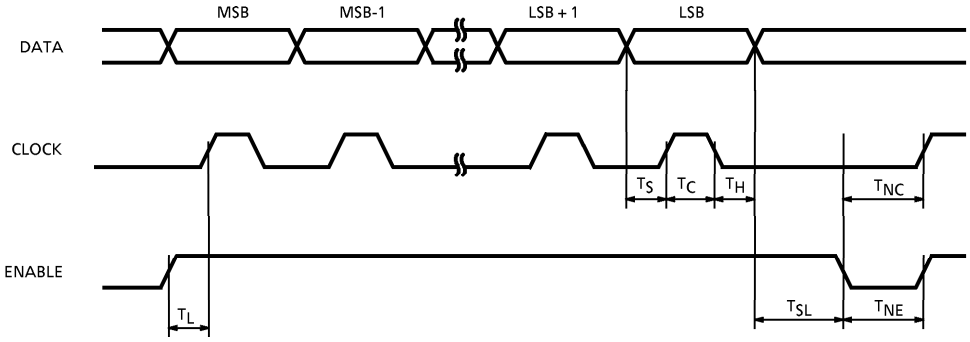
The output polarity of phase detector is as follows :

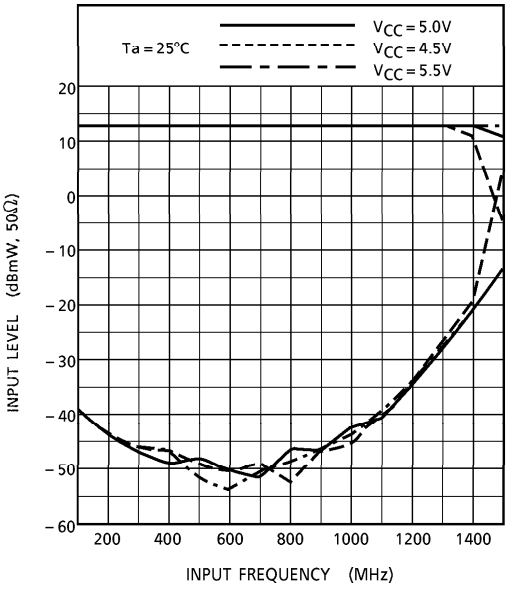
INPUT FREQUENCY	P.D. OUTPUT (PIN 9)
Input frequency > Programmed frequency	High level
Input frequency < Programmed frequency	Low level

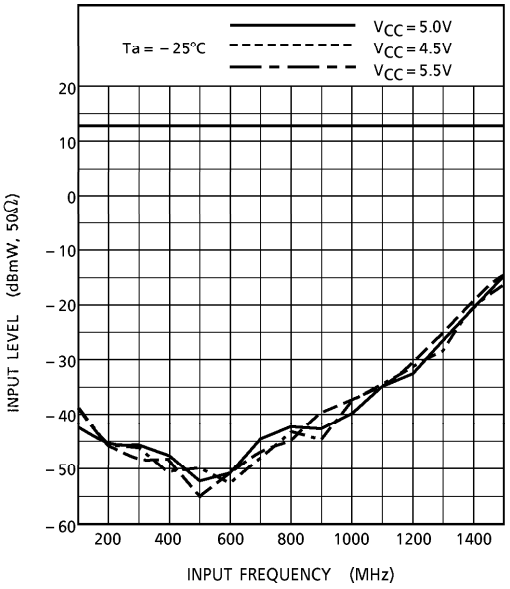
TEST CIRCUIT 3. Input sensitivity test circuit

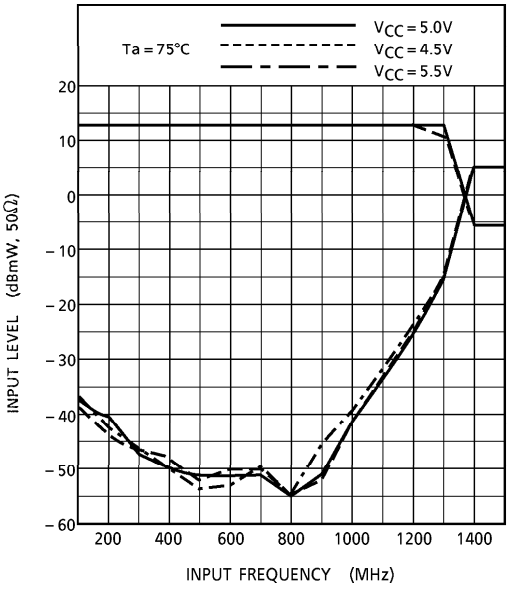


DATA TIMING CHART (Rising timing)

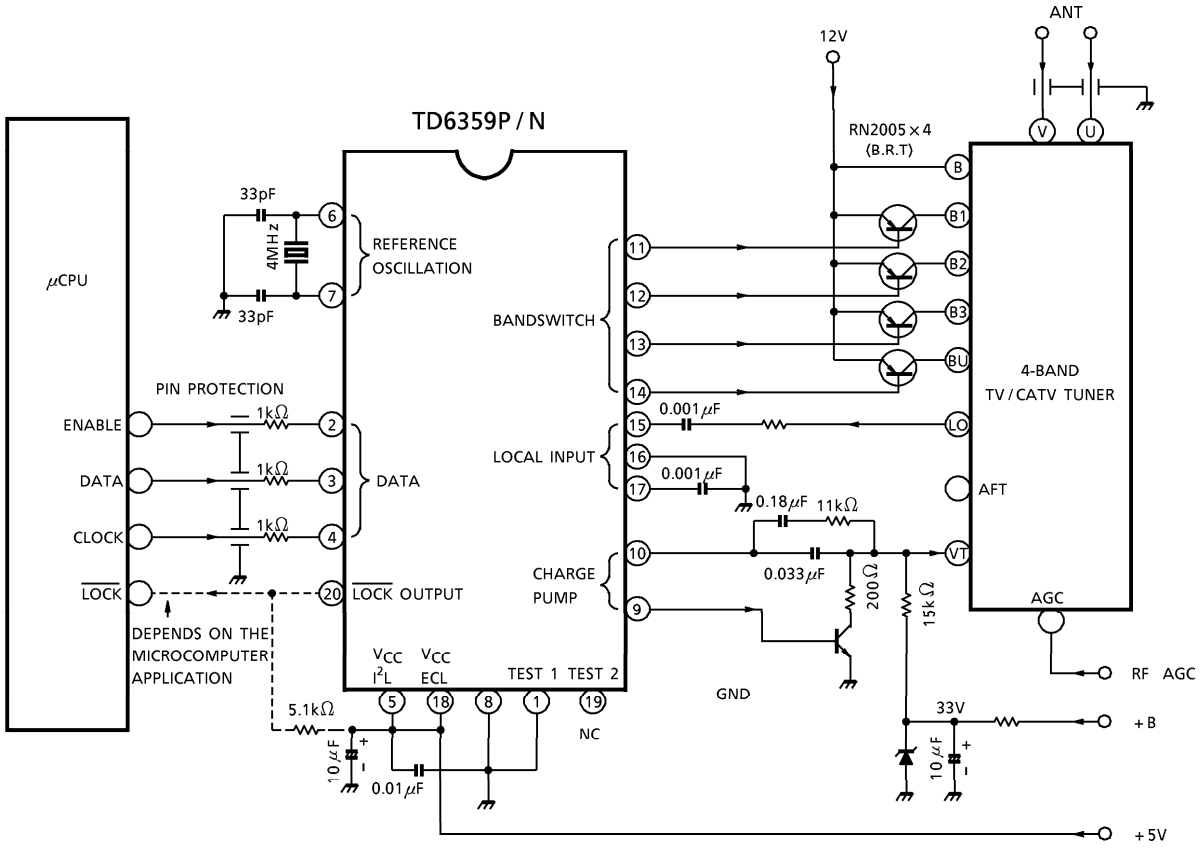








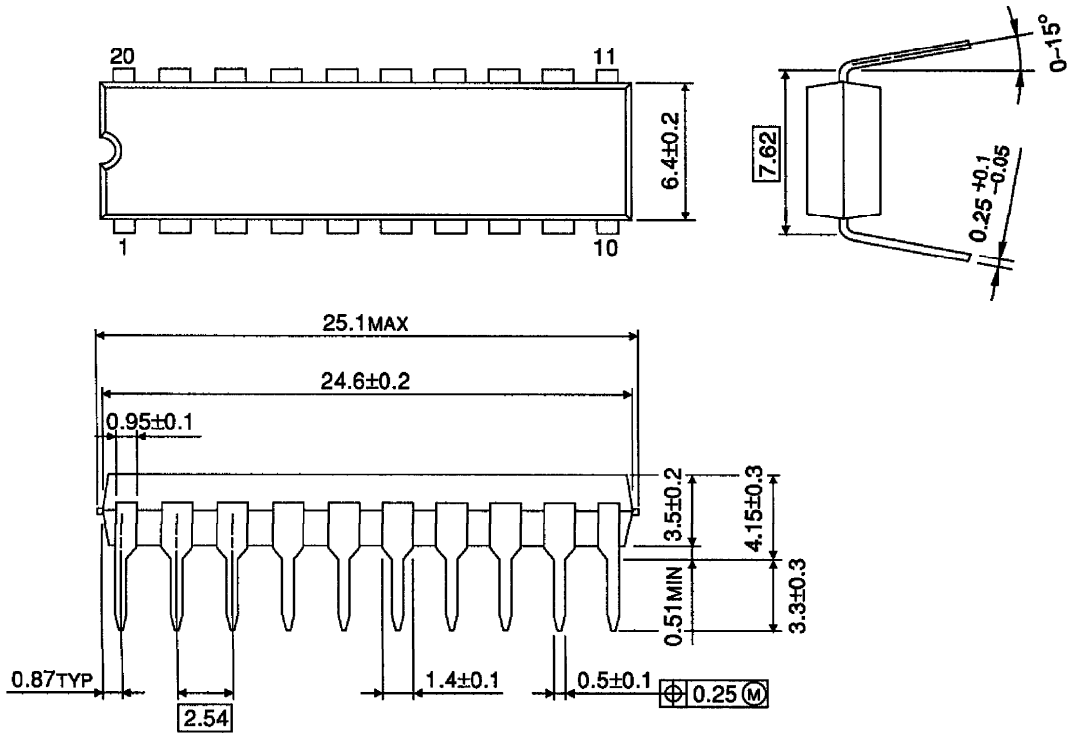
APPLICATION CIRCUIT EXAMPLE OF FREQUENCY SYNTHESIZER



OUTLINE DRAWING

DIP20-P-300-2.54A

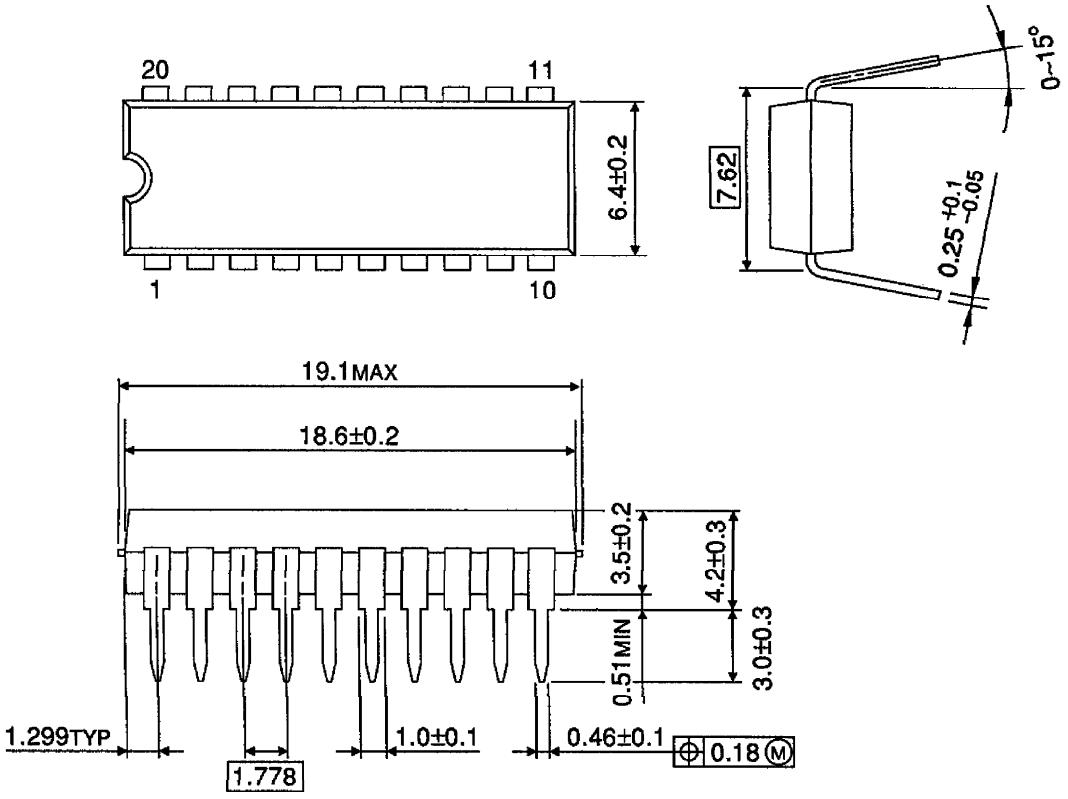
Unit : mm



Weight : 2.25g (Typ.)

OUTLINE DRAWING

SDIP20-P-300-1.78 Unit : mm



Weight : 1.02g (Typ.)