FAIRCHILD

SEMICONDUCTOR ™

MM74C86
Quad 2-Input EXCLUSIVE-OR Gate

General Description

The MM74C86 employs complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range: 3.0V to 15V
■ Guaranteed noise margin: 1.0V
■ High noise immunity: 0.45 V_{CC} (typ.)
■ Low power: TTL compatibility:
   Fan out of 2 driving 74L
■ Low power consumption: 10 nW/package (typ.)
■ The MM74C86 follows the MM74LS86 Pinout

Ordering Code:

Order Number	Package Number	Package Description
MM74C86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74C86N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

Top View
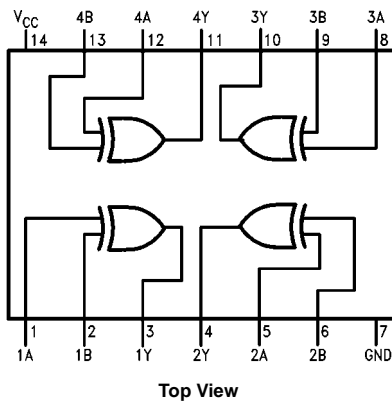
Truth Table

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Level
L = LOW Level

MM74C86

Absolute Maximum Ratings (Note 1)

Voltage at any Pin (Note 1)	-0.3V to $V_{CC} + 0.3$V
Operating Temperature Range	$-55°$C to $+125°$C
Storage Temperature Range	$-65°$C to $+150°$C
Power Dissipation (P_D)	
Dual-In-Line Package	700 mW
Small Outline	500 mW
Operating Range (V_{CC})	3.0V to 15V
Absolute Maximum (V_{CC})	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0$V	3.5			V
		$V_{CC} = 10$V	8.0			
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0$V			1.5	V
		$V_{CC} = 10$V			2.0	
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0$V, $I_O = -10$ μA	4.5			V
		$V_{CC} = 10$V, $I_O = -10$ μA	9.0			
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0$V, $I_O = +10$ μA			0.5	V
		$V_{CC} = 10$V, $I_O = +10$ μA			1.0	
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15$V, $V_{IN} = 15$V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15$V, $V_{IN} = 0$V	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15$V		0.01	15	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75$V	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75$V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75$V, $I_O = -360$ μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75$V, $I_O = 360$ μA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0$V, $V_{OUT} = 0$V $T_A = 25°$C	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10$V, $V_{OUT} = 0$V $T_A = 25°$C	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0$V, $V_{OUT} = V_{CC}$ $T_A = 25°$C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10$V, $V_{OUT} = V_{CC}$ $T_A = 25°$C	8.0	16		mA

AC Electrical Characteristics (Note 2)
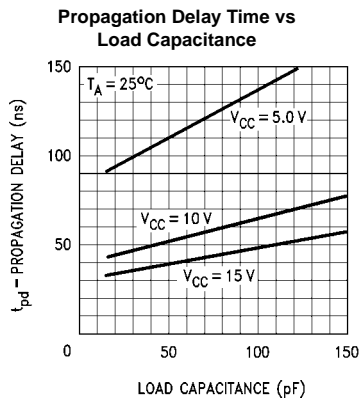
$T_A = 25°$C, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Time to Logical "1" or "0"	$V_{CC} = 5.0$V		110	185	ns
		$V_{CC} = 10$V		50	90	
C_{IN}	Input Capacitance	(Note 3)		5.0		pF
C_{PD}	Power Dissipation Capacitance	Per Gate (Note 4)		20		pF

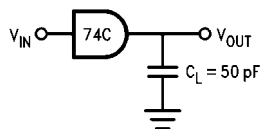**Note 2:** AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

Typical Performance Characteristics

**Propagation Delay Time vs
Load Capacitance**

$T_A = 25°C$
$V_{CC} = 5.0$ V
$V_{CC} = 10$ V
$V_{CC} = 15$ V

t_{pd} – PROPAGATION DELAY (ns)

LOAD CAPACITANCE (pF)

Test Circuits and Waveforms

V_{IN} 74C V_{OUT}
$C_L = 50$ pF

Delays Measured with Input t_r, $t_f = 20$ ns

FIGURE 1. AC Test Circuit

t_r t_f
V_{CC}
V_{IN} 90% 90%
50% 50%
0V 10% 10%
t_{pd}
V_{CC} t_{pd0}
V_{OUT} 50% 50%
0V
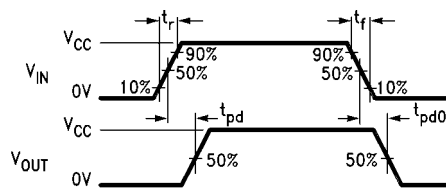
FIGURE 2. Switching Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

LEAD NO. 1
IDENT

30°
TYP

1 2 3 4 5 6 7

0.010
(0.254) MAX

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)
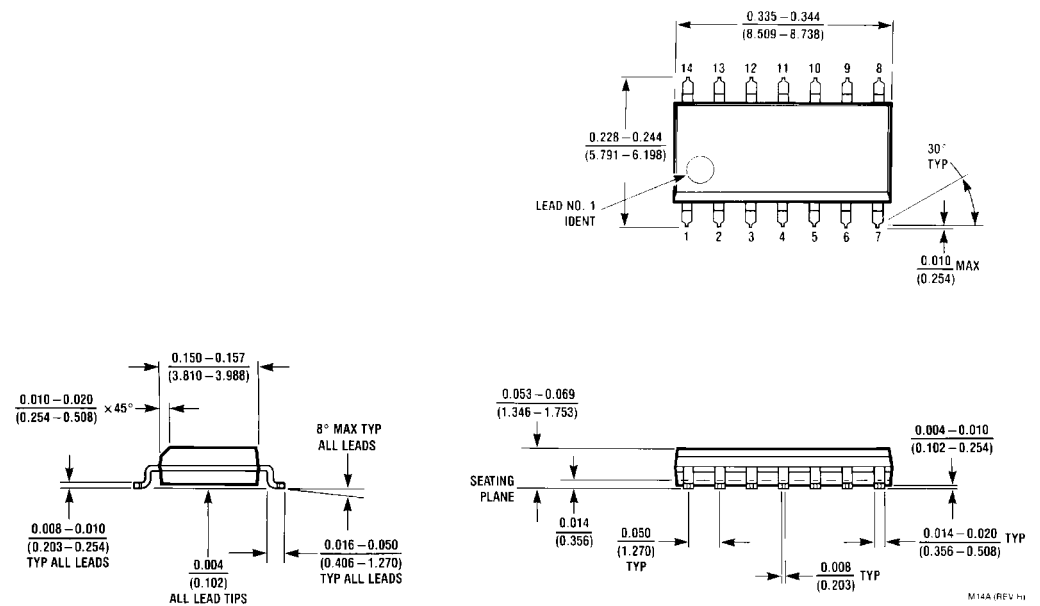
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
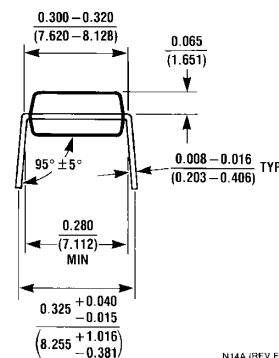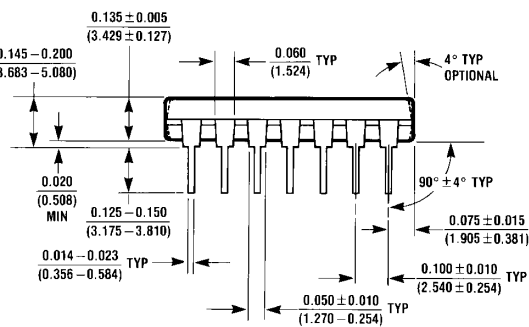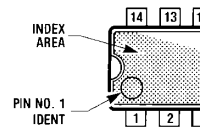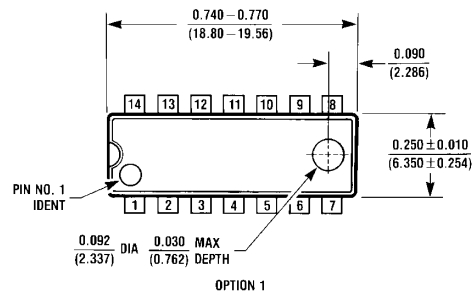
14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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