LXT9762/9782

Fast Ethernet 10/100 Multi-Port Transceiver with Serial MII

Datasheet

General Description

The LXT9782 is an eight-port PHY Fast Ethernet Transceiver that supports IEEE 802.3 physical layer applications at both 10 and 100 Mbps. The LXT9762 offers the same features and functionality in a six-port device. This data sheet uses the singular designation "LXT97x2" to refer to both devices.

The LXT97x2 interfaces multiple Serial Media Independent Interface (SMII) compliant controllers to 10BASE-T and/or 100BASE-TX media.

All network ports provide a combination twisted-pair (TP) or pseudo-ECL (PECL) interface for a 10/100BASE-TX or 100BASE-FX connection.

The LXT97x2 provides three discrete LED drivers for each port, and eight global serial LED outputs. It supports both half- and full-duplex operation at 10 and 100 Mbps and requires only a single 3.3V power supply.

Application

- 100BASE-T, 10/100-TX, or 100BASE-FX Switches and multi-port NICs.

Product Features

- Multiple independent IEEE 802.3-compliant 10/100 ports with integrated filters
- Proprietary Optimal Signal Processing (OSP™) design improves SNR by 3 dB over ideal analog filters
- Robust baseline wander correction for improved 100BASE-TX performance
- 100BASE-FX fiber-optic capability on all ports
- Supports both auto-negotiation and legacy systems without auto-negotiation capability
- JTAG boundary scan
- Multiple Serial MII (SMII) ports for independent PHY port operation
- Configurable via MDIO port or external control pins
- Maskable interrupts
- Very low power consumption (400 mW per port, typical)
- 3.3V operation
- 208-pin PQFP and 272-lead BGA
- 0-70°C ambient temperature range

As of January 15, 2001, this document replaces the Level One document *LXT9762/9782 — Fast Ethernet 10/100 Multi-Port Transceiver with Serial MII.*

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Datasheet

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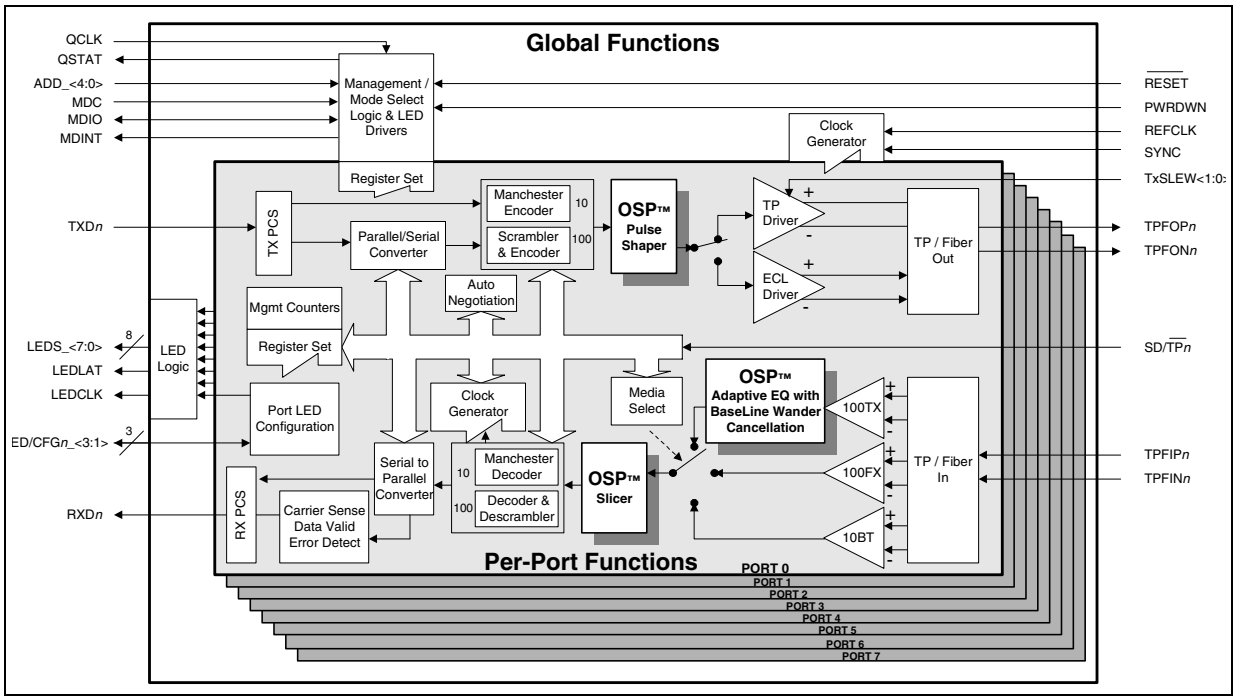
Revision History

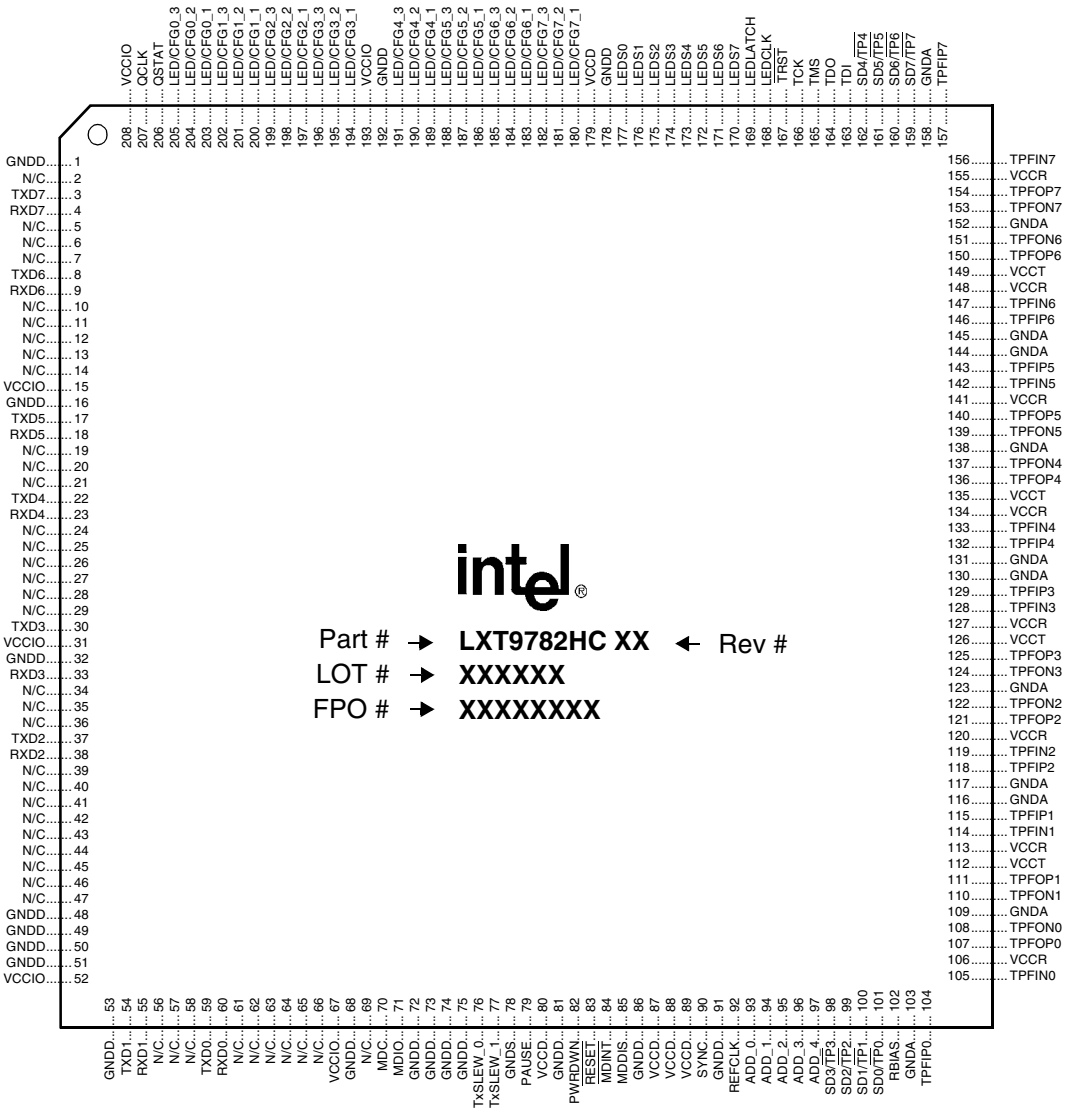
Revision	Date	Description

Figure 1. LXT 9782 Block Diagram



1.0 Preliminary Pin Assignments and Signal Descriptions

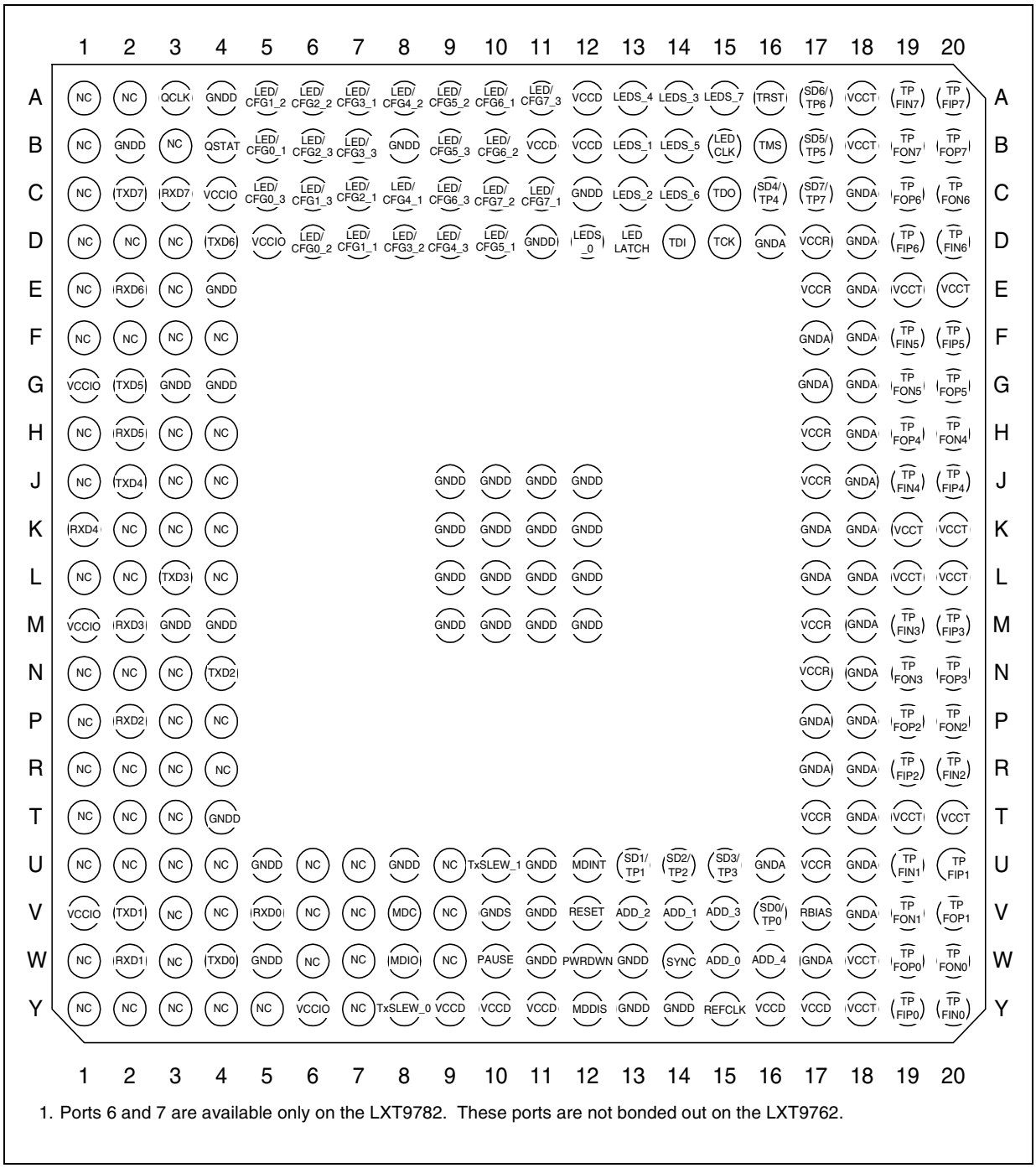
Figure 2. LXT9782HC (PQFP) Preliminary Pin Assignments



Package Topside Markings

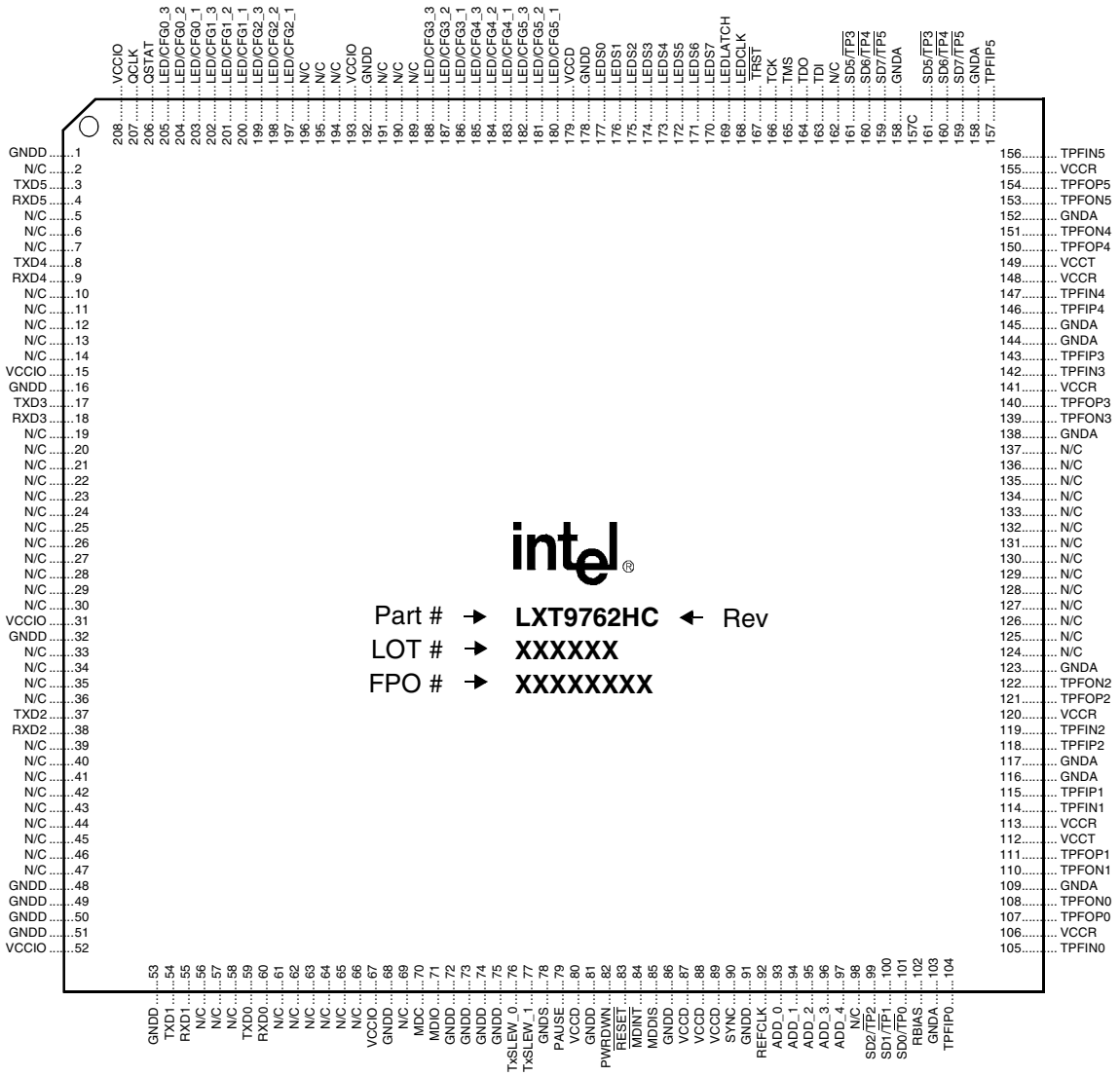
Marking	Definition
Part #	LXT9782 is the unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” (Refer to Specification Update for additional stepping information.)
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Figure 3. LXT9782BC (PBGA) Preliminary Pin Assignments



1. Ports 6 and 7 are available only on the LXT9782. These ports are not bonded out on the LXT9762.

Figure 4. LXT9762HC (PQFP) Preliminary Pin Assignments



1. Ports 6 and 7 are available only on the LXT9782. These ports are not bonded out on the LXT9762.

Package Topside Markings

Marking	Definition
Part #	LXT9762 is the unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” (Refer to Specification Update for additional stepping information.)
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. LXT97x2 Serial MII Signal Descriptions

9762 Pin#	9782 Pin#		Symbol	Type[1]	Signal Description[2, 3]
PQFP	PQFP	PBGA			
Serial MII Data Interface Pins					
59	59	W4	TXD0	I	**Transmit Data - Ports 0-7**. These serial input streams provide data to be transmitted to the network. LXT97x2 clocks the data in synchronously to REFCLK.
54	54	V2	TXD1		
37	37	N4	TXD2		
17	30	L3	TXD3		
8	22	J2	TXD4		
3	17	G2	TXD5		
–	8	D4	TXD6		
–	3	C2	TXD7		
60	60	V5	RXD0	O	**Receive Data - Ports 0-7**. These serial output streams provide data received from the network. LXT97x2 drives the data out synchronously to REFCLK.
55	55	W2	RXD1		
38	38	P2	RXD2		
18	33	M2	RXD3		
9	23	K1	RXD4		
4	18	H2	RXD5		
–	9	E2	RXD6		
–	4	C3	RXD7		
90	90	W14	SYNC	I	**SMII Synchronization.** The MAC must generate a SYNC pulse every 10 REFCLK cycles to synchronize the SMII.
92	92	Y15	REFCLK	I	**Reference Clock**. The LXT97x2 requires a 125 MHz SMII reference clock input at this pin. Refer to Functional Description for detailed clock requirements.
MII Control Interface Pins [3]					
71	71	W8	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for communication between the PHY and MAC or switch ASIC.
84	84	U12	MDINT	OD	**Management Data Interrupt**. When bit 18.1 = 1, an active Low output on this pin indicates status change.
70	70	V8	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 8 MHz.
85	85	Y12	MDDIS	I	**Management Disable**. When MDDIS is High, the MDIO is disabled from read and write operations. When MDDIS is Low at power up or reset, the Hardware Control Interface pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain.
2. Ports 6 and 7 are available only on the LXT9782. These pins are not bonded out on the LXT9762.
3. The LXT97x2 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 2. LXT97x2 Signal Detect/TP Select Signal Descriptions

9762 Pin#	9782 Pin#		Symbol	Type[1]	Signal Description[2]
PQFP	PQFP	PBGA			
101	101	V16	SD0/$\overline{TP0}$	I	**Signal Detect - Ports 0 - 7**. Tying the SD/TP*n* pins High or to a PECL input sets bit 16.0 = 1 and the respective port is forced to FX mode. Do not enable Auto-Negotiation if FX mode is selected. In the absence of an active link, the pin must be pulled High to enable loopback in FX mode. Do not enable Auto-Negotiation if FX mode is selected. The SD/TP*n* pins have internal pull-downs. When not using FX mode, SD/TP*n* pins should be tied to GNDA. **TP Select - Ports 0 - 7**. Tying the SD/TP*n* pins Low sets bit 16.0 = 0 and forces the port to TP mode. The operating mode of each port can be set to 10BASE-T or 100BASE-TX, half- or full-duplex, and auto-negotiation or manual control via the hardware control interface pins as shown in Table 9 on page 27.
100	100	U13	SD1/$\overline{TP1}$		
99	99	U14	SD2/$\overline{TP2}$		
161	98	U15	SD3/$\overline{TP3}$		
160	162	C16	SD4/$\overline{TP4}$		
159	161	B17	SD5/$\overline{TP5}$		
–	160	A17	SD6/$\overline{TP6}$		
–	159	C17	SD7/$\overline{TP7}$		

1. Type Column Coding: I = Input, O = Output.
2. Ports 6 and 7 are available only on the LXT9782. These pins are not bonded out on the LXT9762.

Table 3. LXT97x2 Network Interface Signal Descriptions

9762 Pin#	9782 Pin#		Symbol	Type[1]	Signal Description [2]
PQFP	PQFP	PBGA			
107, 108	107, 108	W19,W20	TPFOP0, TPFON0	O	Twisted-Pair/Fiber Outputs, Positive & Negative - Ports 0-7. During 100BASE-TX or 10BASE-T operation, TPFO pins drive 802.3 compliant pulses onto the line. During 100BASE-FX operation, TPFO pins produce differential PECL outputs for fiber transceivers.
111, 110	111, 110	V20, V19	TPFOP1, TPFON1		
121, 122	121, 122	P19, P20	TPFOP2, TPFON2		
140, 139	125, 124	N20, N19	TPFOP3, TPFON3		
150, 151	136, 137	H19, H20	TPFOP4, TPFON4		
154, 153	140, 139	G20, G19	TPFOP5, TPFON5		
–, –	150, 151	C19, C20	TPFOP6, TPFON6		
–, –	154, 153	B20, B19	TPFOP7, TPFON7		
104, 105	104, 105	Y19, Y20	TPFIP0, TPFIN0	I	**Twisted-Pair/Fiber Inputs, Positive & Negative - Ports 0-7.** During 100BASE-TX or 10BASE-T operation, TPFI pins receive differential 100BASE-TX or 10BASE-T signals from the line. During 100BASE-FX operation, TPFI pins receive differential PECL inputs from fiber transceivers.
115, 114	115, 114	U20, U19	TPFIP1, TPFIN1		
118, 119	118, 119	R19, R20	TPFIP2, TPFIN2		
143, 142	129, 128	M20, M19	TPFIP3, TPFIN3		
146, 147	132, 133	J20, J19	TPFIP4, TPFIN4		
157, 156	143, 142	F20, F19	TPFIP5, TPFIN5		
–, –	146, 147	D19, D20	TPFIP6, TPFIN6		
–, –	157, 156	A20, A19	TPFIP7, TPFIN7		

1. Type Column Coding: I = Input, O = Output.
2. Ports 6 and 7 are available only on the LXT9782. These pins are not bonded out on the LXT9762.

Table 4. LXT97x2 JTAG Test Signal Descriptions

97x2[1] Pin# PQFP	9782 Pin# PBGA	Symbol	Type[2]	Signal Description
163	D14	TDI	I / IP	**Test Data Input**. Test data sampled with respect to the rising edge of TCK.
164	C15	TDO	O	**Test Data Output**. Test data driven with respect to the falling edge of TCK.
165	B16	TMS	I / IP	**Test Mode Select**.
166	D15	TCK	I / ID	**Test Clock**. Clock input for JTAG test (REFCLK).
167	A16	$\overline{\text{TRST}}$	I / IP	**Test Reset**. Reset input for JTAG test.

1. Pin numbers apply to both the LXT9762 and the LXT9782.
2. Type Column Coding: I = Input, O = Output, OD = Open Drain, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

Table 5. LXT97x2 Miscellaneous Signal Descriptions

97x2[1] Pin# PQFP	97x2[1] Pin# PBGA	Symbol	Type[2]	Signal Description[3]		
76 77	Y8 U10	TxSLEW_0 TxSLEW_1	I	**Tx Output Slew Controls 0 and 1**. These pins select the TX output slew rate (rise and fall time) as follows:		
				TxSLEW_1	TxSLEW_0	Slew Rate (Rise and Fall Time)
				0	0	2.5 ns
				0	1	3.1 ns
				1	0	3.7 ns
				1	1	4.3 ns
79	W10	PAUSE	I	**Pause**. Setting this pin High causes LXT97x2 to advertise Pause capabilities on all ports during auto-negotiation.		
82	W12	PWRDWN	I	**Power Down**. When High, forces LXT97x2 into Power-Down mode. This pin is OR'ed with the Power-Down bit (0.11). Refer to discussion on page 28 and to Table 38 on page 66 for more information.		
83	V12	$\overline{\text{RESET}}$	I	**Reset**. This active Low input is OR'ed with the control register Reset bit (0.15). When held Low, outputs are forced to inactive state.		

1. Pin numbers apply to both the LXT9762 and the LXT9782.
2. Type Column Coding: A = Analog, I = Input, O = Output, OD = Open Drain.
3. The LXT97x2 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 5. LXT97x2 Miscellaneous Signal Descriptions (Continued)

97x2[1] Pin#		Symbol	Type[2]	Signal Description[3]
PQFP	PBGA			
97 96 95 94 93	W16 V15 V13 V14 W15	ADD_4 ADD_3 ADD_2 ADD_1 ADD_0	I I I I I	**Address <4:0>**. Sets base address. Each port adds its port number (starting with 0) to this address to determine its PHY address. Port 0 Address = Base + 0. Port 1 Address = Base + 1. Port 2 Address = Base + 2. Port 3 Address = Base + 3. Port 4 Address = Base + 4. Port 5 Address = Base + 5. Port 6 Address = Base + 6 (LXT9782 Only). Port 7 Address = Base + 7 (LXT9782 Only).
102	V17	RBIAS	AI	**Bias**. This pin provides bias current for the internal circuitry. Must be tied to ground through a 22.1 kΩ 1% resistor.
206	B4	QSTAT	O	**Quick Status**. Provides for continuous PHY status updates, without the need for constant polling.
207	A3	QCLK	I	**Quick Clock**. Clock used for sending out QSTAT information. Maximum frequency is 25 MHz.

1. Pin numbers apply to both the LXT9762 and the LXT9782.
2. Type Column Coding: A = Analog, I = Input, O = Output, OD = Open Drain.
3. The LXT97x2 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 6. LXT97x2 Power Supply Signal Descriptions

97x2[1] Pin#		Symbol	Type	Signal Description
PQFP	PBGA			
80, 87, 88, 89, 179	A12, B11, B12, Y9, Y10, Y11, Y16, Y17	VCCD	–	**Digital Power Supply - Core.** +3.3V supply for core digital circuits.
15, 31, 52, 67, 193, 208	C4, D5, G1, M1, Y6, V1	VCCIO	–	**Digital Power Supply - I/O Ring.** +3.3V supply for digital I/O circuits. Regardless of the IO supply, digital I/O pins remain tolerant of 5V signal levels.
106, 113, 120, 127, 134, 141, 148, 155	D17, E17, H17, J17, M17, N17, T17, U17	VCCR	–	**Analog Power Supply.** +3.3V supply for all analog receive circuits.
LXT9762 and LXT9782: 112, 149	A18, B18, E19, E20, K19, K20, L19, L20, T19, T20, W18, Y18	VCCT	–	**Analog Power Supply.** +3.3V supply for all analog transmit circuits.
LXT9782 Only: 126, 135				
1, 16, 32, 48-51, 53, 68, 72-75, 81, 86, 91, 178, 192	A4, B2, B8, C12, D11, E4, G3, G4, J9 - J12, K9 - K12, L9 - L12, M3, M4, M9 - M12, T4, U5, U8, U11, V11, W5, W11, W13, Y13, Y14	GNDD	–	**Digital Ground.** Ground return for both core and I/O digital supplies (VCCD and VCCIO).

1. Unless otherwise noted, pin numbers apply to both the LXT9762 and the LXT9782.

Table 6. LXT97x2 Power Supply Signal Descriptions (Continued)

97x2[1] Pin#		Symbol	Type	Signal Description
PQFP	PBGA			
LXT9762 and LXT9782: 103, 109, 116, 117, 123, 138, 144, 145, 152, 158	C18, D16, D18, E18, F17, F18, G17, G18, H18, J18, K17, K18, L17, L18, M18, N18, P17, P18, R17, R18, T18, U16, U18, V18, W17	GNDA	–	**Analog Ground**. Ground return for analog supply. All ground pins can be tied together using a single ground plane.
LXT9782 Only: 130, 131				
78	V10	GNDS	–	**Substrate Ground.** Ground for chip substrate.

1. Unless otherwise noted, pin numbers apply to both the LXT9762 and the LXT9782.

Table 7. LXT97x2 LED Signal Descriptions

9762 Pin#	9782 Pin#		Symbol	Type[1]	Signal Description[2]
PQFP	PQFP	PBGA			
177	177	D12	LEDS_0	O	**Serial LEDs 0 - 7**. Each serial LED output indicates a particular status condition for every port. Bit 0 is assigned to Port 0, bit 1 is assigned to Port 1, etc. There are 8 possible LEDs per port, for a total of 48 display LEDs. However, typical equipment designs use no more than 3 LEDs per port, selected by the designer. Using per-event, rather than per-port outputs reduces the number of serial shift registers required. Instead of requiring an external serial-to-parallel shift register for each port, this method requires only one per LED type, reducing board space and component costs. Refer to "Serial LED Functions" on page 40 for details.
176	176	B13	LEDS_1		
175	175	C13	LEDS_2		
174	174	A14	LEDS_3		
173	173	A13	LEDS_4		
172	172	B14	LEDS_5		
171	171	C14	LEDS_6		
170	170	A15	LEDS_7		
168	168	B15	LEDCLK	O	**LED Clock.** 1 MHz clock for LED serial data output.
169	169	D13	LEDLATCH	O	**LED Latch.** Framing signal for serial LED outputs.
203 204 205	203 204 205	B5 D6 C5	LED/CFG0_1 LED/CFG0_2 LED/CFG0_3	I OD OS	**Port 0 LED Drivers 1 -3.** These pins drive LED indicators for Port 0. Each output indicates one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 75 for details). **Port 0 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 27 for details).
200 201 202	200 201 202	D7 A5 C6	LED/CFG1_1 LED/CFG1_2 LED/CFG1_3	I OD OS	**Port 1 LED Drivers 1 -3.** These pins drive LED indicators for Port 1. Each output indicates one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 75 for details). **Port 1 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 27 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain, OS = Open Source.
2. Ports 6 and 7 are available only on the LXT9782. These pins are not bonded out on the LXT9762.

Table 7. LXT97x2 LED Signal Descriptions (Continued)

9762 Pin#	9782 Pin#		Symbol	Type[1]	Signal Description[2]
PQFP	PQFP	PBGA			
197 198 199	197 198 199	C7 A6 B6	LED/CFG2_1 LED/CFG2_2 LED/CFG2_3	I OD OS	**Port 2 LED Drivers 1 -3.** These pins drive LED indicators for Port 2. Each output indicates one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 75 for details). **Port 2 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 27 for details).
186 187 188	194 195 196	A7 D8 B7	LED/CFG3_1 LED/CFG3_2 LED/CFG3_3	I OD OS	**Port 3 LED Drivers 1 -3.** These pins drive LED indicators for Port 3. Each output indicates one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 75 for details). **Port 3 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 27 for details).
183 184 185	189 190 191	C8 A8 D9	LED/CFG4_1 LED/CFG4_2 LED/CFG4_3	I OD OS	**Port 4 LED Drivers 1 -3.** These pins drive LED indicators for Port 4. Each output indicates one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 75 for details). **Port 4 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 27 for details).
180 181 182	186 187 188	D10 A9 B9	LED/CFG5_1 LED/CFG5_2 LED/CFG5_3	I OD OS	**Port 5 LED Drivers 1 -3.** These pins drive LED indicators for Port 5. Each output indicates one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 75 for details). **Port 5 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 27 for details).
– – –	183 184 185	A10 B10 C9	LED/CFG6_1 LED/CFG6_2 LED/CFG6_3	I OD OS	**Port 6 LED Drivers 1 -3.** These pins drive LED indicators for Port 6. Each output indicates one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 75 for details). **Port 6 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 27 for details).
– – –	180 181 182	C11 C10 A11	LED/CFG7_1 LED/CFG7_2 LED/CFG7_3	I OD OS	**Port 7 LED Drivers 1 -3.** These pins drive LED indicators for Port 7. Each output indicates one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 75 for details). **Port 7 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 27 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain, OS = Open Source.
2. Ports 6 and 7 are available only on the LXT9782. These pins are not bonded out on the LXT9762.

Table 8. Unused Pins

97x2 Pin#	9782 Pin#	Symbol	Type	Signal Description
PQFP	PBGA			
LXT9762 and LXT9782: 2, 5-7, 10-14, 19-21, 24-29, 34-36, 39-47, 56-58, 61-66, 69	A1,A2, B1, B3, C1, D1 - D3, E1, E3, F1 - F4, H1, H3, H4, J1, J3, J4, K2 - K4, L1, L2, L4, N1 - N3, P1, P3, P4, R1 - R4, T1 - T3, U1 - U4, U6, U7, U9, V3, V4, V6, V7, V9, W1, W3, W6, W7, W9, Y1 - Y5, Y7	N/C	–	**No Connection - LXT97x2**. These pins are not used on either the LXT9762 or LXT9782 and should not be connected.
LXT9762 Only: 98, 124 - 137, 162, 189 - 191, 194 - 196		N/C	–	**No Connection - LXT9762 Only**. These additional pins are not used on the LXT9762 and should not be connected.

2.0 Functional Description

2.1 Introduction

The LXT9782 eight-port Fast Ethernet 10/100 Transceiver supports 10 Mbps and 100 Mbps networks. It complies with all applicable requirements of IEEE 802.3. Each port directly drives either a 100BASE-TX line (up to 100 meters) or a 10BASE-T line (up to 185 meters). The LXT9782 also supports 100BASE-FX operation via a Pseudo-ECL (PECL) interface. The LXT9762 offers the same features and functionality in a six-port device. This data sheet uses the singular designation “LXT97x2” to refer to both devices.

2.1.1 OSP™ Architecture

Intel's LXT97x2 incorporates high-efficiency Optimal Signal Processing™ design techniques, combining the best properties of digital and analog signal processing to produce a truly optimal device.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). This improves receiver noise and cross-talk performance.

The OSP signal processing scheme requires substantially less computational logic than traditional DSP-based designs. This lowers power consumption and also reduces the logic switching noise generated by DSP engines clocked at speeds up to 125 MHz. Logic switching noise can be a considerable source of EMI generated on the device’s power supplies.

The OSP-based LXT97x2 provides improved data recovery, EMI performance, and power consumption.

2.1.2 Comprehensive Functionality

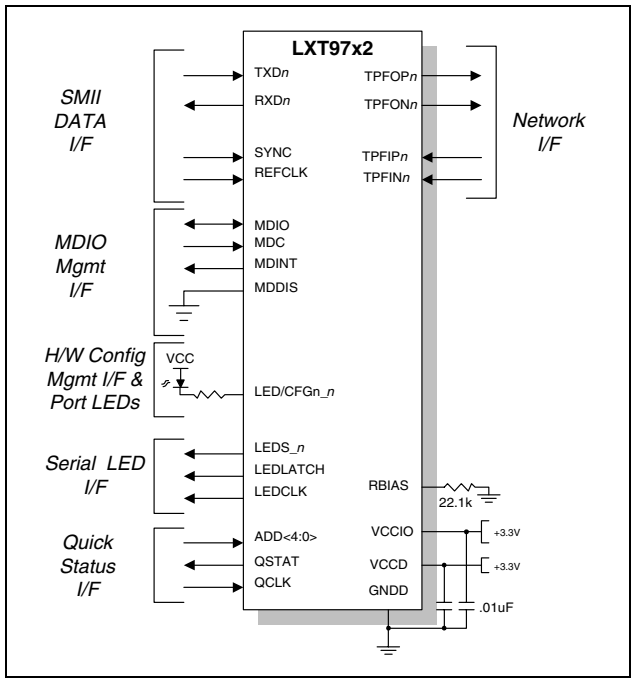
The LXT97x2 performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. This device also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

On power-up, the LXT97x2 reads its configuration pins to check for forced operation settings. If not configured for forced operation, each port uses auto-negotiation/parallel detection to automatically determine line operating conditions. The LXT97x2 provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

If the PHY device on the other side of the link supports auto-negotiation, the LXT97x2 will auto-negotiate with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT97x2 will automatically detect the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and set its operating conditions accordingly.

The LXT97x2 provides an individual serial MII (SMII) for each network port. The SMII ports provide for communication between the Media Access Controllers (MACs) and the network ports. The SMII bit stuffing protocol is automatically set once the network port operating conditions have been determined

Figure 5. LXT97x2 Interfaces



2.2 Interface Descriptions

2.2.1 10/100 Network Interface

The LXT97x2 supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX). Each network interface port consists of four external pins (two differential signal pairs). The pins are shared between twisted-pair (TP) and fiber. Refer to Table 2 on page 14 for specific pin assignments.

The LXT97x2 output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX PECL output. When not transmitting data, the LXT97x2 generates 802.3-compliant link pulses or idle code. Input signals are decoded either as a 100BASE-TX, 100-BASE-FX, or 10BASE-T input, depending on the mode selected. The interface speed is determined by auto-negotiation/parallel detection or manual control.

2.2.1.1 Twisted-Pair Interface

When operating at 100 Mbps, the LXT97x2 continuously transmits and receives MLT3 symbols. When not transmitting data, the LXT97x2 generates “IDLE” symbols.

During 10 Mbps operation, Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state.

The LXT97x2 supports either 100BASE-TX or 10BASE-T connections over 100Ω, Category 5, Unshielded Twisted Pair (UTP) cable. Only a transformer, RJ-45 connector, load resistor, and bypass capacitors are required to complete this interface. On the receive side, the internal impedance is high enough that it has no practical effect on the external termination circuit. On the transmit side, Intel's patented waveshaping technology shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings (refer to Table 5 on page 15) allow the designer to match the output waveform to the magnetic characteristics.

2.2.1.2 Fiber Interface

The LXT97x2 provides a PECL interface suitable for driving a fiber-optic coupler. The PECL interface complies with the ANSI X3.166 specification.

Fiber ports cannot be enabled via auto-negotiation; they must be enabled via the Hardware Control Interface or MDIO registers.

2.2.2 SMII Data Interface

The LXT97x2 provides six or eight independent SMII ports with a common reference clock and SYNC signal, as well as an MDIO management interface. The SMII Data Interface exchanges data between the LXT97x2 and up to eight Media Access Controllers (MACs).

2.2.3 Configuration Management Interface

The LXT97x2 provides both a Hardware Control Interface (via the LED/CFG pins) and an MDIO interface for device configuration and management.

2.2.3.1 Hardware Control Interface

The LXT97x2 provides a Hardware Control Interface for applications where the MDIO is not desired. The Hardware Control Interface uses the three LED driver pins for each port. Refer to the discussion in the Initialization section for additional details.

2.2.3.2 MDIO Management Interface

The LXT97x2 supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the LXT97x2. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers. Some registers are required and their functions are defined by the IEEE 802.3 specification. Additional registers allow for expanded functionality.

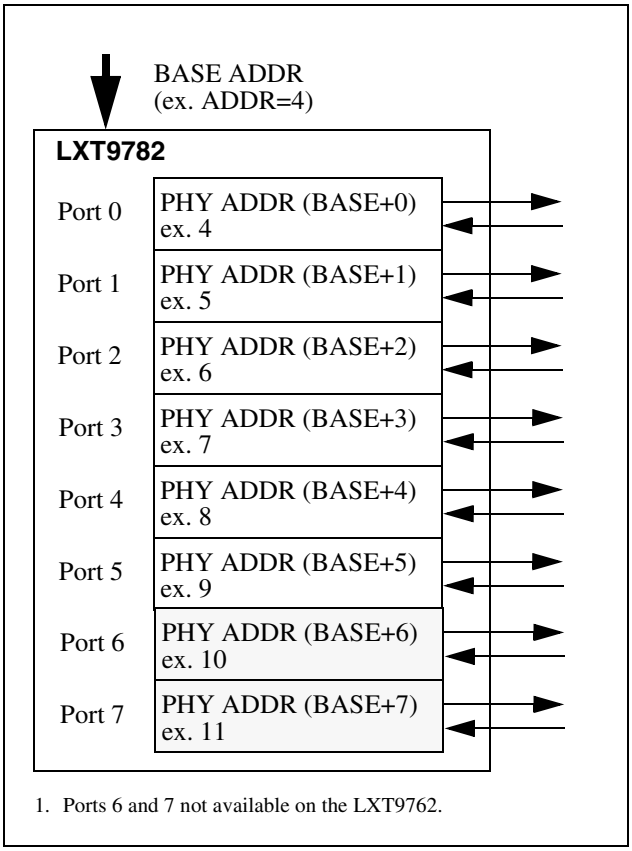
Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-32) and Y is the bit number (0-15).

The physical interface consists of a data line (MDIO) and clock line (MDC). Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, the MDIO read and write operations are disabled and the Hardware Control Interface provides primary configuration control. When MDDIS is Low, the MDIO port is enabled for both read and write operations and the Hardware Control Interface is not used. The timing for the MDIO Interface is shown in Table 33 on page 61. MDIO read and write cycles are shown in Figure 7 (read) and Figure 8 (write).

MII Addressing

The protocol allows one controller to communicate with multiple LXT97x2 chips. Pins ADD_<4:0> determine the base address. Each port adds its port number (0 through *n*) to the base address to obtain its port address as shown in Figure 6.

Figure 6. Port Address Scheme



1. Ports 6 and 7 not available on the LXT9762.

Figure 7. Management Interface Read Frame Structure

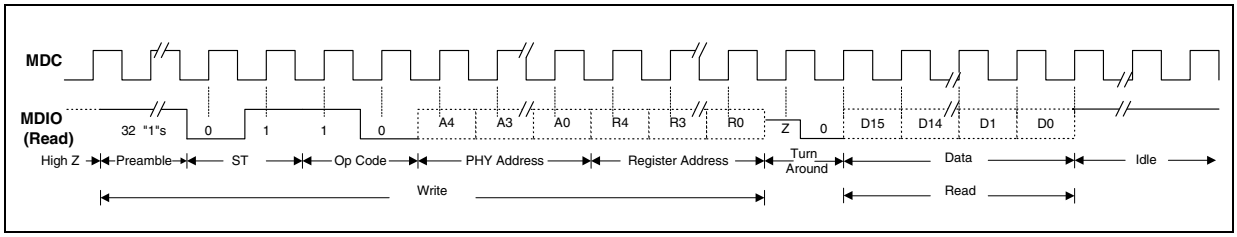
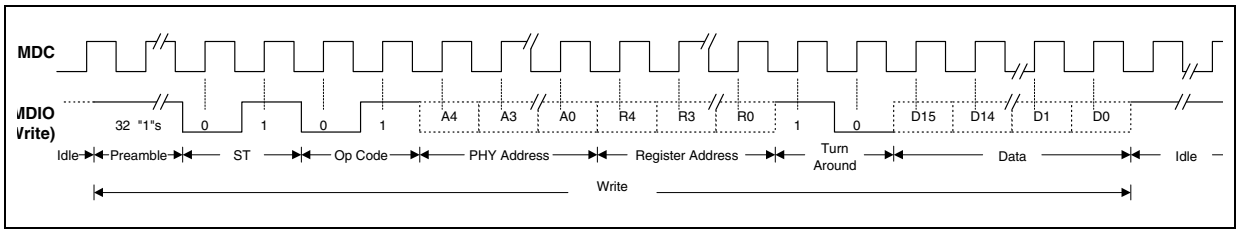


Figure 8. Management Interface Write Frame Structure



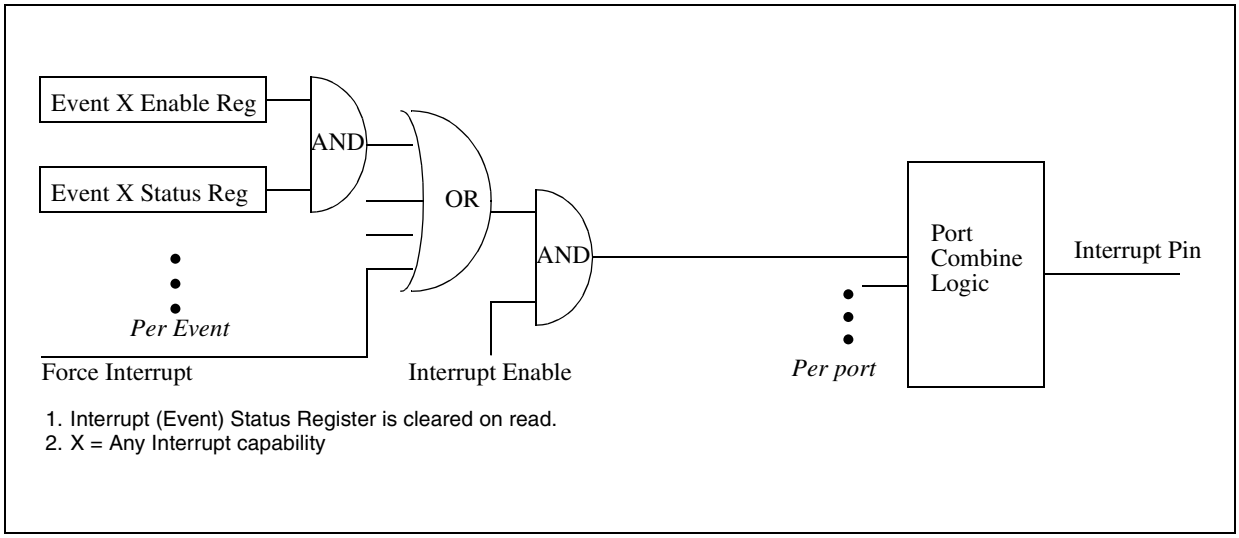
MII Interrupts

The LXT97x2 provides a single interrupt pin available to all ports. Interrupt logic is shown in Figure 9. The LXT97x2 also provides two dedicated interrupt registers for each port. Register 18 (Table 49 on page 73) provides interrupt enable and mask functions and Register 19 (Table 50 on page 74) provides interrupt status. Setting bit 18.1 = 1, enables a port to request interrupt via the $\overline{\text{MDINT}}$ pin. An active Low on this pin indicates a status change on the LXT97x2. However, because it is a shared interrupt, it does not indicate which port is requesting service.

Interrupts may be caused by five conditions:

- Receive Monitor counter full
- Auto-negotiation complete
- Speed status change
- Duplex status change
- Link status change

Figure 9. Interrupt Logic



2.3 Operating Requirements

2.3.1 Power Requirements

The LXT97x2 requires four power supply inputs, VCCD, VCCR, VCCT and VCCIO. The digital and analog circuits require 3.3 V supplies (VCCD, VCCR and VCCT). These inputs may be supplied from a single source although decoupling is required to each respective ground.

An additional supply may be used for the SMII (VCCIO). VCCIO should be supplied from the same power source used to supply the controller on the other side of the SMII interface. Refer to Table 20 on page 54 for the SMII I/O characteristics.

As a matter of good practice, these supplies should be as clean as possible. Typical filtering and decoupling are shown in Figure 23 on page 49.

2.3.2 Clock Requirements

2.3.2.1 Reference Clock

The LXT97x2 requires a constant 125 MHz reference clock (REFCLK). The reference clock is used to generate transmit signals and recover receive signals. A crystal-based clock is recommended over a derived clock (i.e, PLL-based) to minmize transmit jitter. Refer to Table 21 on page 54 for clock timing requirements.

2.3.2.2 SYNC Signal

The LXT97x2 requires a 12.5 MHz input pulse for SMII synchronization. See"SYNC Pulse" on page 31

2.3.2.3 Serial LED Clock

The LXT97x2 requires a 1 MHz clock input to synchronize the serial LED output.

2.3.2.4 Quick Status Clock

The LXT97x2 requires a clock input (up to 25 MHz) to synchronize the Quick Status output.

2.4 Initialization

When the LXT97x2 is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link. The configuration bits may be set by the Hardware Control Interface pins or by an MDIO write operation as shown in Figure 10.

The following modes are available using either Hardware Control or MDIO Control:

- Force network link to 100FX (Fiber).
- Force network link operation to:
  - 100TX, Full-Duplex

— 100TX, Half-Duplex

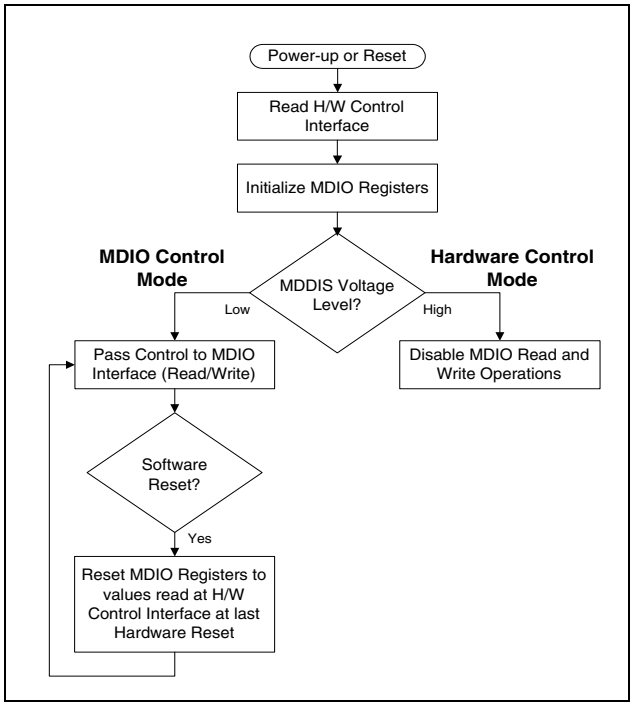
— 10BASE-T, Full-Duplex

— 10BASE-T, Half-Duplex

- Allow auto-negotiation / parallel-detection.

When the network link is forced to a specific configuration, the LXT97x2 immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT97x2 begins the auto-negotiation / parallel-detection operation.

Figure 10. Initialization Sequence



2.4.1 Hardware Configuration Settings

The LXT97x2 provides a hardware option to set the initial device configuration. The LED/CFG drivers can operate as either open drain or open source circuits as shown in Figure 11. This provides three control bits per port, as listed in Table 9. In applications where all ports configured the same, several pins may be tied together with a single resistor.

Figure 11. Hardware Control Settings

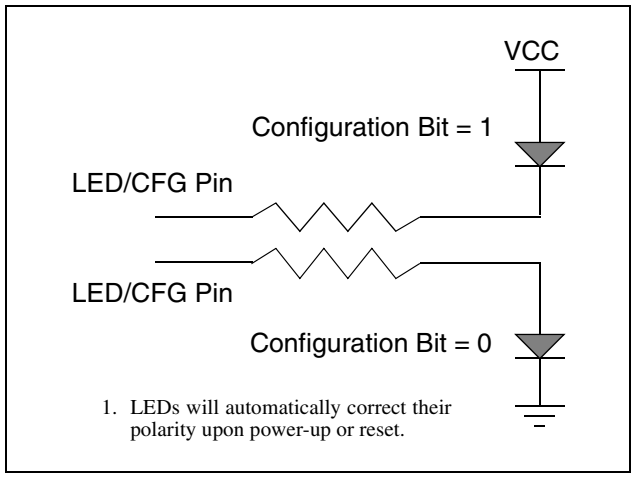


Table 9. Hardware Configuration Settings

Desired Configuration			Pin Settings			Resulting Register Bit Values						
			LED/CFG*n*_[1]			Control Register			AN Advertisement Register			
AutoNeg Mode	Speed Mode	Duplex Mode	1	2	3	AutoNeg 0.12	Speed 0.13	FD 0.8	100FD 4.8	100TX 4.7	10 FD 4.6	10T 4.5
Disabled	10	Half	0	0	0	0	0	0	X X X X [2] Auto-Negotiation Advertisement			
		Full	0	0	1			1				
	100	Half	0	1	0		1	0				
		Full	0	1	1			1				
Enabled[3]	100	Half	1	0	0	1	1	0	0	1	0	0
		Full	1	0	1			1	1			
	10/100	Half	1	1	0			0	0		0	1
		Full	1	1	1			1	1		1	

1. These pins set the default values for registers 0 and 4 accordingly.
2. X = Don't Care.
3. Do not select Fiber mode with Auto-Negotiation enabled.

2.4.2 Reset

The LXT97x2 provides both hardware and software resets. Configuration control of Auto-Negotiation, speed and duplex mode selection is handled differently for each. During a hardware reset, settings for bits 0.13, 0.12 and 0.8 are read in from the pins (refer to Table 38 on page 66).

During a software reset (0.15 = 1), these bit settings are not re-read from the pins. They revert back to the values that were read in during the last hardware reset. Therefore, any changes to pin values made since the last hardware reset will not be detected during a software reset.

During a hardware reset, register information is unavailable for 1 ms after de-assertion of the reset. During a software reset (0.15 = 1) the registers are available for reading. The reset bit should be polled to see when the part has completed reset (0.15 = 0).

2.4.3 Power-Down Mode

The LXT97x2 offers both global and per-port power-down modes.

2.4.3.1 Global (Hardware) Power Down

The global power-down mode is controlled by PWRDWN pin 82 (PQFP) or pin W12 (PBGA). When PWRDWN is High, the following conditions are true:

- All LXT97x2 ports and clock are shut down.
- All outputs are tri-stated.
- All weak pad pull-up and pull-down resistors are disabled.
- The MDIO registers are not accessible.
- The MDIO registers are reset after power down.

2.4.3.2 Port Power Down

Individual port power-down control is provided by bit 0.11 in the respective port Control Registers (refer to Table 38 on page 66). During individual port power-down, the following conditions are true:

- The individual port is shut down.
- The MDIO registers remain accessible.
- The MDIO registers are unaffected.

2.5 Link Establishment

2.5.1 Auto-Negotiation

The LXT97x2 attempts to auto-negotiate with its counter-part across the link by sending Fast Link Pulse (FLP) bursts. Each burst consists of 33 link pulses spaced 62.5 µs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may be present or absent to indicate a “1” or a “0”. Each FLP burst exchanges 16 bits of data, which are referred to as a “page”. All devices that support auto-negotiation must implement the “Base Page” defined by IEEE 802.3 (Registers 4 and 5). LXT97x2 also supports the optional ‘Next Page’ function (Registers 7 and 8).

2.5.1.1 Base Page Exchange

By exchanging Base Pages, the LXT97x2 and its link partner communicate their capabilities to each other. Both sides must receive at least three identical base pages for negotiation to proceed. Each side finds the highest common capabilities that both sides support. Both sides then exchange more pages, and finally agree on the operating state of the line.

2.5.1.2 Next Page Exchange

Additional information, above that required by base page exchange is also sent via “Next Pages’. The LXT97x2 fully supports the 802.3 method of negotiation via Next Page exchange.

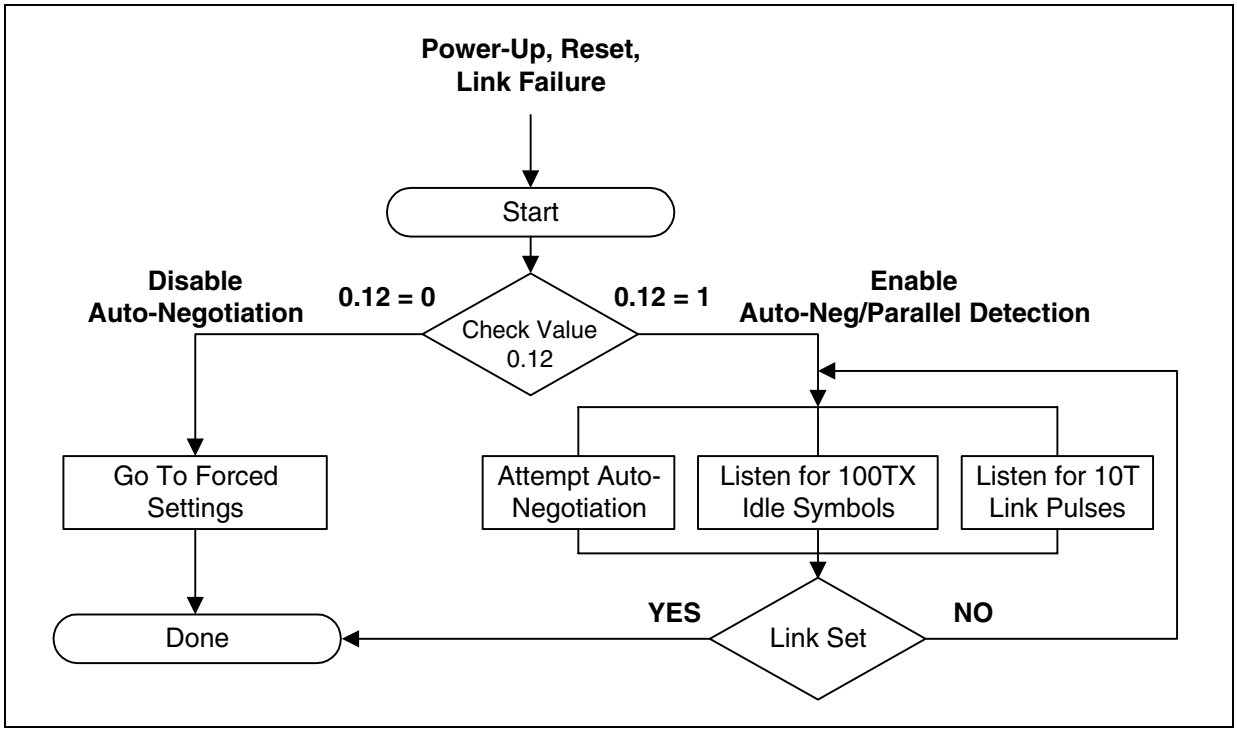
2.5.1.3 Controlling Auto-Negotiation

When auto-negotiation is controlled by software, the following steps are recommended:

- After power-up, power-down, or reset, the power-down recovery time, as specified in Table 34 on page 62, must be exhausted before proceeding.
- Set the auto-negotiation advertisement register bits.
- Enable auto-negotiation (set MDIO bit 0.12 = 1).

Do not enable Auto-Negotiation if fiber mode is selected.

Figure 12. Link Establishment Process



2.5.2 Parallel Detection

In parallel with auto-negotiation, the LXT97x2 also monitors for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either is detected, the device automatically reverts to the corresponding operating mode. Parallel detection allows the LXT97x2 to communicate with devices that do not support auto-negotiation.

2.6 Serial MII Operation

The LXT97x2 exchanges transmit and receive data with the controller via the Serial MII (SMII). The SMII performs the following functions:

- Conveys complete MII information between a 10/100 PHY and MAC with two pins per port.

- Allows a multi-port MAC/PHY communication with one system clock.
- Operates in both half and full duplex.
- Supports per-packet switching between 10 Mbps and 100 Mbps data rates.

The Serial MII operates at 125 MHz using a global reference clock and frame synchronization signal (REFCLK and SYNC). Each port has an individual two-line data interface (TXD*n* and RXD*n*). All signals are synchronous to REFCLK. Figure 13 is a simple SMII block diagram and Table 10 summarizes the SMII signals.

Data is exchanged in 10-bit serial words. Each word contains one data byte (two nibbles of 4B coded data) and two status bits. When the port is operating at 100 Mbps, each word contains a new data byte. When the port is operating at 10 Mbps, each data byte is repeated 10 times.

Table 10. SMII Signal Summary

Signal	To	From	Purpose
TXD	PHY	MAC	Receive data & control
RXD	MAC	PHY	Transmit data & control
SYNC	PHY	MAC	Synchronization
REFCLK	MAC & PHY	System	Synchronization

1. Refer to Table 1 on page 13 for detailed signal descriptions.

Figure 13. Simplified SMII Application Diagram

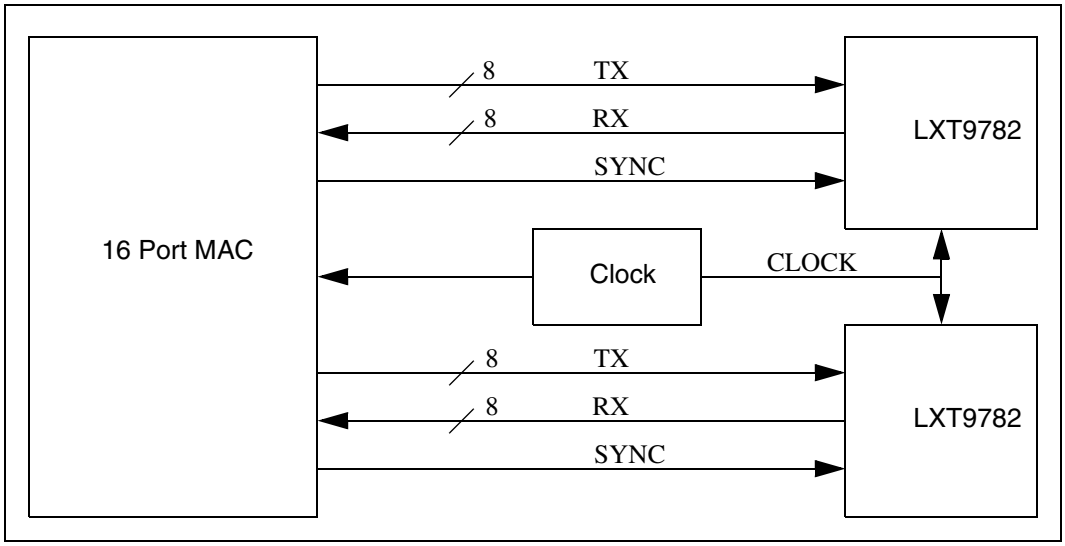
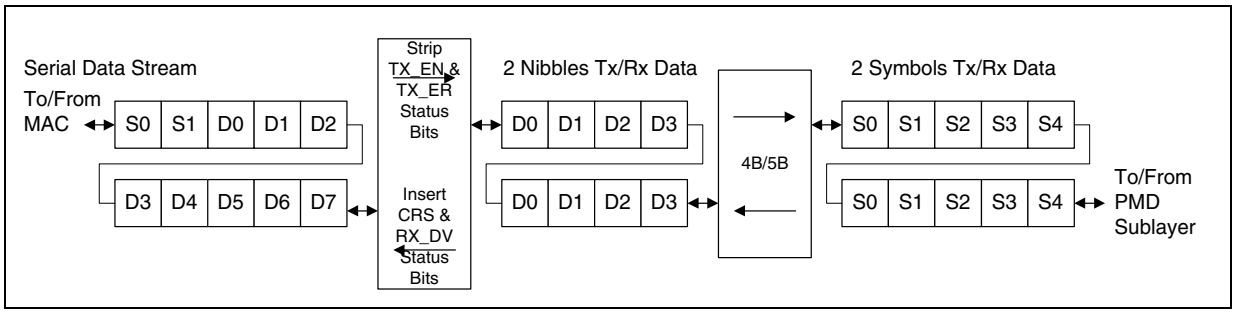


Figure 14. 100Mbps Serial MII Data Flow



2.6.1 Reference Clock

REFCLK operates at 125 MHz. The transmit and receive data and control streams must always be synchronized to REFCLK by the MAC and PHY. The LXT97x2 samples these signals on the rising edge of REFCLK.

2.6.2 SYNC Pulse

The SYNC pulse delimits segment boundaries and synchronizes with REFCLK. The MAC must continuously generate a SYNC pulse once every 10 REFCLK cycles. The SYNC pulse signals the start of each new segment as shown in Figure 15 and Figure 17.

2.6.3 Transmit Data Stream

Transmit data and control information are signalled in ten bit segments. In 100 Mbps mode each segment contains a new byte of data. In 10 Mbps mode the MAC must repeat a 10M serial word on TXD ten times. LXT97x2 may sample that serial word at any point.

The SYNC pulse signals the start of a new segment as shown in Figure 15.

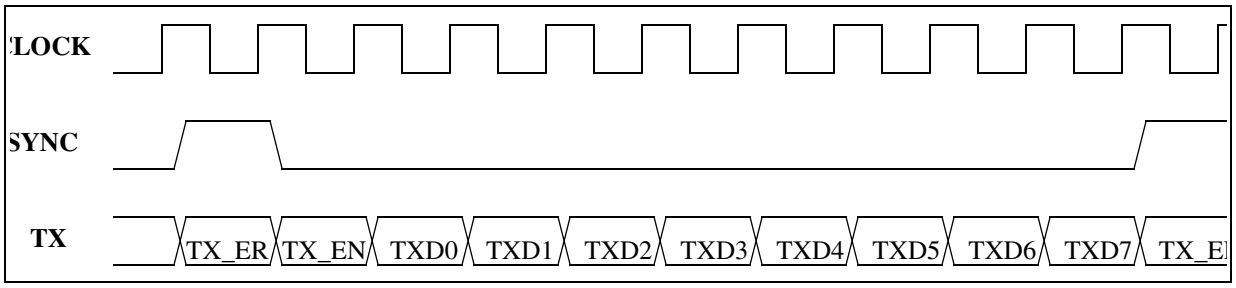
2.6.3.1 Transmit Enable

The MAC must assert the TX_EN bit in each segment of TXData, and de-assert TX_EN*n* after the last segment of the packet.

2.6.3.2 Transmit Error

In 100BASE-x mode when the MAC asserts the TX_ER bit, the LXT97x2 will drive “H” symbols onto the network interface. TX_ER does not have any function in 10M operation.

Figure 15. Serial MII Transmit Synchronization



2.6.4 Receive Data Stream

Receive data and control information are signalled in ten bit segments. In 100 Mbps mode each segment contains a new byte of data. In 10 Mbps mode each segment is repeated ten times (except for the CRS bit) and the MAC can sample any one of the ten segments.

2.6.4.1 Carrier Sense

The CRS bit (slot 0) is generated when a packet is received from the network interface. The CRS bit is set in real time, even in 10 Mbps mode. (All other bits are repeated in 10 sequential segments).

2.6.4.2 Receive Data Valid

The LXT97x2 asserts the RX_DV bit (slot 1) when it receives a valid packet. The assertion timing changes depend on line operating speed:

- For 100TX and 100FX links, the RX_DV bit is asserted from the first nibble of preamble to the last nibble of the data packet.
- For 10BT links, the entire preamble is truncated. The RX_DV bit is asserted with the first nibble of the Start-of-Frame Delimiter (SFD) “5D” and remains asserted until the end of the packet.

2.6.4.3 Receive Error

In 100BASE-X mode when the LXT97x2 receives an errored symbol from the network, it drives “1110” on the associated RXD pin.

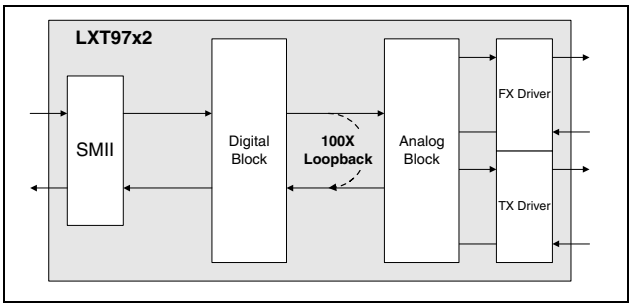
2.6.4.4 Receive Status Encoding

The LXT97x2 encodes status information onto the RXD line during IPG as listed in Table 11 on page 33. Status bit RXD<5> indicates the validity of the upper nibble (RXD<7:4> of the last byte of the previous frame). RXD and RX_DV are passed through the internal elasticity FIFO to smooth any clock rate differences between the recovered clock and the 125 MHz reference clock.

2.6.5 Loopback

A test loopback function is available for 100 Mbps SMII testing. Bit 0.14 must be set High for correct operation. When data is looped back, whatever the MAC transmits is looped back in its entirety, including the preamble. In FX mode, the respective SD/$\overline{\text{TPn}}$ pin must be pulled High to enable loopback.

Figure 16. Loopback Paths



2.6.6 Collision

The SMII interface does not provide a collision output and relies on the MAC to interpret COL conditions using CRS and TX_EN. CRS is unaffected by the transmit path.

Figure 17. Serial MII Receive Synchronization

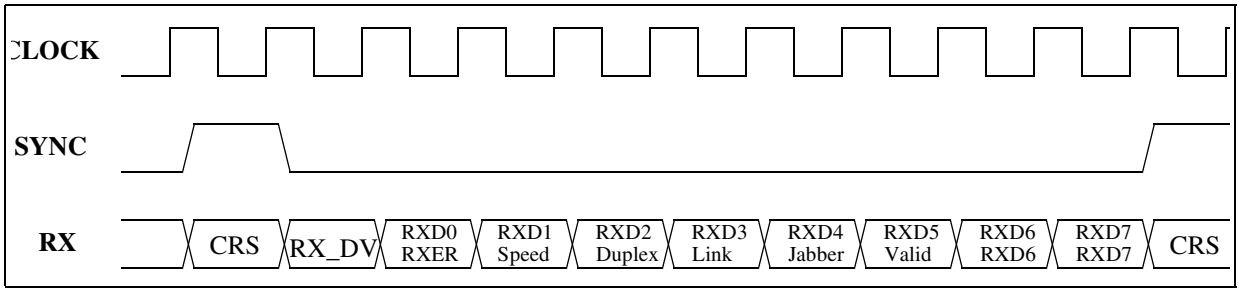


Table 11. RX Status Encoding Bit Definitions

Signal	Definition	
CRS	Carrier Sense - identical to MII, except that it is not an asynchronous signal.	
RX_DV	Receive Data Valid - identical to MII. When RX_DV = 0, status information is transmitted to the MAC. When RX_DV = 1, received data is transmitted to the MAC.	0 = Status Byte 1 = Valid Data Byte
RX_ER (RXD0)	Inter-frame status bit RXD0 indicates whether or not the PHY detected an error somewhere in the previous frame.	0 = No Error 1 = Error
SPEED (RXD1)	Inter-frame status bit RXD1 indicates port operating speed.	0 = 10Mbps 1 = 100Mbps
DUPLEX (RXD2)	Inter-frame status bit RXD2 indicates port duplex condition.	0 = Half 1 = Full
1. Both RXD0 and RXD5 bits are valid in the segment immediately following a frame, and remain valid until the first data segment of the next frame begins.		

Table 11. RX Status Encoding Bit Definitions (Continued)

Signal	Definition	
LINK (RXD3)	Inter-frame status bit RXD3 indicates port link status.	0 = Down 1 = Up
JABBER (RXD4)	Inter-frame status bit RXD4 indicates port jabber status.	0 = OK 1 = Error
VALID (RXD5)	Inter-frame status bit RXD5 conveys the validity of the upper nibble of the last byte of the previous frame.	0 = Invalid 1 = Valid
RXD)	Reserved	Ignore
RXD7	This bit is set to 1.	Always = 1
1. Both RXD0 and RXD5 bits are valid in the segment immediately following a frame, and remain valid until the first data segment of the next frame begins.		

2.7 100 Mbps Operation

2.7.1 100BASE-X Network Operations

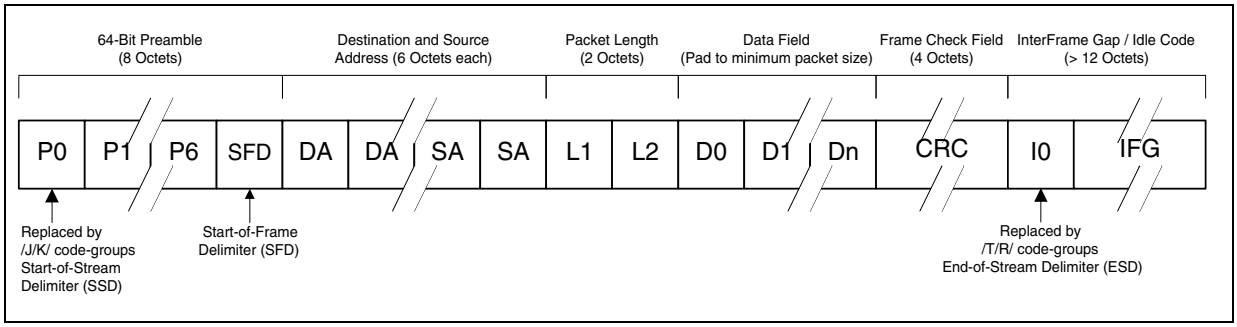
During 100BASE-X operation, the LXT97x2 transmits and receives 5-bit symbols across the network link. Figure 18 shows the structure of a standard frame packet. When the MAC is not actively transmitting data, the LXT97x2 sends out Idle symbols on the line.

In 100TX mode, the LXT97x2 scrambles the data and transmits it to the network using MLT-3 line code. The MLT-3 signals received from the network are descrambled and decoded and sent across the MII to the MAC.

In 100FX mode, the LXT97x2 transmits and receives NRZI signals across the PECL interface. An external 100FX transceiver module is required to complete the fiber connection.

As shown in Figure 18, the MAC starts each transmission with a preamble pattern. As soon as the LXT97x2 detects the start of preamble, it transmits a J/K Start-of-Stream Delimiter (SSD) symbol to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the Start-of-Frame Delimiter (SFD), packet data, and CRC. Once the packet ends, the LXT97x2 transmits the T/R End-of-Stream Delimiter (ESD) symbol and then returns to transmitting Idle symbols.

Figure 18. 100BASE-X Frame Format



2.7.2 .100BASE-X Protocol Sublayer Operations

With respect to the 7-layer communications model, the LXT97x2 is a Physical Layer 1 (PHY) device. The LXT97x2 implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) sublayers of the reference model defined by the IEEE 802.3u specification. The following paragraphs discuss LXT97x2 operation from the reference model point of view.

2.7.2.1 PCS Sublayer

The Physical Coding Sublayer (PCS) provides the MII interface, as well as the 4B/5B encoding/ decoding function described in Table 12 on page 36.

For 100TX and 100FX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TX_EN is de-asserted.

For 10T operation, the PCS layer merely provides a bus interface and serialization/de-serialization function. 10T operation does not use the 4B/5B encoder.

Preamble Handling

When the MAC asserts TX_EN, the PCS substitutes a /J/K symbol pair, also known as the Start-of-Stream Delimiter (SSD), for the first two nibbles received across the MII. The PCS layer continues to encode the remaining MII data according to the 4B/5B coding rules until TX_EN is de-asserted. It then returns to supplying IDLE symbols to the line driver.

In the receive direction, the PCS layer performs the opposite function, substituting two preamble nibbles for the SSD.

Dribble Bits

The LXT97x2 handles dribbles bits in all modes. If between 1-4 dribble bits are received, the nibble is passed across the SMII, padded with 1s if necessary. If between 5-7 dribble bits are received, the second nibble is not sent onto the SMII bus.

Figure 19. Protocol Sublayers

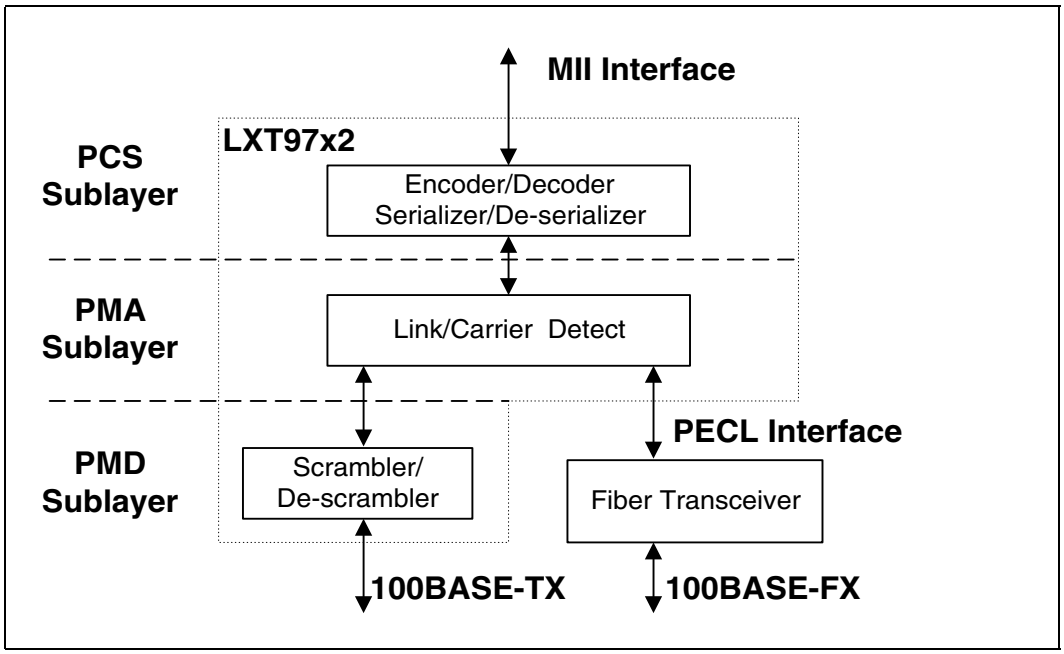


Table 12. 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
DATA	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

Table 12. 4B/5B Coding (Continued)

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 11	Idle. Used as inter-stream fill code
	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
CONTROL	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (ESD), part 1 of 2
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (ESD), part 2 of 2
	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	undefined	Invalid	0 0 0 0 0	Invalid
	undefined	Invalid	0 0 0 0 1	Invalid
INVALID	undefined	Invalid	0 0 0 1 0	Invalid
	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 0 1 1 0	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

2.7.2.2 PMA Sublayer

Link

In 100 Mbps mode, the LXT97x2 establishes a link whenever the scrambler becomes locked and remains locked for approximately 50 ms. If the scrambler loses lock (<12 consecutive idle symbols during a 2 ms window), the link is taken down. This provides a very robust link, essentially filtering out any small noise hits that may otherwise disrupt the link. Furthermore, 100M idle patterns do not bring up a 10M link.

The LXT97x2 reports link failure via the MII status bits (1.2, 17.10, and 19.4) and interrupt functions. If auto-negotiate is enabled, link failure causes the LXT97x2 to re-negotiate.

Link Failure Override

The LXT97x2 normally transmits 100 Mbps data packets or Idle symbols only when the link is up, and transmits only FLP bursts when the link is not up. Setting bit 16.14 = 1 overrides this function, allowing the LXT97x2 to transmit data packets even when the link is down. This feature is provided as a diagnostic tool. Note that auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT97x2 automatically begins transmitting FLP bursts if the link goes down.

Carrier Sense

For 100TX and 100FX links, a Start-of-Stream Delimiter (SSD) or /J/K symbol pair causes assertion of carrier sense (CRS). An End-of-Stream Delimiter (ESD), or /T/R symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R; however, in this case the RX_ER bit in the RX Status Frame is asserted for one clock cycle when CRS is de-asserted.

- For 10T links, CRS assertion is based on reception of valid preamble, and de-assertion on reception of an End-of-Frame (EOF) marker.

Receive Data Valid

The LXT97x2 asserts the RX_DV bit when it receives a valid packet. However, RXD outputs zeros until the received data is decoded and available for transfer to the controller.

2.7.2.3 Twisted-Pair PMD Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides signal scrambling and descrambling, line coding and decoding (MLT-3 for 100TX, Manchester for 10T), as well as receiving, polarity correction, and baseline wander correction functions.

Scrambler/Descrambler (100TX Only)

The scrambler spreads the signal power spectrum and reduces EMI using an 11-bit, non-data-dependent polynomial. The receiver automatically decodes the polynomial whenever IDLE symbols are received.

The scrambler/descrambler can be bypassed by setting bit 16.12 = 1. The scrambler is automatically bypassed when the fiber interface is enabled. Scrambler bypass provides diagnostic and test support.

Baseline Wander Correction

The LXT97x2 provides a baseline wander correction function, making the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition “unbalanced”. This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander can cause receiver errors, particularly in less robust designs, at long line lengths (100 meters). The exact characteristics of the wander are completely data dependent.

The LXT97x2 baseline wander correction characteristics allow the LXT97x2 to recover error-free data while receiving worst-case “killer” packets over all cable lengths.

Polarity Correction

The LXT97x2 automatically detects and corrects for receive signal (TPIP/N) inversion. Reversed polarity is detected if eight inverted link pulses, or four inverted EOF markers, are received consecutively. If link pulses or data are not received by the maximum receive time-out period, the polarity converter resets to a non-inverted state.

Fiber PMD Sublayer

The LXT97x2 provides a PECL interface for connection to an external fiber-optic transceiver. (The external transceiver provides the PMD function for fiber media.) The LXT97x2 uses an NRZI format for the fiber interface. The fiber interface operates at 100 Mbps and does not support 10FL applications.

Far End Fault Indications

The LXT97x2 Signal Detect pins receive signal fault indications from local fiber transceivers via the SD pins. The device can also detect far end fault code in the received data stream. The LXT97x2 "ORs" both fault conditions to set bit 1.4. Bit 1.4 is set once and clears when read.

Either fault condition causes the LXT97x2 to drop the link unless Forced Link Pass is selected (16.14 = 1). Link down condition is then reported via interrupts and status bits.

In response to locally detected signal faults (SD activated by the local fiber transceiver), the affected port can transmit the far end fault code if fault code transmission is enabled by bit 16.2.

- When bit 16.2 = 1, transmission of the far end fault code is enabled. The LXT97x2 transmits far end fault code if fault conditions are detected by the Signal Detect pins.
- When bit 16.2 = 0, the LXT97x2 does not transmit far end fault code. It continues to transmit idle code and may or may not drop link depending on the setting for bit 16.14.

2.8 10 Mbps Operation

The LXT97x2 operates as a standard 10BASE-T transceiver. Data transmitted by the MAC is Manchester-encoded, and transmitted on the TPOP/N outputs. Received data is decoded and passed to the MAC. The LXT97x2 supports all the standard 10 Mbps functions.

During 10BASE-T (10T) operation, the LXT97x2 transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the LXT97x2 sends out link pulses on the line.

In 10T mode, the polynomial scrambler/descrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT97x2 and sent across the MII to the MAC.

The LXT97x2 does not support fiber connections at 10 Mbps.

2.8.1 10T Preamble Handling

The LXT97x2 offers two options for preamble handling, selected by bit 16.5. In 10T Mode when 16.5 = 0, the LXT97x2 strips the entire preamble off of received packets. CRS is asserted coincident with SFD. RX_DV is held Low for the duration of the preamble. When RX_DV is asserted, the very first two nibbles driven by the LXT97x2 are the SFD “5D” hex followed by the body of the packet.

In 10T mode with 16.5 = 1, the LXT97x2 passes the preamble through the MII and asserts RX_DV and CRS simultaneously. In 10T loopback, the LXT97x2 loops back whatever the MAC transmits to it, including the preamble.

2.8.2 10T Dribble Bits

The LXT97x2 device handles dribbles bits in all modes. If between 1-4 dribble bits are received, the nibble is passed across the SMII, padded with 1s if necessary. If between 5-7 dribble bits are received, the second nibble is not sent onto the SMII bus.

2.8.3 10T Link Test

In 10T mode, the LXT97x2 always transmit link pulses. If the Link Test function is enabled, it monitors the connection for link pulses. Once link pulses are detected, data transmission is enabled and remains enabled as long as either the link pulses or data transmission continue. If the link pulses stop, data transmission is disabled.

If the Link Test function is disabled, the LXT97x2 transmits to the connection regardless of detected link pulses. Link Test can be disabled by setting bit 16.14 = 1.

2.8.3.1 Link Failure

Link failure occurs if Link Test is enabled and no link pulses or packets are received. If this condition occurs, the LXT97x2 returns to the link establishment mode selected at initialization.

2.8.4 10T Jabber

If a transmission exceeds the jabber timer, the LXT97x2 disables the transmit and loopback functions. The LXT97x2 automatically exits jabber mode after the unjab time has expired. The jabber timer can be disabled by setting bit 16.10 = 1.

2.9 Monitoring Operations

2.9.1 Serial LED Functions

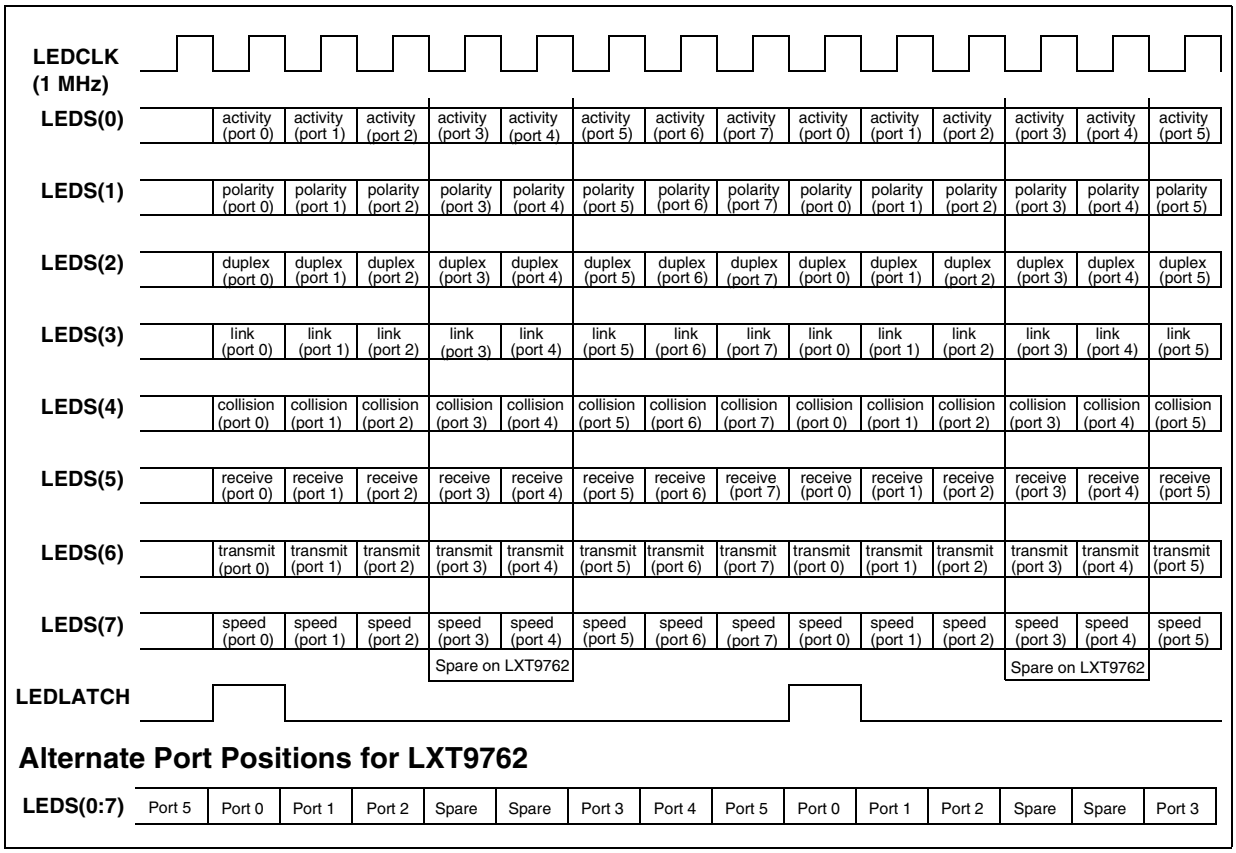
The LXT97x2 provide eight serial LED outputs (LEDS7:0) which may be attached to external HC595-type shift registers (refer to Figure 26 on page 52). The LEDCLK signal is used to shift data into the 595’s internal shift register. The LEDLATCH signal is used to latch data from the 595’s internal shift register to the 595’s internal storage register. The LXT97x2 drives the LEDS*n* and LEDLATCH outputs on the falling edge of LEDCLK. All serial LEDs will be stretched in accordance with bits 20.1 and 20.3:2.

Each serial output reports a specific status condition for all ports. Ports 0 through 7 are assigned bits 0:7 in each stream (bits 3 and 4 are not used on the LXT9762).

The serial outputs report the following conditions for each port:

- LEDS0 Serial Output indicates Activity
  0 = Active1 = Inactive
- LEDS1 Serial Output indicates Polarity (10 Mbps)
  0 = Switched Polarity1 = Normal Polarity
- LEDS2 Serial Output indicates Duplex (D)
  0 = Full Duplex1 = Half Duplex
- LEDS3 Serial Output indicates Link
  0 = Link active1 = Link inactive
- LEDS4 Serial Output indicates Collision
  0 = Collision active1 = Collision inactive
- LEDS5 Serial Output indicates Receive
  0 = Receive active1 = Receive inactive
- LEDS6 Serial Output indicates Transmit
  0 = Transmit active1 = Transmit inactive
- LEDS7 Serial Output indicates Speed
  0 = 100 Mbps1 = 10 Mbps

Figure 20. Serial LED Streams



2.9.2 Per-Port LED Driver Functions

The LXT97x2 incorporates three direct drive LEDs per port. On power up, all the LEDs outputs are asserted for approximately 1 second after Reset is de-asserted. Each LED driver can be programmed to indicate one of several status conditions using the LED Configuration Register. Each per-port LED can be programmed (refer to Table 51 on page 75) to indicate one the following conditions:

- Operating Speed
- Transmit Activity
- Receive Activity
- Collision Condition
- Link Status
- Duplex Mode

The LEDs can also be programmed to display various combined status conditions. For example, setting bits 20.15:12 = 1101 produces the following combination of Link and Activity indications:

- If Link is down LED is off.
- If Link is up LED is on.

- If Link is up AND activity is detected, the LED blinks at the stretch interval selected by bits 20.3:2 and continues to blink as long as activity is present.

The LED driver pins also provide manual configuration control during Hardware Control operation. Refer to the discussion of "Hardware Control Interface" on page 22 for details.

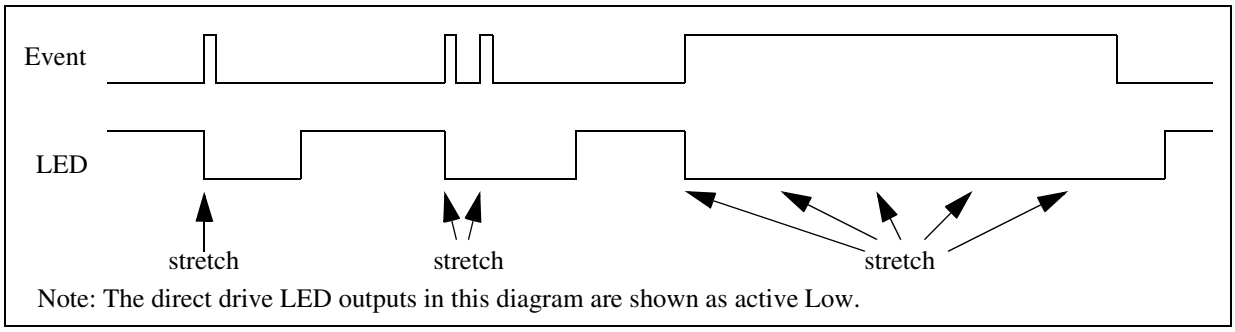
2.9.2.1 LED Pulse Stretching

The LED Configuration Register also provides optional LED pulse stretching to 30, 60, or 100 ms. If during this pulse stretch period, the event occurs again, the pulse stretch time will be further extended.

When an event such as receiving a packet occurs it will be edge detected and it will start the stretch timer. The LED driver will remain asserted until the stretch timer expires. If another event occurs before the stretch timer expires then the stretch timer will be reset and the stretch time will be extended.

When a long event (such as duplex status) occurs it will be edge detected and it will start the stretch timer. When the stretch timer expires the edge detector will be reset so that a long event will cause another pulse to be generated from the edge detector which will reset the stretch timer and cause the LED driver to remain asserted. Figure 21 shows how the stretch operation functions.

Figure 21. LED Pulse Stretching



Note: The direct drive LED outputs in this diagram are shown as active Low.

2.9.3 Monitoring Auto-Negotiation

Auto-negotiation can be monitored as follows:

- Bit 17.7 is set to 1 once the auto-negotiation process is completed.
- Bits 1.2 and 17.10 are set to 1 once the link is established.
- Additional bits in Register 1 (refer to Table 39 on page 66) and Register 17 (refer to Table 48 on page 72) can be used to determine the link operating conditions and status.

2.9.3.1 Monitoring Next Page Exchange

The LXT97x2 offers an Alternate Next Page mode to simplify the next page exchange process. Normally, bit 6.1 (Page Received) remains set until read. When Alternate Next Page mode is enabled (16.1 = 1), bit 6.1 is automatically cleared whenever a new negotiation process takes place. This prevents the user from reading an old value in 6.1 and assuming that Registers 5 and 8 (Partner Ability) contain valid information. Additionally, the LXT97x2 uses bit 6.5 to indicate

when the current received page is the base page. This information is useful for recognizing when next pages must be resent due to a new negotiation process starting. Bits 6.1 and 6.5 are cleared when read.

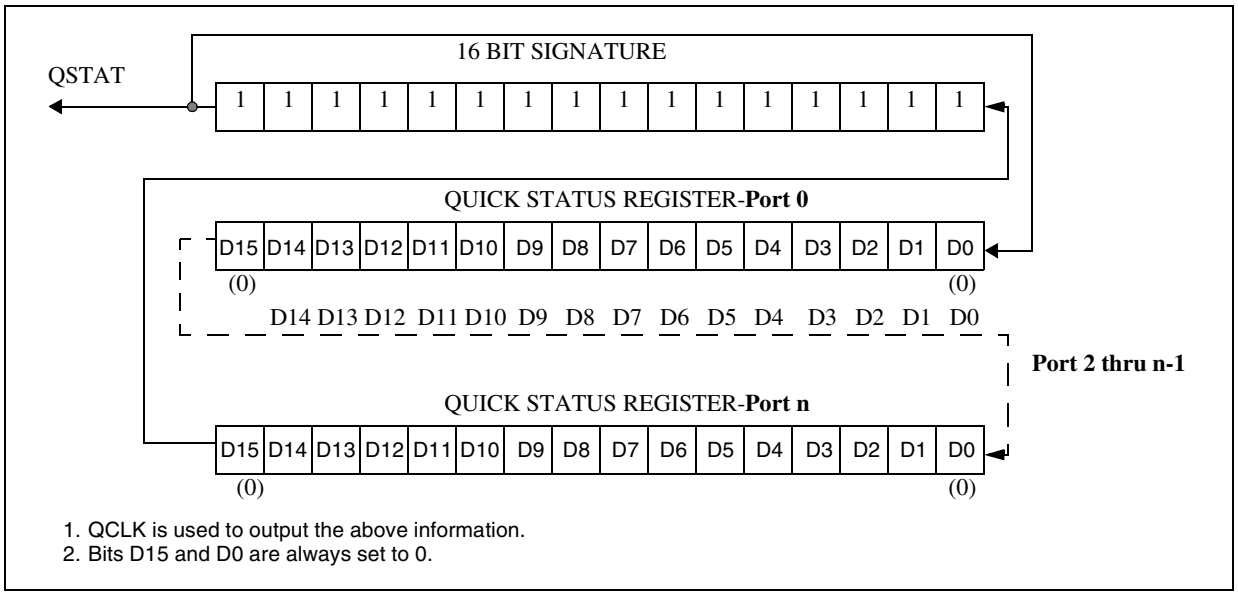
2.9.4 Using the Quick Status Register

The LXT97x2 continuously sends out the Quick Status Register contents on the QSTAT pin. This output provides a continuous, real-time status update of several different LXT97x2 attributes and modes including RX, TX, COL and the auto-negotiation process.

The 16 bits of the Quick Status Register are separated by a 16-bit signature frame (1111111111111111) to simplify interface designs.

The LXT97x2 sources this status information separated by the signature with respect to the falling edge of the QCLK input. An ASIC need supply only 1 clock output (up to 25 MHz) for multiple PHY devices. Refer to Table 48 on page 72 for Quick Status bits descriptions.

Figure 22. Quick Status Register



1. QCLK is used to output the above information.
2. Bits D15 and D0 are always set to 0.

2.10 Boundary Scan (JTAG1149.1) Functions

LXT97x2 includes a IEEE 1149.1 boundary scan test port for board level testing. All digital input, output, and input/output pins are accessible via boundary scan.

2.10.1 Boundary Scan Interface

This interface consists of five pins (TMS,TDI,TDO, TCK and TRST). It includes a state machine, data register array, and instruction register. The TMS and TDI pins are internally pulled up. TCK is internally pulled down. TDO does not have an internal pull-up or pull-down.

2.10.2 State Machine

The TAP controller is a 16 state machine driven by the TCK and TMS pins. Upon reset, the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS is High for five TCK periods.

2.10.3 Instruction Register

The IDCODE instruction is always invoked after the state machine resets. The decode logic ensures the correct data flow to the data registers according to the current instruction. Valid instructions are listed in Table 14.

2.10.4 Boundary Scan Register

Each BSR cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. There are four modes of operation as listed in Table 13.

Table 13. BSR Mode of Operation

Mode	Description
1	Capture
2	Shift
3	Update
4	System Function

Table 14. Supported JTAG Instructions

Name	Code	Description	Data Register
EXTEST	0000000000000000	External Test	BSR
IDCODE	1111111111111110	ID Code Inspection	ID REG
SAMPLE	1111111111111110	Sample Boundary	BSR
High Z	1111111111001111	Force Float	Bypass
Clamp	1111111111101111	Clamp	BSR
BYPASS	1111111111111111	Bypass Scan	Bypass

Table 15. Device ID Register

31:28	27:12	11:8	7:1	0
Version	Part ID (hex)	Jedec Continuation Characters	JEDEC ID[1]	Reserved
0000	2622 (LXT9762) 2636 (LXT9782)	0000	111 1110	1

1. The JEDEC ID is an 8-bit identifier. The MSB is for parity and is ignored. Intel's JEDEC ID is FE (1111 1110) which becomes 111 1110.

3.0 Application Information

3.1 Design Recommendations

The LXT97x2 complies with IEEE requirements and provides outstanding receive Bit Error Rate (BER) and long-line-length performance. Obtaining maximum performance from the LXT97x2 requires attention to detail and good design practices. Refer to the LXT97x2 Design and Layout Guide for detailed design and layout information.

3.1.1 General Design Guidelines

Adhering to generally accepted design practices minimizes noise levels on power and ground planes. Up to 50 mV of noise is considered acceptable. 50 to 80 mV of noise is considered marginal. High-frequency switching noise can be reduced, and its effects can be eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of .01 µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT97x2 and the RJ-45 connectors at the edge of the board.
- Do not extend any circuit power and ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

3.1.2 Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane can cause EMI problems and degrade line performance. Minimize ground noise as much as possible using good general techniques and by filtering the VCC plane. Predicting the noise performance of any design is difficult, although certain factors greatly increase the risk of noise problems:

- Poorly-regulated or over-burdened power supplies
- Wide data busses (32-bits+) running at a high clock rate
- DC-to-DC converters

Intel recommends filtering the power supply to the analog VCC pins of the LXT97x2. This has two benefits. First, prevents digital switching noise from affecting the analog circuitry inside the LXT97x2, which helps line performance. Second, if the VCC planes are laid out correctly, it keeps digital switching noise away from external connectors, reducing EMI problems.

Intel recommends dividing the VCC plane into two sections. The digital section supplies power to the VCCD and VCCIO pins of the LXT97x2. The analog section supplies power to the VCCA pins. The break between the two planes should run underneath the device. In designs with more than one LXT97x2, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. Beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. A bulk cap (2.2 -10 µF) should be place on each side of each bead.

In addition, a high-frequency bypass cap (.01µF) should be placed near each analog VCC pin.

3.1.3 Power and Ground Plane Layout Considerations

Take great care when laying out the power and ground planes. The following guidelines are recommended:

- Follow the guidelines in the *LXT97x2 Design & Layout Guide* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPFOP/N and TPFIP/N signals, away from the magnetics, and away from the RJ-45 connectors.
- Place the layers so that the TPFOP/N and TPFIP/N signals can be routed near or next to the ground plane. For EMI reasons, it is more important to shield TPFOP/N than TPFIP/N.

3.1.3.1 Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ45 connectors to the magnetics, and can be used to terminate unused signal pairs (‘Bob Smith’ termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2 kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2 kV isolation to the Bob Smith termination.

3.1.4 MII Terminations

Series termination resistors are not required on the SMII signals driven by the LXT97x2.

3.1.5 The RBIAS Pin

The LXT97x2 requires a 22.1 kΩ, 1% resistor directly connected between the RBIAS pin and ground. Place the RBIAS resistor as close to the RBIAS pin as possible. Run an etch directly from the pin to the resistor, and sink the other side of the resistor to a filtered ground. Surround the RBIAS trace with a filtered ground; do not run high-speed signals next to RBIAS.

3.1.6 The Twisted-Pair Interface

Follow standard guidelines for a twisted-pair interface:

- Keep transmit pair traces as short as possible; both traces should have the same length.

- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- Route the transmit pair adjacent to a ground plane. The optimum arrangement is to place the transmit traces two to three layers from the ground plane, with no intervening signals.
- The output stage of the transmitter shown in Figure 24 on page 50 is designed to match the 100Ω characteristic impedance of an unshielded CAT5 twisted-pair wire. The external resistor that is typically required for impedance matching is integrated in the transmitter of the LXT97xx. The internal termination provides a constant current reference in both 10BASE-T and 100BASE-TX applications and meets all IEEE transmitter requirements such as return loss, while reducing external component requirements. It has no impact in fibre designs.
- Some magnetic vendors are producing magnetics with improved return loss performance. Use of these improved magnetics increases the return loss budget available to the system designer.
- Improve EMI performance by filtering the TPO center tap. A single ferrite bead may be used to supply center tap current to all ports. All ports draw a combined total of 520 mA so the bead should be rated at 780 mA.

3.1.6.1 Magnetics Information

The LXT97x2 requires a 1:1 ratio for the receive transformers and a 1:1 ratio for the transmit transformers. The transformer isolation voltage should be rated at 1.5 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 16 for transformer requirements. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and validate the magnetics for the specific application.

3.1.7 The Fiber Interface

The fiber interface consists of a PECL transmit and receive pair to an external fiber-optic transceiver. The transmit and receive pair should be DC-coupled to the transceiver, and biased appropriately. Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 25 on page 51 shows a typical example.

Table 16. Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	
Tx turns ratio	–	1 : 1	–	–	
Insertion loss	0.0	0.6	1.1	dB	
Primary inductance	350	–	–	µH	
Transformer isolation	–	1.5	–	kV	
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz

3.2 Typical Application Circuits

Figure 24 shows a typical layout of the LXT97x2 twisted-pair interface in a dual-high (stacked) RJ45 application.

Figure 23. Power and Ground Supply Connections

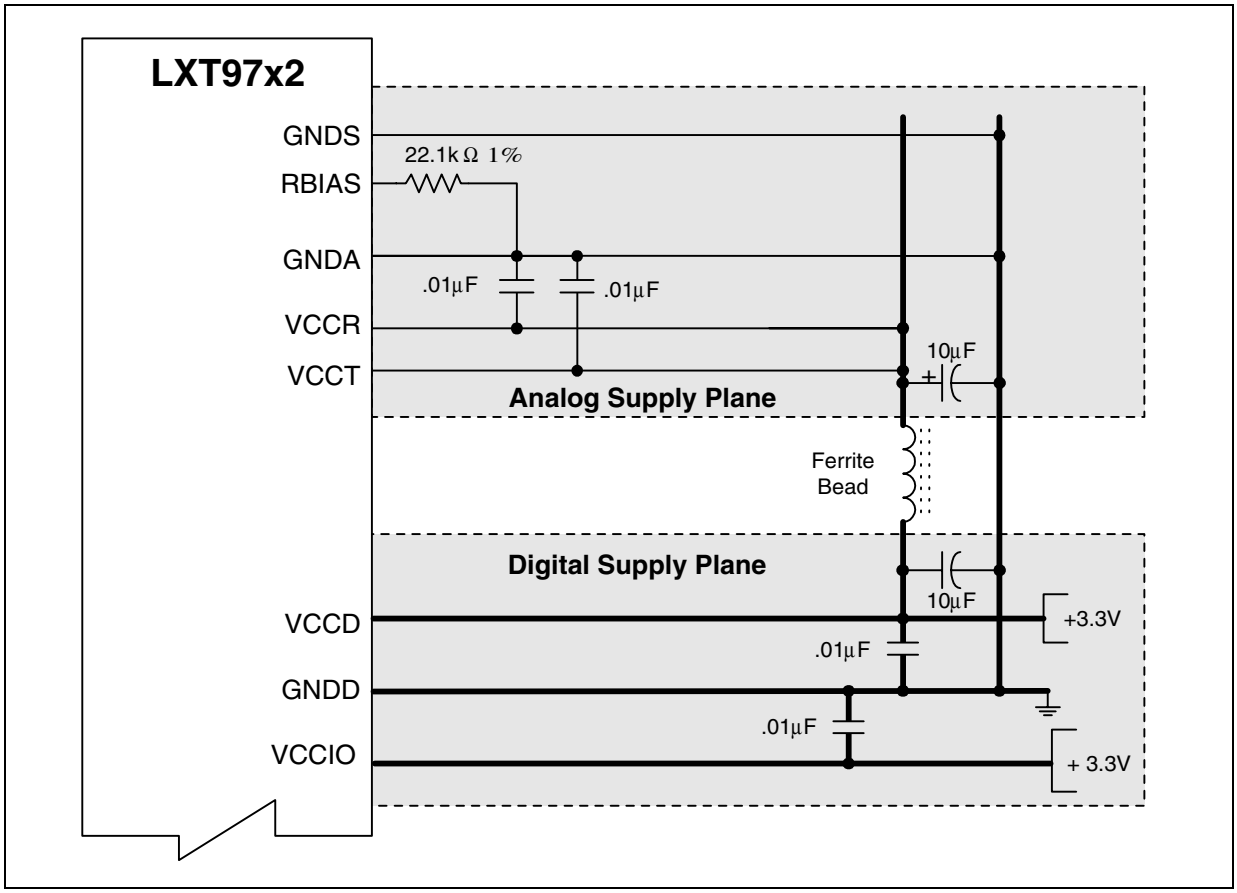
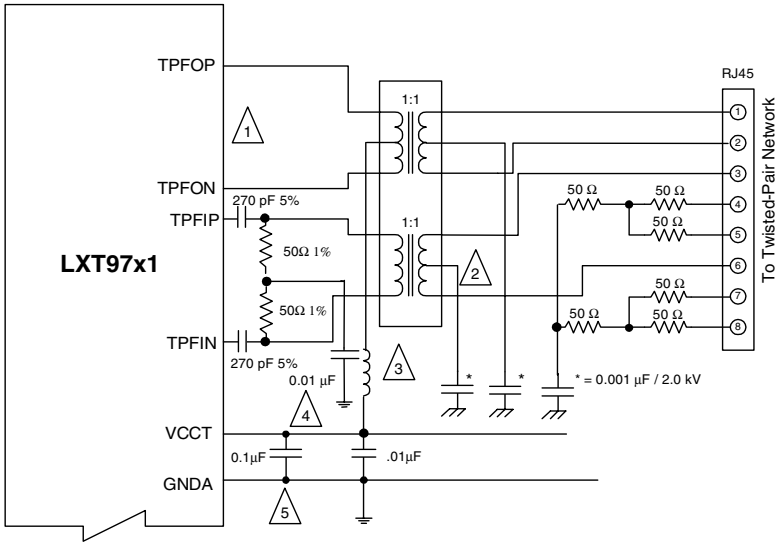
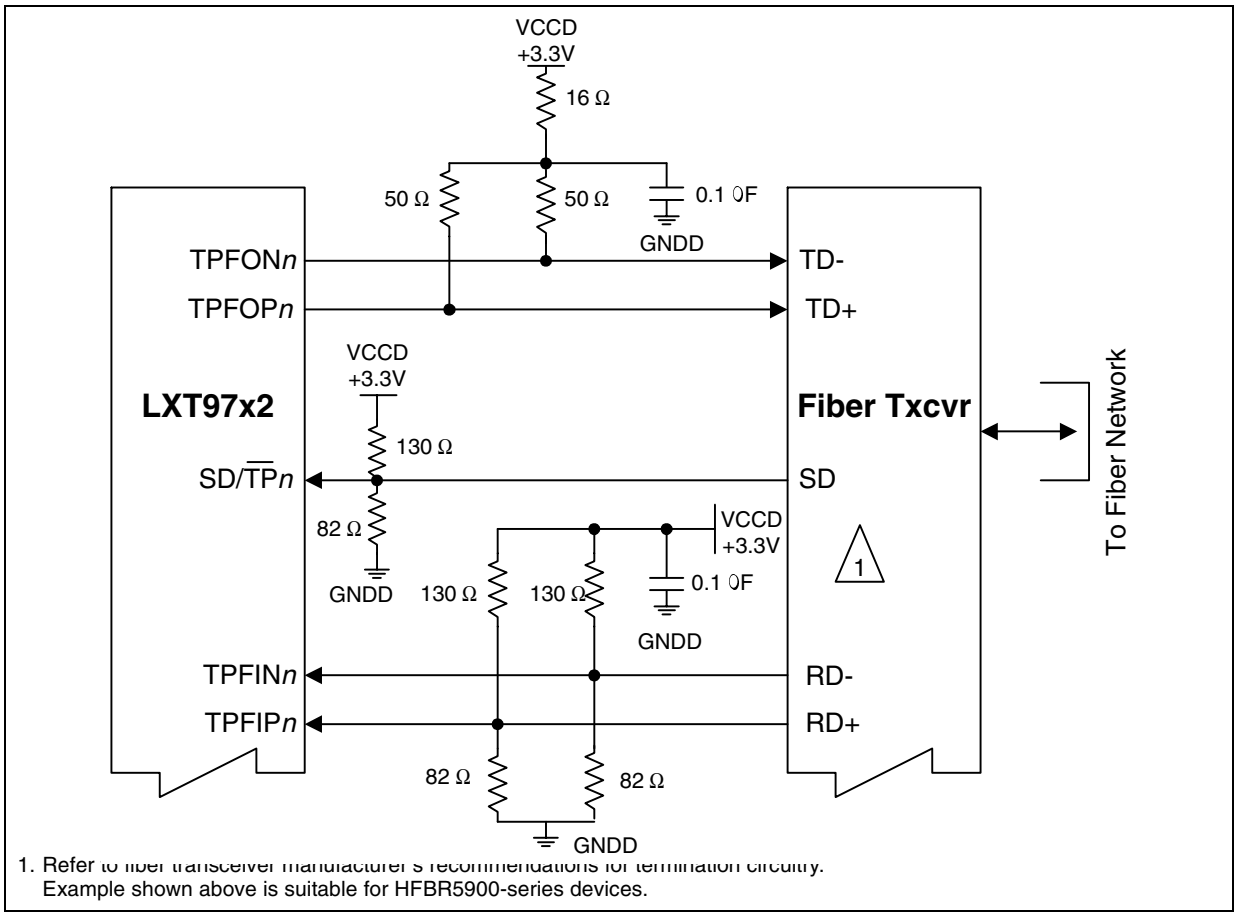


Figure 24. Typical Twisted-Pair Interface



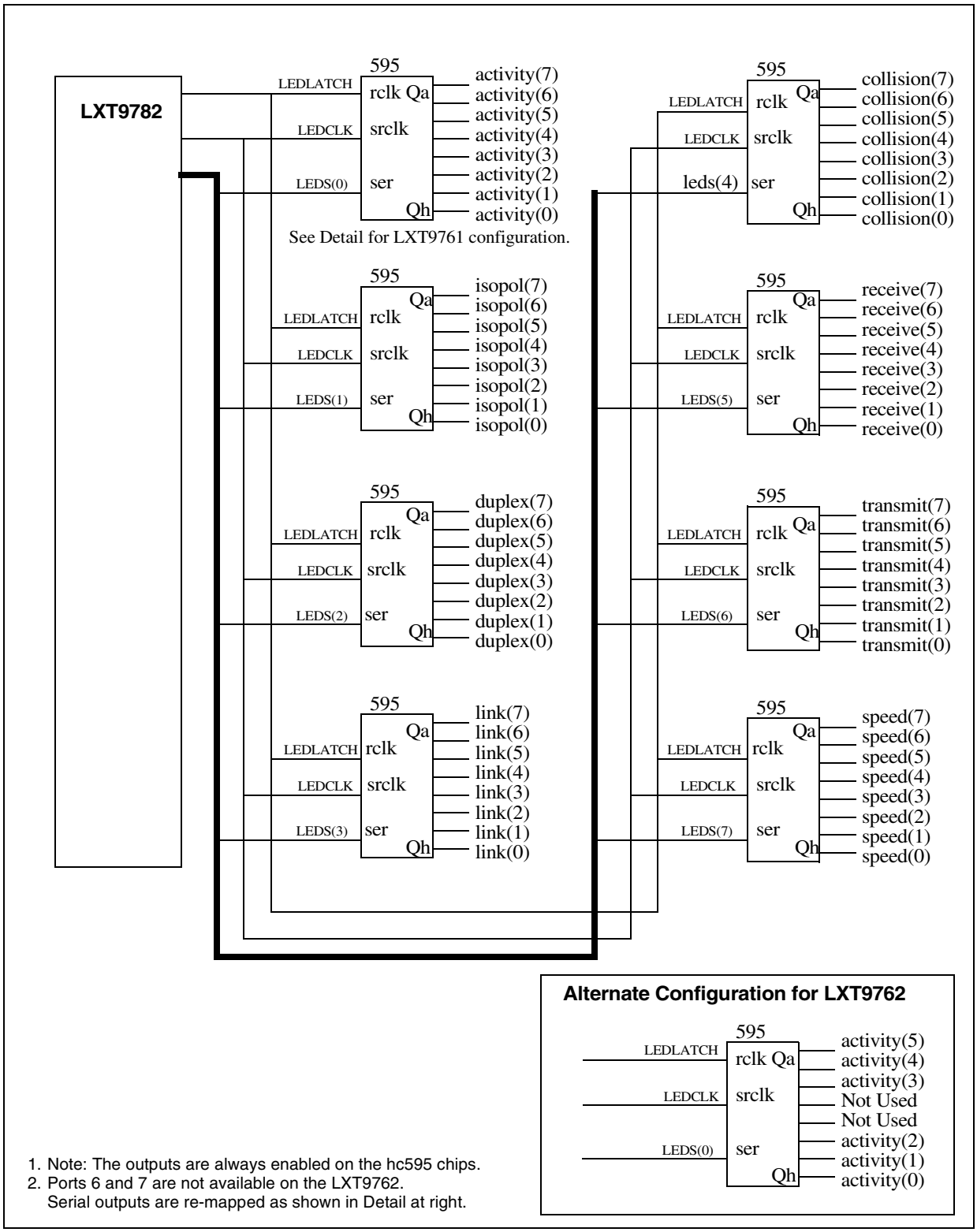
1. The 100Ω transmit load termination resistor typically required is integrated in the LXT97xx.
2. Magnetics without a receive pair center-tap do not require a 2 kV termination.
3. Center tap current may be supplied from 3.3V VCCA as shown. However, additional power savings may be realized by supplying the center-tap from from a 2.5V current source. In either case a single ferrite bead (rated at 800 mA) may be used to supply center tap current to all ports.
4. Receive common mode bypass cap may improve BER performance in systems with noisy power supplies.
5. Recommended 0.1µF capacitor to improve the EMI performance.

Figure 25. Typical Fiber Interface



1. Refer to fiber transceiver manufacturer's recommendations for termination circuitry. Example shown above is suitable for HFBR5900-series devices.

Figure 26. Typical Serial LED Interface



1. Note: The outputs are always enabled on the hc595 chips.
2. Ports 6 and 7 are not available on the LXT9762.
   Serial outputs are re-mapped as shown in Detail at right.

4.0 Test Specifications

Table 17 through Table 34 and Figure 28 through Figure 39 represent the target specifications of the LXT97x2. These specifications are guaranteed by test, except where noted "by design." Minimum and maximum values listed in Table 19 through Table 34 apply over the recommended operating conditions specified in Table 18.

Table 17. Absolute Maximum Ratings

Parameter		Sym	Min	Max	Units
Supply voltage		VCC	-0.3	4.0	V
Operating temperature	Ambient	TOPA	-15	+85	ºC
	Case	TOPC	–	+120	ºC
Storage temperature		TST	-65	+150	ºC

Caution: Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units
Recommended operating temperature	Ambient	TOPA	0	–	70	ºC
	Case[4]	TOPC	0	–	122	ºC
Recommended supply voltage[2]	Analog & Digital	Vcca, Vccd	3.15	3.3	3.45	V
	I/O	Vccio	3.15	–	3.45	V
VCC current	100BASE-TX	ICC	–	121	140	mA
	100BASE-FX	ICC	–	–	140	mA
	10BASE-T	ICC	–	–	–	mA
	Power Down Mode	ICC	–	–	–	mA
	Auto-Negotiation	ICC	–	114.5[3]	–	mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.
3. Per port @ 3.3V.
4. Environmental Condition - Natural convection (still air). Topc should be measured in the worst case thermal condition (chassis, application, environment). If the Topc is greater than 122C, Air Flow ('100 LFM) or heat sink (Attach: Thermoset WP100 tape, 1"x1" square with a 0.75" diameter phase-change dot. Heat Sink: Thermally 31x31 mm-sq low profile, P/N 22370B must be added. Alternate thermal solutions may be used and/or required depending on specific system conditions.

Table 19. Digital I/O Characteristics [1]

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage[3]	V_{IL}	–	–	0.8	V	–
Input High voltage[3]	V_{IH}	2.0	–	–	V	–
Input current	I_I	-100	–	100	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

1. Applies to all pins except SMII pins. Refer to Table 20 for SMII I/O Characteristics.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. Does not apply to REFCLK, QCLK or TCK. Refer to Table 21 for clock input levels.

Table 20. Digital I/O Characteristics - SMII Pins

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-100	–	100	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.2	–	–	V	I_{OH} = -4 mA, V_{CC} = 3.3V
	V_{OH}	2.0	–	–	V	I_{OH} = -4 mA, V_{CC} = 2.5V
Driver output resistance (Line driver output enabled)	R_O[2]	–	100	–	Ω	V_{CC} = 2.5V
	R_O[2]	–	100	–	Ω	V_{CC} = 3.3V

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 21. Required REFCLK and SYNC Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input rise/fall time	Trf	–	1	–	ns	–
REFCLK frequency	*F*	–	125	–	MHz	–
REFCLK clock frequency tolerance[2]	Δf	–	–	± 100	ppm	–
REFCLK clock duty cycle[2]	Tdc	40	–	60	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 22. 100BASE-TX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	VP	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	–	102	%	Note 2
Signal rise/fall time	TRF	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	TRFS	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	+/- 0.5	ns	Offset from 16ns pulse width at 50% of pulse peak
Overshoot	VO	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω(+/-1%) resistor.

Table 23. 100BASE-FX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Note: Peak differential output voltage (single ended)	VOP	0.6	–	1.5	V	–
Note: Signal rise/fall time	TRF	–	–	1.9	ns	10 <–> 90% 2.0 pF load
Note: Jitter (measured differentially)	–	–	–	1.4	ns	–
Note: Peak differential input voltage	VIP	0.55	–	1.5	V	–
Note: Common mode input range	VCMIR	–	–	VCC - 0.7	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 24. 10BASE-T Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	VOP	2.2	2.5	2.8	V	Note 2
Link transmit period	–	8	–	24	ms	–
Transmit timing jitter added by the MAU and PLS sections [3, 4]	–	0	2	11	ns	Note 5
Link min receive timer	TLRmin	2	4	7	ms	–
Link max receive timer	TLRmax	50	64	150	ms	–
Time link loss receive	TLL	50	64	150	ms	–
Differential squelch threshold	VDS	–	390	–	mV Peak	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω(+/-1%) resistor.
3. Parameter is guaranteed by design; not subject to production testing.
4. IEEE 802.3 specifies maximum jitter addition at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.
5. After line model specified by IEEE 802.3 for 10BASE-T MAU

Figure 27. MII Sync Timing

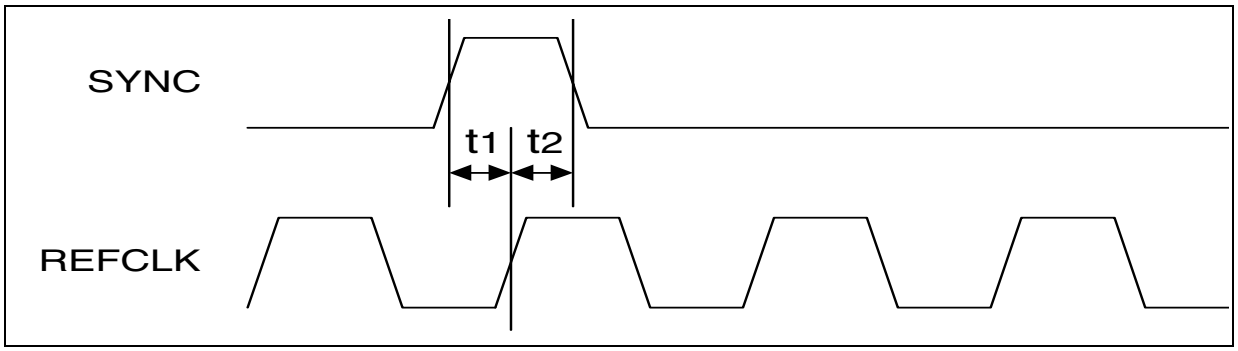


Table 25. MII Sync Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
SYNC setup to REFCLK rising edge	t1	1.5	–	–	ns	–
SYNC delay from REFCLK rising edge	t2	1	–	–	ns	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 28. 100BASE-TX Receive Timing

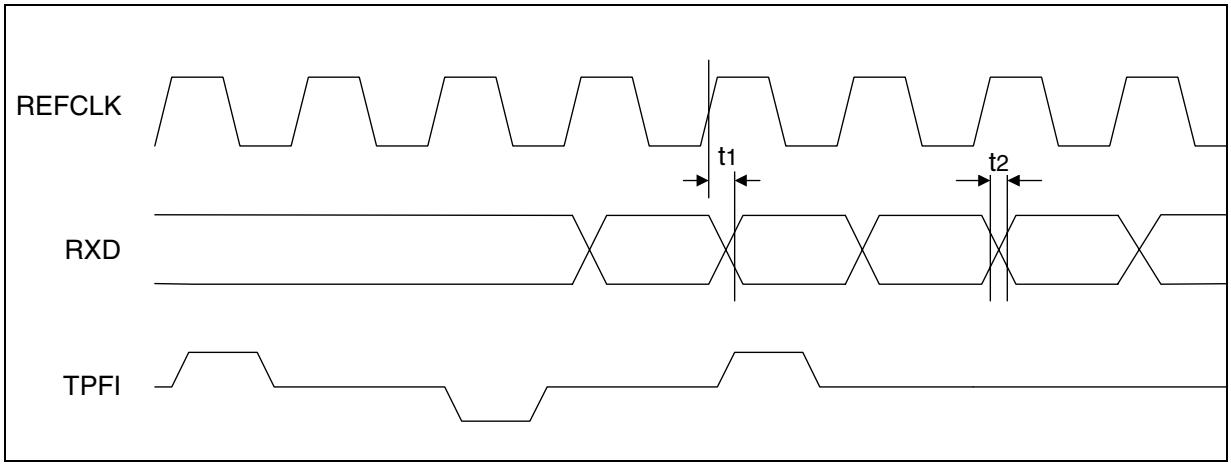


Table 26. 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD setup from REFCLK rising edge	t1	2	–	5	ns	See Figure 29
RXD Rise/Fall Time	t2	–	3	–	ns	–
Receive start of /J/ to CRS asserted	–	–	16	–	BT	Synchronous sampling of SMII
Receive start of /T/ to CRS de-asserted	–	–	20	–	BT	Synchronous sampling of SMII
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 29. SMII Output Delay Test Setup

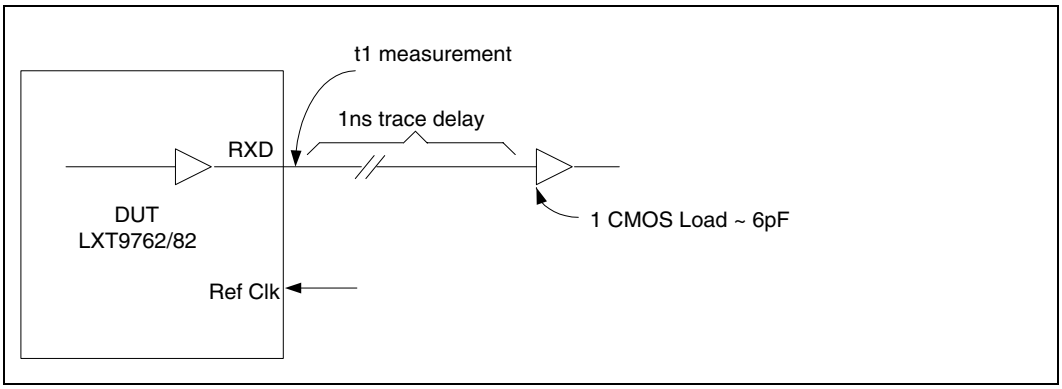


Figure 30. 100BASE-TX Transmit Timing

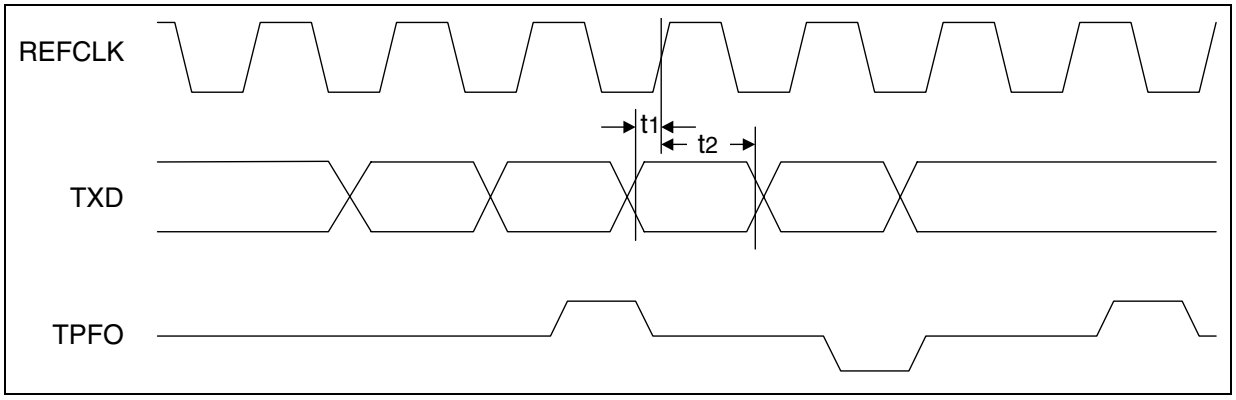


Table 27. 100BASE-TX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD setup to REFCLK rising edge	t1	1.5	–	–	ns	–
TXD hold from REFCLK rising edge	t2	1	–	–	ns	–
TXEN sampled to start of /J/	–	–	12	–	BT	Synchronous sampling of SMII
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 31. 100BASE-FX Receive Timing

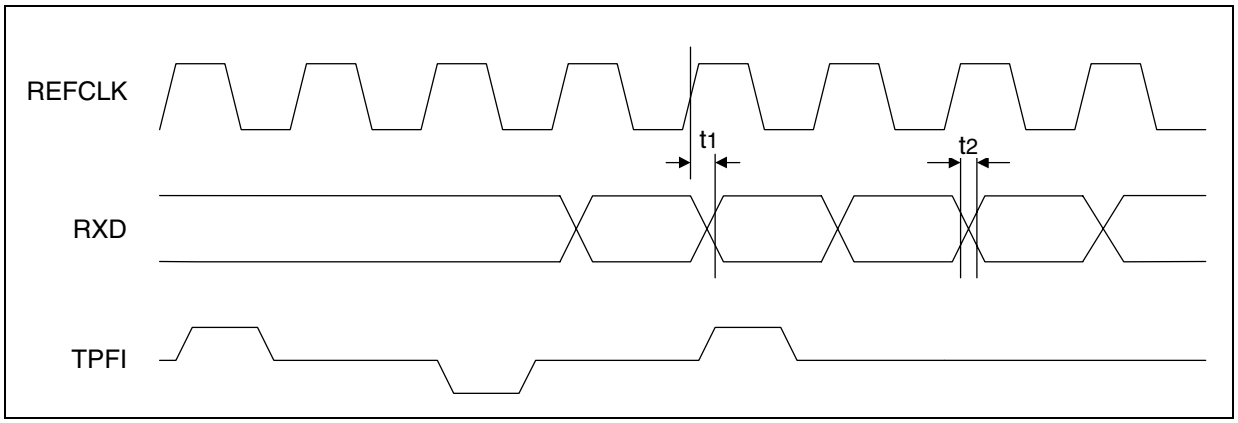


Table 28. 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD setup from REFCLK rising edge	t1	2	–	5	ns	See Figure 29
RXD Rise/Fall Time	t2	–	3	–	ns	–
Receive start of /J/ to CRS asserted	–	–	16	–	BT	Synchronous sampling of SMII
Receive start of /T/ to CRS de-asserted	–	–	20	–	BT	Synchronous sampling of SMII
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 32. 100BASE-FX Transmit Timing

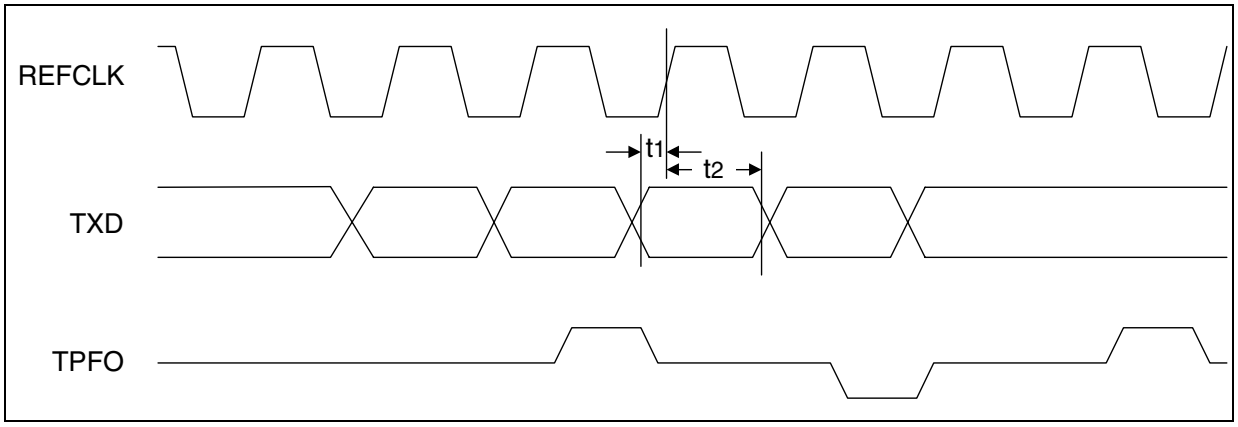


Table 29. 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD setup to REFCLK rising edge	t1	1.5	–	–	ns	–
TXD hold from REFCLK rising edge	t2	1	–	–	ns	–
TXEN sampled to start of /J/	–	–	12	–	BT	Synchronous sampling of SMII
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 33. 10BASE-T Receive Timing

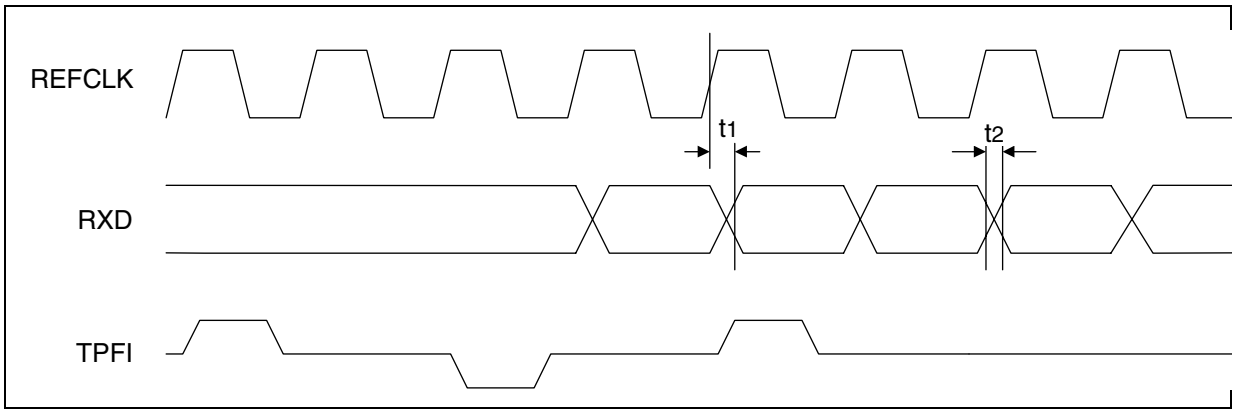


Table 30. 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD setup from REFCLK rising edge	t1	2	–	5	ns	See Figure 29
RXD Rise/Fall Time	t2	–	3	–	ns	–
Receive Start-of-Frame to CRS asserted	–	–	9	–	BT	Synchronous sampling of SMII[2]
Receive Start-of-Idle to CRS de-asserted	–	–	12	–	BT	Synchronous sampling of SMII[2]

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Assumes each SMII segment is sampled for CRS.

Figure 34. 10BASE-T Transmit Timing

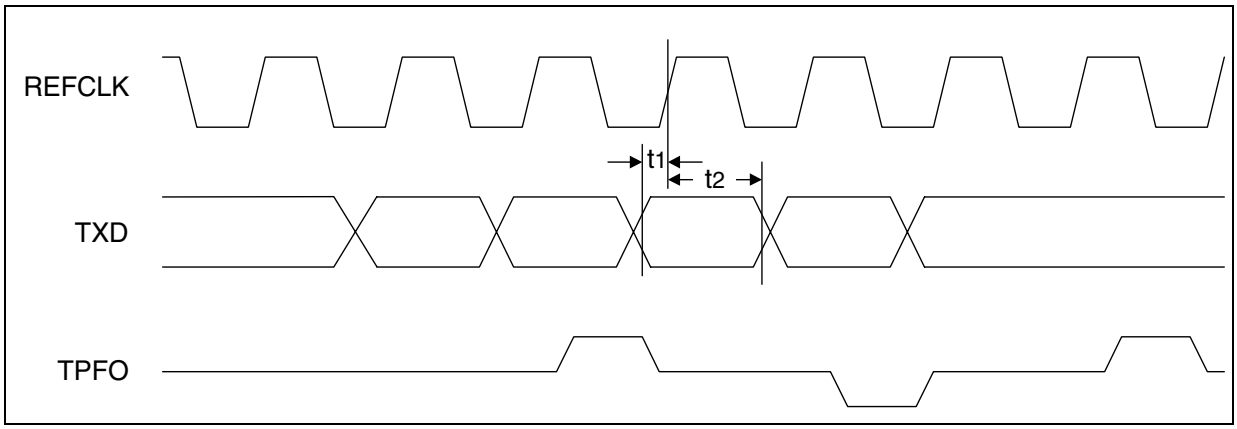


Table 31. 10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD setup to REFCLK rising edge	t1	1.5	–	–	ns	–
TXD hold from REFCLK rising edge	t2	1	–	–	ns	–
TXEN sampled to Start-of-Frame	–	–	8	–	BT	Synchronous sampling of SMII

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 35. Auto-Negotiation and Fast Link Pulse Timing

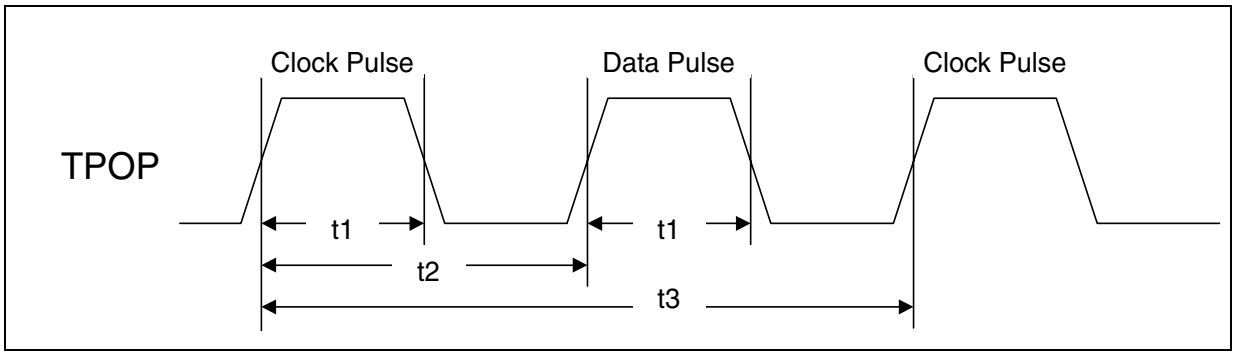


Figure 36. Fast Link Pulse Timing

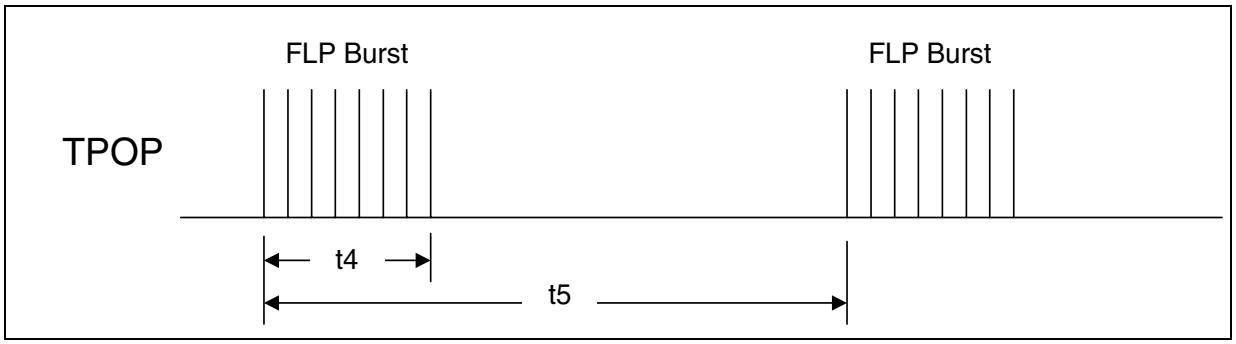


Table 32. Auto-Negotiation and Fast Link Pulse Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	–
Clock pulse to Data pulse	t2	55.5	–	69.5	µs	–
Clock pulse to Clock pulse	t3	111	–	139	µs	–
FLP burst width	t4	–	2	–	ms	–
FLP burst to FLP burst	t5	8	–	24	ms	–
Clock/Data pulses per burst	–	17	–	33	ea	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 37. MDIO Write Timing (MDIO Sourced by MAC)

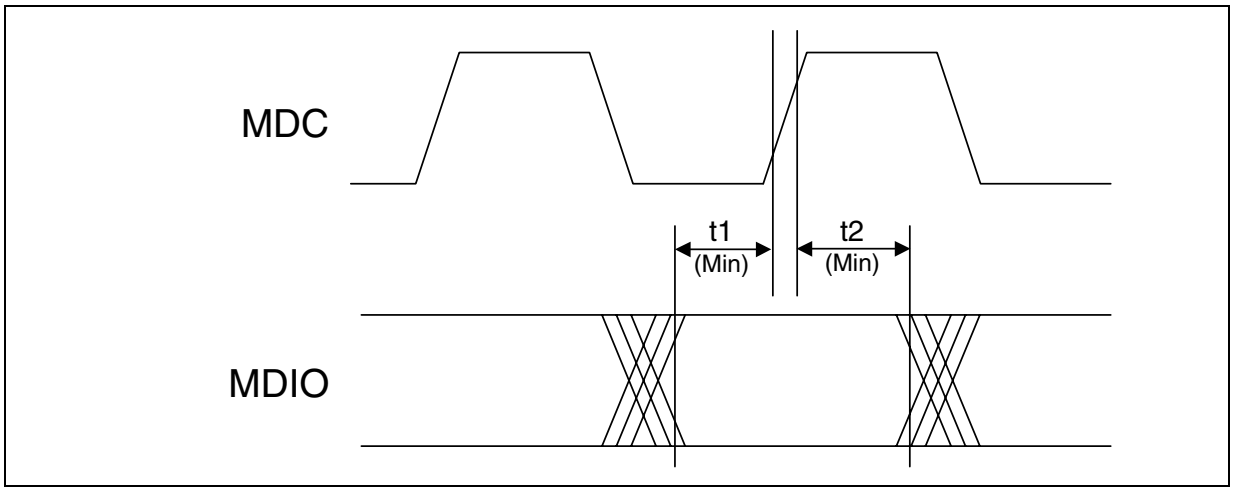


Figure 38. MDIO Read Timing (MDIO Sourced by PHY)

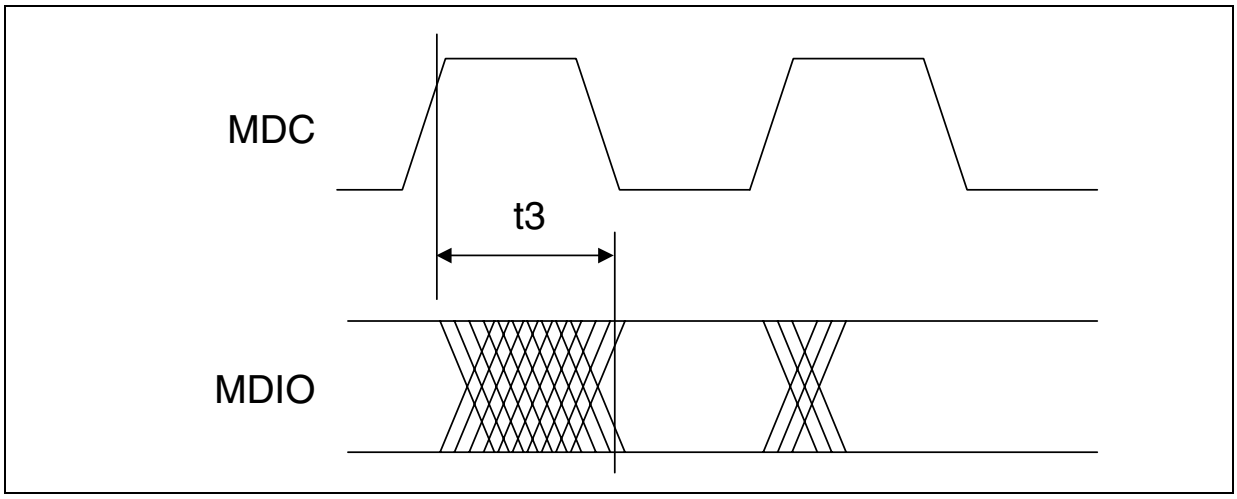


Table 33. MDIO Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
MDIO setup before MDC, sourced by STA	t1	10	–	–	ns	MDC = 2.5 MHz
		1	–	–	ns	MDC = 8 MHz
MDIO hold after MDC, sourced by STA	t2	10	–	–	ns	MDC = 2.5 MHz
		1	–	–	ns	MDC = 8 MHz
MDC to MDIO output delay, sourced by PHY	t3	10	–	300	ns	MDC = 2.5 MHz
		1	130	–	ns	MDC = 8 MHz

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 39. Power-Up Timing

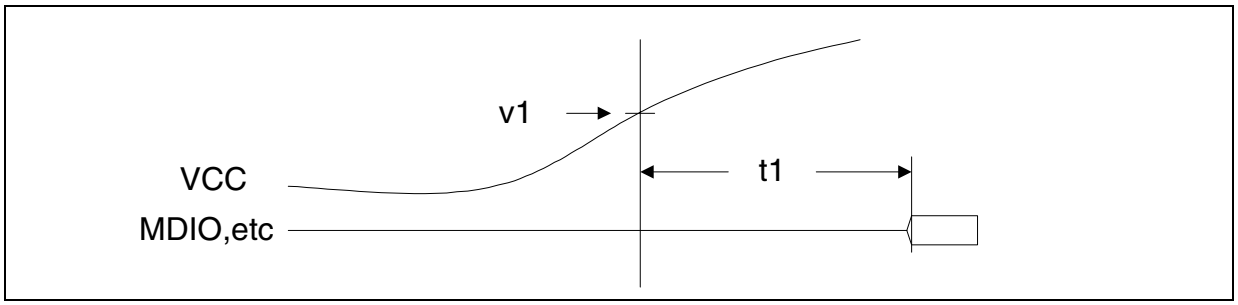


Table 34. Power-Up Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Voltage threshold	v1	–	2.9	–	V	–
Power Up delay	t1	–	–	500	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 40. $\overline{\text{Reset}}$ and Power-Down Recovery Timing

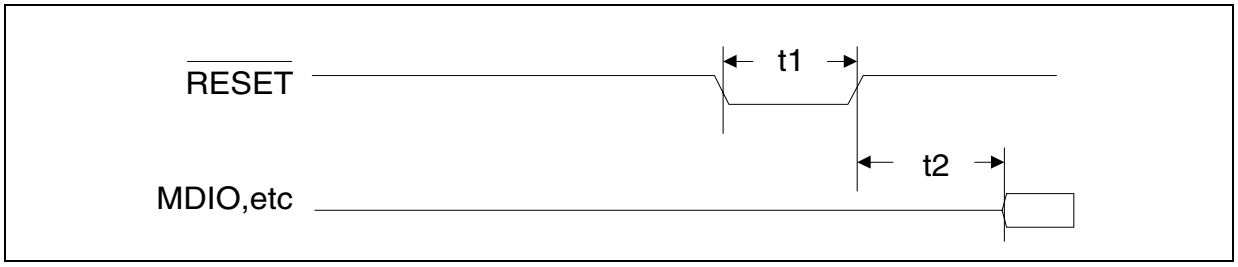


Table 35. $\overline{\text{Reset}}$ and Power-Down Recovery Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
$\overline{\text{RESET}}$ pulse width	t1	10	–	–	ns	
$\overline{\text{RESET}}$ recovery delay	t2	–	1	–	ms	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

5.0 Register Definitions

The LXT97x2 register set includes multiple 16-bit registers, 16 registers per port. Table 36 presents a complete register listing. Table 37 is a complete memory map of all registers and Table 38 through Table 53 provide individual register definitions.

- Base registers (0 through 8) are defined in accordance with the "Reconciliation Sublayer and Media Independent Interface" and "Physical Layer Link Signaling for 10/100 Mbps Auto-Negotiation" sections of the IEEE 802.3 specification.
- Additional registers (16 through 22) are defined in accordance with the IEEE 802.3 specification for adding unique chip functions.

Table 36. Register Set

Address	Register Name	Bit Assignments
0	Control Register	Refer to Table 38 on page 66
1	Status Register	Refer to Table 39 on page 66
2	PHY Identification Register 1	Refer to Table 40 on page 67
3	PHY Identification Register 2	Refer to Table 41 on page 68
4	Auto-Negotiation Advertisement Register	Refer to Table 42 on page 68
5	Auto-Negotiation Link Partner Base Page Ability Register	Refer to Table 43 on page 69
6	Auto-Negotiation Expansion Register	Refer to Table 44 on page 70
7	Auto-Negotiation Next Page Transmit Register	Refer to Table 45 on page 71
8	Auto-Negotiation Link Partner Next Page Receive Register	Refer to Table 46 on page 71
9	1000BASE-T/100BASE-T2 Control Register	Not Implemented
10	1000BASE-T/100BASE-T2 Status Register	Not Implemented
15	Extended Status Register	Not Implemented
16	Port Configuration Register	Refer to Table 47 on page 72
17	Quick Status Register	Refer to Table 48 on page 72
18	Interrupt Enable Register	Refer to Table 49 on page 73
19	Interrupt Status Register	Refer to Table 50 on page 74
20	LED Configuration Register	Refer to Table 51 on page 75
21-27	Reserved	
28	Transmit Control Register #1	Refer to Table 52 on page 76
29	Reserved	
30	Transmit Control Register #2	Refer to Table 53 on page 76
31	Reserved	

Table 37. Register Bit Map

Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Control Register																	
Control	Reset	Loopback	Speed Select	A/N Enable	Power Down	Reserved	Re-start A/N	Duplex Mode	COL Test	Speed Select	Reserved						0
Status Register																	
Status	100Base-T4	100Base-X Full Duplex	100Base-X Half Duplex	10Mbps Full Duplex	10Mbps Half Duplex	100Base-T2 Full Duplex	100Base-T2 Half Duplex	Extended Status	Reserved	MF Preamble Suppress	A/N Complete	Remote Fault	A/N Ability	Link Status	Jabber Detect	Extended Capability	1
PHY ID Registers																	
PHY ID 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	2
PHY ID2	PHY ID No						MFR Model No						MFR Rev No				3
Auto-Negotiation Advertisement Register																	
A/N Advertise	Next Page	Reserved	Remote Fault	Reserved	Asymm Pause	Pause	100Base-T4	100Base-TX Full Duplex	100Base-TX	10Base-T Full Duplex	10Base-T	IEEE Selector Field					4
Auto-Negotiation Link Partner Base Page Ability Register																	
A/N Link Ability	Next Page	Ack	Remote Fault	Reserved	Asymm Pause	Pause	100Base-T4	100Base-TX Full Duplex	100Base-TX	10Base-T Full Duplex	10Base-T	IEEE Selector Field					5
Auto-Negotiation Expansion Register																	
A/N Expansion	Reserved										Base Page	Parallel Detect Fault	Link Partner Next Page Able	Next Page Able	Page Received	Link Partner A/N Able	6
Auto-Negotiation Next Page Transmit Register																	
A/N Next Page Txmit	Next Page	Reserved	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											7
Auto-Negotiation Link Partner Next Page Ability Register																	
A/N Link Next Page	Next Page	Reserved	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											8
Port Configuration Register																	

Table 37. Register Bit Map (Continued)

Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Port Config	Reserved	Link Disable	Txmit Disable	Bypass Scrambler (100TX)	Bypass 4B/5B (100TX)	Jabber (10T)	SQE (10T)	TP Loopback (10T)	Reserved	FIFO Size	PRE_EN	Reserved	Reserved	Remote Fault Enable	Alternate Next Page	Fiber Select	16
Quick Status Register																	
Quick Status	Reserved	10/100 Mode	Transmit Status	Receiver Status	Collision Status	Link	Duplex Mode	Auto-Neg	Auto-Neg Complete	Reserved	Polarity	Pause	Error	Reserved	Reserved	Reserved	17
Interrupt Enable Register																	
Interrupt Enable	Reserved							Reserved	Auto-Neg Mask	Speed Mask	Duplex Mask	Link Mask	Reserved	Reserved	Interrupt Enable	Test Interrupt	18
Interrupt Status Register																	
Interrupt Status	Reserved							Reserved	Auto-Neg Done	Speed Change	Duplex Change	Link Change	Reserved	MD Interrupt	Reserved	Reserved	19
LED Configuration Register																	
LED Config	LED1				LED2				LED3				LED Freq		Pulse Stretch	Reserved/ Invalid Polarity	20
Analog Test Register #1																	
Analog #1	Reserved			Reserved									Bandwidth Control		Slew Control		28
Analog Test Register #2																	
Analog #2	Reserved		Driver Amp	Reserved													30

Table 38. Control Register (Address 0)

Bit	Name	Description	Type [1]	Default
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC	0
0.14	Loopback [2]	1 = enable loopback mode 0 = disable loopback mode	R/W	0
0.13	Speed Selection	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mbps (not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	R/W	Note 3 00
0.12	Auto-Negotiation Enable [4]	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process	R/W	Note 3 0
0.11	Power Down	1 = power down 0 = normal operation	R/W	0
0.10	Reserved	Write as zero. Ignore on read.	R/W	0
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = normal operation	R/W SC	
0.8	Duplex Mode	1 = Full Duplex 0 = Half Duplex	R/W	Note 3 0
0.7	Collision Test	This bit is ignored by the LXT97x2. 1 = Enable COL signal test 0 = Disable COL signal test	R/W	0
0.6	Speed Selection 1000 Mb/s	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mbps (not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	**R/W**	**00**
0.5:0	Reserved	Write as 0, ignore on Read	**R/W**	**00000**

1. R/W = Read/Write
   RO = Read Only
   SC = Self Clearing
2. Internal Fiber Loopback Function is activated when the external SD/TP# pin for the port is pulled High.
3. Default value of bits 0.12, 0.13 and 0.8 are determined by hardware pins at Reset. Refer to Reset discussion on page 27.
4. Do not enable Auto-Negotiation if Fiber Mode is selected.

Table 39. Status Register (Address 1)

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO	0
1.14	100BASE-X Full Duplex	1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X	RO	1
1.13	100BASE-X Half Duplex	1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X	RO	1

1. RO = Read Only
   LL = Latching Low
   LH = Latching High
2. Bit 1.4 is not valid if Auto-Negotiation is selected while operating in Fiber mode.

Table 39. Status Register (Address 1) (Continued)

Bit	Name	Description	Type [1]	Default
1.12	10 Mbps Full Duplex	1 = PHY able to operate at 10 Mbps in full-duplex mode 0 = PHY not able to operate at 10 Mbps full-duplex mode	RO	1
1.11	10 Mbps Half Duplex	1 = PHY able to operate at 10 Mbps in half-duplex mode 0 = PHY not able to operate at 10 Mbps in half-duplex	RO	1
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full-duplex 100BASE-T2 0 = PHY not able to perform full-duplex 100BASE-T2	RO	0
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half-duplex 100BASE-T2	RO	0
1.8	Extended Status	1 = Extended status information in register 15 0 = No extended status information in register 15	RO	0
1.7	Reserved	1 = ignore when read	RO	0
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO	0
1.5	Auto-Negotiation complete	1 = Auto-negotiation complete 0 = Auto-negotiation not complete	RO	0
1.4	Remote Fault[2]	1 = Remote fault condition detected 0 = No remote fault condition detected	RO/LH	0
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber condition detected 0 = Jabber condition not detected	RO/LH	0
1.0	Extended Capability	1 = Extended register capabilities 0 = Extended register capabilities	RO	0

1. RO = Read Only
   LL = Latching Low
   LH = Latching High
2. Bit 1.4 is not valid if Auto-Negotiation is selected while operating in Fiber mode.

Table 40. PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI.	RO	0013 hex

1. RO = Read Only

Table 41. PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID number	The PHY identifier composed of bits 19 through 24 of the OUI.	RO	011110
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number.	RO	001000 (LXT9762) 001011 (LXT9782)
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number.	RO	XXXX

1. RO = Read Only

Figure 41. PHY Identifier Bit Mapping

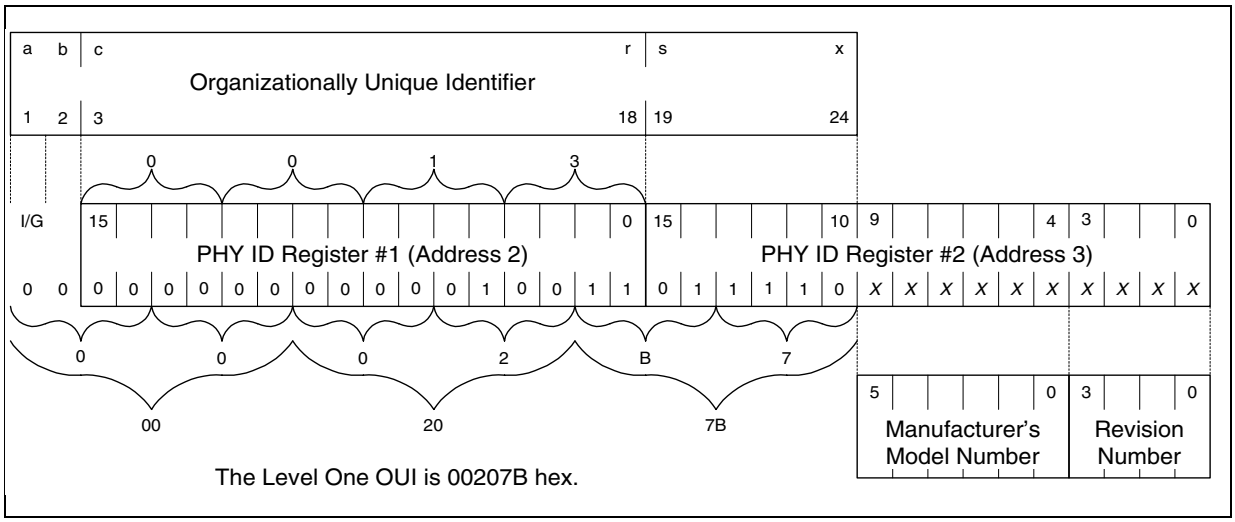


Table 42. Auto-Negotiation Advertisement Register (Address 4)

Bit	Name	Description	Type [1]	Default
4.15	Next Page	1 = Port has ability to send multiple pages. 0 = Port has no ability to send multiple pages.	R/W	1
4.14	Reserved	Ignore.	RO	0
4.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R/W	0
4.12	Reserved	Ignore.	R/W	0
4.11	Asymmetric Pause	Pause operation defined in Clause 40 and 27.	R/W	0
4.10	Pause	1 = Pause operation enabled for full-duplex links. 0 = Pause operation disabled.	R/W	Note 2

1. R/W = Read/Write
   RO = Read Only
   LHR = Latches High on Reset
2. The default setting of bit 4.10 (PAUSE) is determined by pin 79.
3. Default value of bits 4.8:5 are determined by hardware pins at Reset. Refer to Reset discussion on page 27.

Table 42. Auto-Negotiation Advertisement Register (Address 4) (Continued)

Bit	Name	Description	Type [1]	Default
4.9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. (The LXT97x2 does not support 100BASE-T4 but allows this bit to be set to advertise in the Auto-Negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W	0
4.8	100BASE-TX full-duplex	1 = Port is 100BASE-TX full duplex capable. 0 = Port is not 100BASE-TX full duplex capable.	R/W	Note 3
4.7	100BASE-TX	1 = Port is 100BASE-TX capable. 0 = Port is not 100BASE-TX capable.	R/W	Note 3
4.6	10BASE-T full-duplex	1 = Port is 10BASE-T full duplex capable. 0 = Port is not 10BASE-T full duplex capable.	R/W	Note 3
4.5	10BASE-T	1 = Port is 10BASE-T capable. 0 = Port is not 10BASE-T capable.	R/W	Note 3
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future Auto-Negotiation development. <11111> = Reserved for future Auto-Negotiation development. Unspecified or reserved combinations should not be transmitted.	R/W	00001

1. R/W = Read/Write
   RO = Read Only
   LHR = Latches High on Reset
2. The default setting of bit 4.10 (PAUSE) is determined by pin 79.
3. Default value of bits 4.8:5 are determined by hardware pins at Reset. Refer to Reset discussion on page 27.

Table 43. Auto-Negotiation Link Partner Base Page Ability Register (Address 5)

Bit	Name	Description	Type [1]	Default
5.15	Next Page	1 = Link Partner has ability to send multiple pages. 0 = Link Partner has no ability to send multiple pages.	RO	0
5.14	Acknowledge	1 = Link Partner has received Link Code Word from LXT97x2. 0 = Link Partner has not received Link Code Word from the LXT97x2.	RO	0
5.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	RO	0
5.12	Reserved	Ignore.	RO	0
5.11	Asymmetric Pause	Pause Operation defined in Clauses 40 and 27 1 = Link Partner is Asymmetric Pause capable. 0 = Link Partner is not Asymmetric Pause capable.	RO	0
5.10	Pause	1 = Link Partner is Pause capable. 0 = Link Partner is not Pause capable.	RO	0

1. RO = Read Only

Table 43. Auto-Negotiation Link Partner Base Page Ability Register (Address 5) (Continued)

Bit	Name	Description	Type [1]	Default
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	RO	0
5.8	100BASE-TX full duplex	1 = Link Partner is 100BASE-TX full duplex capable. 0 = Link Partner is not 100BASE-TX full duplex capable.	RO	0
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	RO	0
5.6	10BASE-T full duplex	1 = Link Partner is 10BASE-T full duplex capable. 0 = Link Partner is not 10BASE-T full duplex capable.	RO	0
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	RO	0
5.4:0	Selector Field S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future Auto-Negotiation development. <11111> = Reserved for future Auto-Negotiation development. Unspecified or reserved combinations shall not be transmitted.	RO	00000

1. RO = Read Only

Table 44. Auto-Negotiation Expansion (Address 6)

Bit	Name	Description	Type [1]	Default
6.15:6	Reserved	Ignore on read.	RO	0
6.5	Base Page	This bit indicates the status of the auto-negotiation variable, base page. It flags synchronization with the auto-negotiation state diagram allowing detection of interrupted links. This bit is only used if bit 16.1 (Alternate Next Page feature) is set. 1 = base_page = true 0 = base_page = false	RO	0
6.4	Parallel Detection Fault	1 = Parallel detection fault has occurred. 0 = Parallel detection fault has not occurred.	RO LH	0
6.3	Link Partner Next Page Able	1 = Link partner is next page able. 0 = Link partner is not next page able.	RO	0
6.2	Next Page Able	1 = Local device is next page able. 0 = Local device is not next page able.	RO	1
6.1	Page Received	1 = Indicates that a new page has been received as and the received code word has been loaded into register 5 (base pages) or register 8 (next pages) as specified in clause 28 of 802.3. This bit will be cleared on read. If bit 16.1 is set, the Page Received bit will also be cleared when mr_page_rx = false or transmit_disable = true.	RO LH	0
6.0	Link Partner A/N Able	1 = Link partner is auto-negotiation able. 0 = Link partner is not auto-negotiation able.	RO	0

1. RO = Read Only
   LH = Latching High

Table 45. Auto-Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type [1]	Default
7.15	Next Page (NP)	1 = Additional next pages follow 0 = Last page	R/W	0
7.14	Reserved	Write as 0, ignore on read	RO	0
7.13	Message Page (MP)	1 = Message page 0 = Unformatted page	R/W	1
7.12	Acknowledge 2 (ACK2)	1 = Will comply with message. 0 = Can not comply with message.	R/W	0
7.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero. 0 = Previous value of the transmitted Link Code Word equalled logic one.	R/W	0
7.10:0	Message/ Unformatted Code Field		R/W	00000000001

1. R/W = Read/Write
   RO = Read Only

Table 46. Auto-Negotiation Link Partner Next Page Receive Register (Address 8)

Bit	Name	Description	Type [1]	Default
8.15	Next Page (NP)	1 = Link Partner has additional next pages to send. 0 = Link Partner has no additional next pages to send.	RO	0
8.14	Acknowledge (ACK)	1 = Link Partner has received Link Code Word from LXT97x2. 0 = Link Partner has not received Link Code Word from LXT97x2.	RO	0
8.13	Message Page (MP)	1 = Page sent by the Link Partner is a Message Page. 0 = Page sent by the Link Partner is an Unformatted Page.	RO	0
8.12	Acknowledge 2 (ACK2)	1 = Link Partner will comply with the message. 0 = Link Partner can not comply with the message.	RO	0
8.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero. 0 = Previous value of the transmitted Link Code Word equalled logic one.	RO	0
8.10:0	Message/ Unformatted Code Field		RO	0

1. RO = Read Only

Note: Registers 9, 10 and 15 are not implemented.
These registers only apply to 100BASE-T2 and 1000BASE-T, neither of which are supported by this device.

Table 47. Port Configuration Register (Address 16, Hex 10)

Bit	Name	Description	Type	Default
16.15	Reserved	This bit is ignored by the LXT97x2.	R/W	0
16.14	Force Link Pass	1 = Forces internal registers and state machines to Link Pass state. 0 = Normal operation.	R/W	0
16.13	Transmit Disable	1 = Disable Twisted-Pair transmitter. 0 = Normal Operation.	R/W	0
16.12	Bypass Scramble (100BASE-TX)	1 = Bypass Scrambler and Descrambler. 0 = Normal Operation.	R/W	0
16.11	Reserved	This bit is ignored by the LXT97x2.	R/W	0
16.10	Jabber (10BASE-T)	1 = Disable Jabber. 0 = Normal operation.	R/W	0
16.9	SQE (10BASE-T)	This bit is ignored by the LXT97x2. 1 = Enable Heart Beat. 0 = Disable Heart Beat.	R/W	0
16.8	TP Loopback (10BASE-T)	1 = Disable TP loopback during half duplex operation. 0 = Normal Operation.	R/W	1
16.7	Reserved	This bit is ignored by the LXT97x2.	R/W	0
16.6	FIFO Size	0 = FIFO allows packets up to 2 KBytes. 1 = FIFO allows packets up to 8 KBytes. Note: This assumes a 100 ppm difference between the reference clock and the recovered clock.	R/W	0
16.5	Preamble Enable	0 = Set RX_DV high coincident with SFD. 1 = Set RX_DV high and RXD=preamble when CRS is asserted.	R/W	0
16.4	Reserved	Write as zero. Ignore on read.	R/W	0
16.3	Reserved	Write as zero. Ignore on read.	R/W	0
16.2	Far End Fault Transmit Enable	1 = Enable Far End Fault code transmission. 0 = Disable Far End Fault code transmission.	R/W	1
16.1	Alternate NP feature	1 = Enable alternate auto-negotiate next page feature. 0 = Disable alternate auto-negotiate next page feature.	R/W	0
16.0	Fiber Select	1 = Select fiber mode for this port. 0 = Select TP mode for this port.	R/W	Note 2

1. R/W = Read /Write
2. The default value of bit 16.0 is determined at Reset by the SD/$\overline{\text{TP}}$*n* pin for the respective port. If SD/$\overline{\text{TP}}$*n* is tied Low, the default value of bit 16.0 = 0. If SD/$\overline{\text{TP}}$*n* is not tied Low, the default value of bit 16.0 = 1. Refer to Reset discussion on page 27.

Table 48. Quick Status Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default
17.15	Reserved	Always 0	RO	0
17.14	10/100 Mode	1 = LXT97x2 is operating in 100BASE-TX mode. 0 = LXT97x2 is not operating 100BASE-TX mode.	RO	0
17.13	Transmit Status	1 = LXT97x2 is transmitting a packet 0 = LXT97x2 is not transmitting a packet	RO	0

1. RO = Read Only

Table 48. Quick Status Register (Address 17, Hex 11) (Continued)

Bit	Name	Description	Type [1]	Default
17.12	Receive Status	1 = LXT97x2 is receiving a packet 0 = LXT97x2 is not receiving a packet	RO	0
17.11	Collision Status	1 = Collision is occurring 0 = No collision	RO	0
17.10	Link	1 = Link is up 0 = Link is down	RO	0
17.9	Duplex Mode	1 = Full duplex 0 = Half duplex	RO	0
17.8	Auto-Negotiation	1 = LXT97x2 is in Auto-Negotiation Mode 0 = LXT97x2 is in manual mode	RO	0
17.7	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed This bit is only valid when auto-negotiate is enabled, and is equivalent to bit 1.5.	RO	0
17.6	Reserved	Ignore	RO	0
17.5	Polarity	1= Polarity is reversed 0= Polarity is not reversed	RO	0
17.4	Pause	1 = LXT97x2 is Pause capable 0 = LXT97x2 is not Pause capable This bit is equivalent to bit 4.10.	RO	
17:3	Error	1 = Error occurred (Remote Fault, X,Y,Z) 0 = No error occurred	RO	0
17:2:0	Reserved	Ignore	RO	0

1. RO = Read Only

Table 49. Interrupt Enable Register (Address 18, Hex 12)

Bit	Name	Description	Type [1]	Default
18.15:8	Reserved	Write as 0; ignore on read.	R/W	N/A
18.7	ANMSK	Mask for Auto-Negotiate Complete 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.6	SPEEDMSK	Mask for Speed Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.5	DUPLEXMSK	Mask for Duplex Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.4	LINKMSK	Mask for Link Status Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt	R/W	0
18.3	Reserved	Write as 0, ignore on read.	R/W	0

1. R/W = Read /Write

Table 49. Interrupt Enable Register (Address 18, Hex 12) (Continued)

Bit	Name	Description	Type [1]	Default
18.2	Reserved	Write as 0, ignore on read.	R/W	0
18.1	INTEN	1 = Enable interrupts on this port. 0 = Disable interrupts on this port.	R/W	0
18.0	TINT	1 = Force interrupt on $\overline{\text{MDINT}}$. 0 = Normal operation	R/W	0
1. R/W = Read /Write				

Table 50. Interrupt Status Register (Address 19, Hex 13)

Bit	Name	Description	Type [1]	Default
19.15:8	Reserved	Ignore	RO	N/A
19.7	ANDONE	Auto-Negotiation Status 1= Auto-Negotiation has completed 0= Auto-Negotiation has not completed	RO/SC	N/A
19.6	SPEEDCHG	Speed Change Status 1 = A Speed Change has occurred since last reading this register 0 = A Speed Change has not occurred since last reading this register	RO/SC	0
19.5	DUPLEXCHG	Duplex Change Status 1 = A Duplex Change has occurred since last reading this register 0 = A Duplex Change has not occurred since last reading this register	RO/SC	0
19.4	LINKCHG	Link Status Change Status 1 = A Link Change has occurred since last reading this register 0 = A Link Change has not occurred since last reading this register	RO/SC	0
19.3	Reserved	Ignore	RO/SC	0
19.2	MDINT	1 = Indicates MII interrupt pending 0 = Indicates no MII interrupt pending	RO/SC	
19.1:0	Reserved	Ignore	RO	0
1. R/W = Read/Write RO = Read Only SC = Self Clearing when read.				

Table 51. LED Configuration Register (Address 20, Hex 14)

Bit	Name	Description	Type [1]	Default
20.15:12	LED1 Programming bits	0000 = Display Speed Status (Continuous, Default) 0001 = Display Transmit Status (Stretched) 0010 = Display Receive Status (Stretched) 0011 = Display Collision Status (Stretched) 0100 = Display Link Status (Continuous) 0101 = Display Duplex Status (Continuous)[5] 0110 = Reserved 0111 = Display Receive or Transmit Activity (Stretched) 1000 = Test mode- turn LED on (Continuous) 1001 = Test mode- turn LED off (Continuous) 1010 = Test mode- blink LED fast (Continuous) 1011 = Test mode- blink LED slow (Continuous) 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3,5] 1111 = Reserved	R/W	0000
20.11:8	LED2 Programming bits	0000 = Display Speed Status (Continuous, Default) 0001 = Display Transmit Status (Stretched) 0010 = Display Receive Status (Stretched) 0011 = Display Collision Status (Stretched) 0100 = Display Link Status (Continuous) 0101 = Display Duplex Status (Continuous)[5] 0110 = Reserved 0111 = Display Receive or Transmit Activity (Stretched) 1000 = Test mode- turn LED on (Continuous) 1001 = Test mode- turn LED off (Continuous) 1010 = Test mode- blink LED fast (Continuous) 1011 = Test mode- blink LED slow (Continuous) 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3,5] 1111 = Reserved	R/W	0100
20.7:4	LED3 Programming bits	0000 = Display Speed Status (Continuous, Default) 0001 = Display Transmit Status (Stretched) 0010 = Display Receive Status (Stretched) 0011 = Display Collision Status (Stretched) 0100 = Display Link Status (Continuous) 0101 = Display Duplex Status (Continuous)[5] 0110 = Reserved 0111 = Display Receive or Transmit Activity (Stretched) 1000 = Test mode- turn LED on (Continuous) 1001 = Test mode- turn LED off (Continuous) 1010 = Test mode- blink LED fast (Continuous) 1011 = Test mode- blink LED slow (Continuous) 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3,5] 1111 = Reserved	R/W	0010

1. R/W = Read /Write
   RO = Read Only
   LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up.
   The secondary LED driver (Receive or Activity) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full duplex.
   Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Duplex LED may be active for a brief time after loss of link.

Table 51. LED Configuration Register (Address 20, Hex 14) (Continued)

Bit	Name	Description	Type [1]	Default
20.3:2	LEDFREQ	00 = Stretch LED events to 30 ms 01 = Stretch LED events to 60 ms 10 = Stretch LED events to 100 ms 11 = Reserved	R/W	00
20.1	PULSE-STRETCH	0 = Disable pulse stretching of all LEDs 1 = Enable pulse stretching of all LEDs	R/W	1
20.0	Reserved		R/W	0

1. R/W = Read /Write
   RO = Read Only
   LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up.
   The secondary LED driver (Receive or Activity) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full duplex.
   Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Duplex LED may be active for a brief time after loss of link.

Table 52. Transmit Control Register #1 (Address 28)

Bit	Name	Description	Type	Default
28.12:4	Reserved	Ignore.	R/W	N/A
28.3:2	Bandwidth Control	00 = Nominal Differential Amp Bandwidth 01 = Slower 10 = Fastest 11 = Faster	R/W	00
28.1:0	Risetime Control	00 = 2.5ns 01 = 3.1ns 10 = 3.7ns 11 = 4.3ns	R/W	Note 2

1. RO = Read Only.
   R/W = Read/Write.
2. The default setting of bits 28.1:0 (Risetime) is determined by pins 91 and 94 TxSLEW<1:0>.

Table 53. Transmit Control Register #2 (Address 30)

Bit	Name	Description	Type	Default
30.15:14	Reserved		R/W	N/A
30.13	Increase Driver Amplitude	1 = Increase Driver Amplitude 5% in all modes. 0 = Normal operation.	R/W	0
30.12:0	Reserved		R/W	N/A

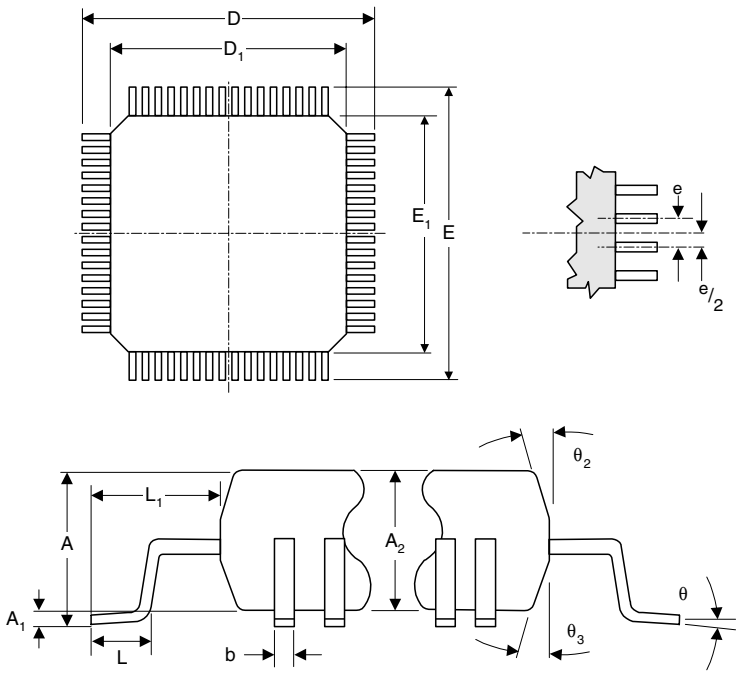
1. RO = Read Only.

6.0 Package Specifications

Figure 42. LXT97x2 PQFP Package Specification

208-Pin Plastic Quad Flat Package

- Part Number LXT9762HC (6-port model)
- Part Number LXT9782HC (8-port model)
- Commercial Temperature Range (0°C to 70°C)

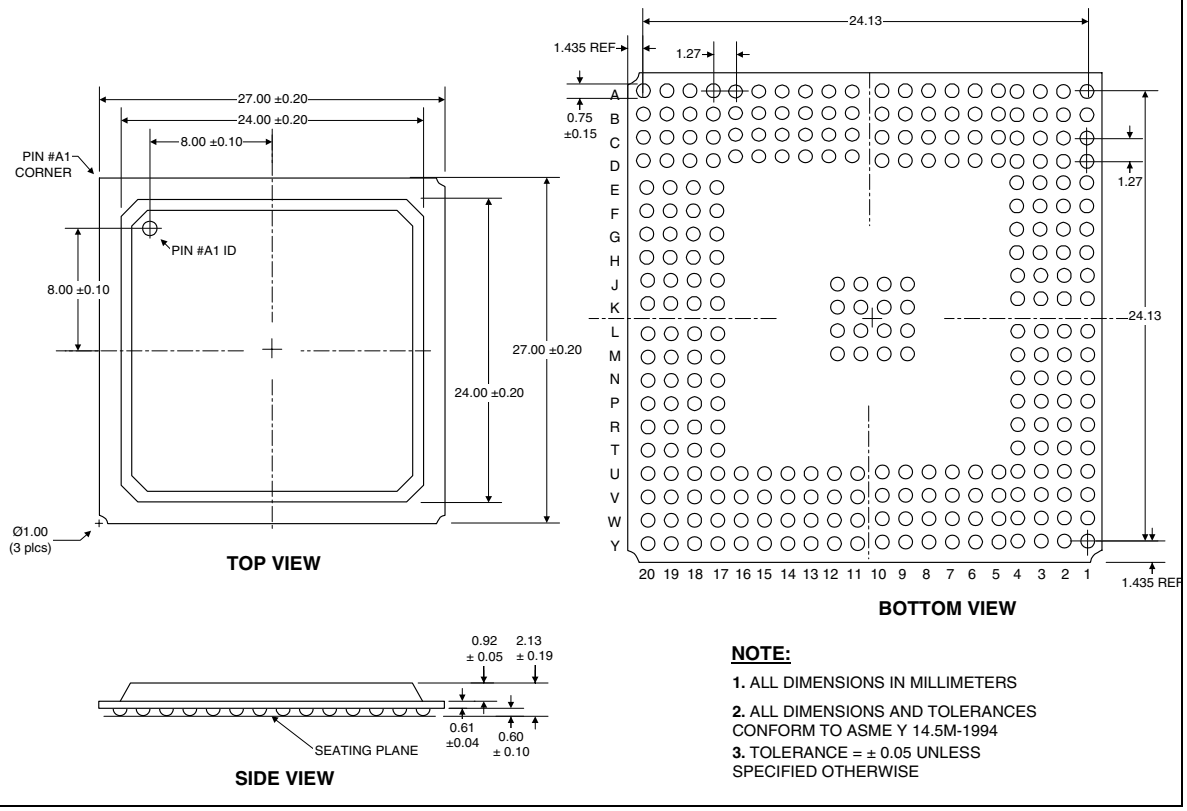


Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°

Figure 43. LXT97x2 PBGA Package Specification

272-Lead Plastic Ball Grid Array

- Part Number LXT9782BC (8-port model)
- Commercial Temperature Range (0°C to 70°C)



NOTE:

1. ALL DIMENSIONS IN MILLIMETERS
2. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994
3. TOLERANCE = ± 0.05 UNLESS SPECIFIED OTHERWISE