

8-Bit μ p-compatible D/A converter

NE/SE5018/5019

DESCRIPTION

The NE/SE5018/19 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches which are controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the \overline{LE} input is in the low state. When \overline{LE} goes high, the input data present at the moment of transition is latched and retained until \overline{LE} again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to \pm LSB (0.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 6800 and many other μ Ps

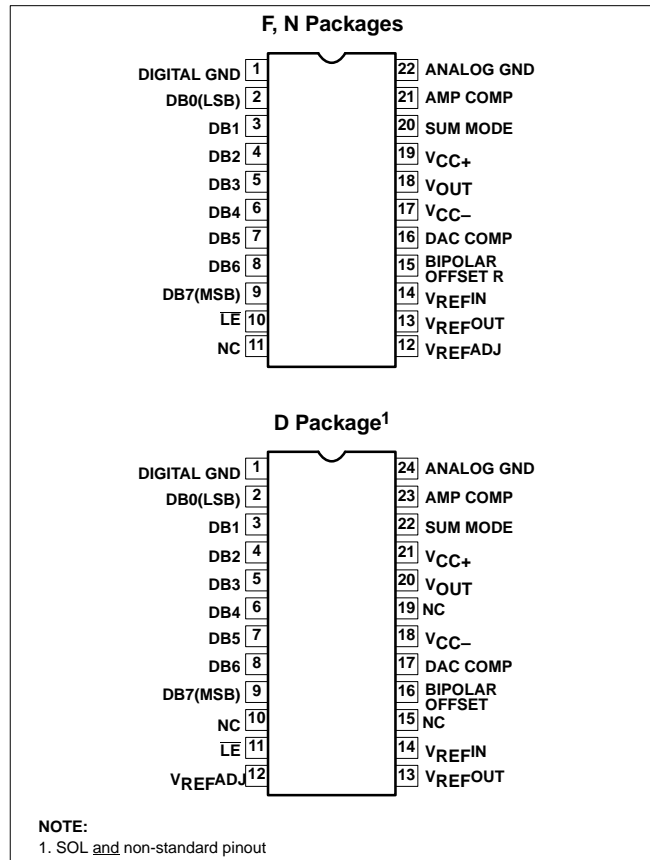
APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG # |
|--|-------------------|--------------|-------|
| 22-Pin Ceramic Dual In-Line Package (CERDIP) | 0 to +70°C | NE5018/5019F | 0585B |
| 22-Pin Ceramic Dual In-Line Package (CERDIP) | -55°C to +125°C | SE5018/5019F | 0585B |
| 22-Pin Plastic Dual In-Line Package (DIP) | 0 to +70°C | NE5018/5019N | 0409B |
| 22-Pin Plastic Dual In-Line Package (DIP) | -55°C to +125°C | SE5018/5019N | 0409B |
| 24-Pin Small Outline Large (SOL) Package | 0 to +70°C | NE5018/5019D | 0173D |

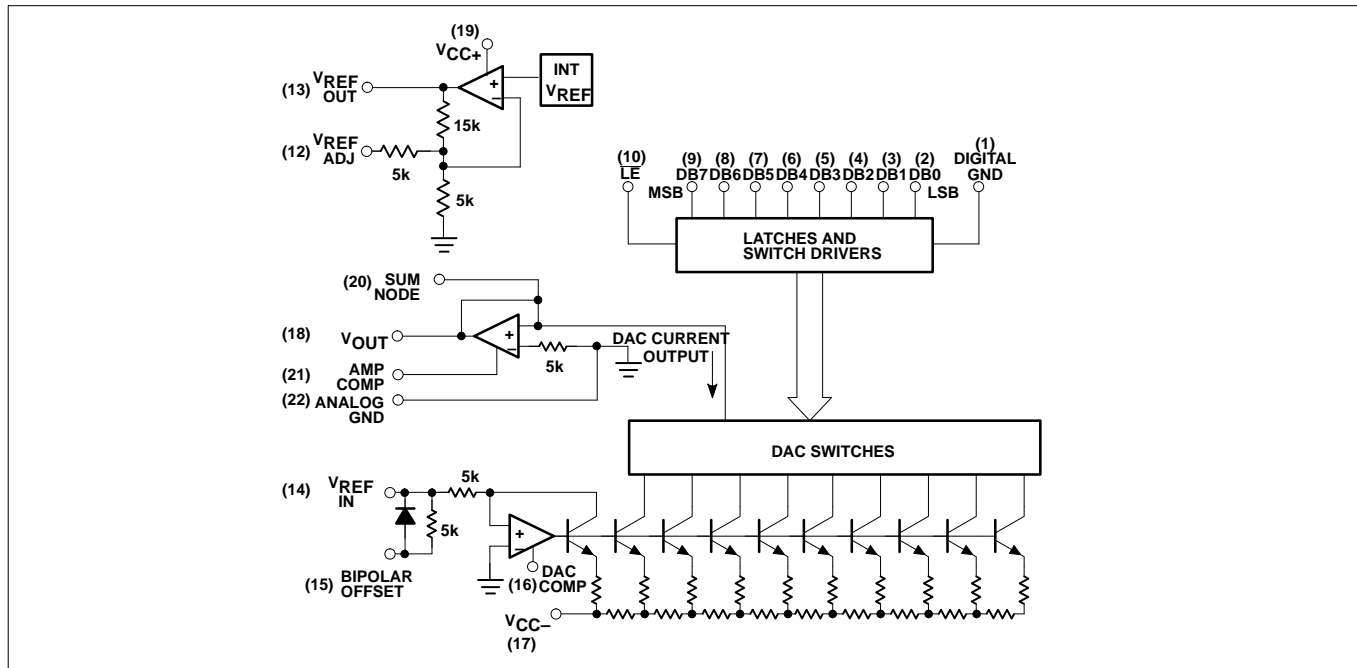
PIN CONFIGURATIONS



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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---------------|--|----------------|------------|
| V_{CC+} | Positive supply voltage | 18 | V |
| V_{CC-} | Negative supply voltage | -18 | V |
| V_{IN} | Logic input voltage | 0 to 18 | V |
| $V_{REF IN}$ | Voltage at $V_{REF IN}$ input | 12 | V |
| $V_{REF ADJ}$ | Voltage at $V_{REF ADJ}$ | 0 to V_{REF} | V |
| V_{SUM} | Voltage at sum node | 12 | V |
| $I_{REF SC}$ | Short-circuit current to ground at $V_{REF OUT}$ | Continuous | |
| $I_{OUT SC}$ | Short-circuit current to ground or either supply at V_{OUT} | Continuous | |
| P_D | Maximum power dissipation, $T_A=25^\circ C$ (still-air) ¹ | | |
| | F package | 1740 | mW |
| | N package | 2190 | mW |
| | D package | 1600 | mW |
| T_A | Operating temperature range | | |
| | SE5018 | -55 to +125 | $^\circ C$ |
| | NE5018 | 0 to +70 | $^\circ C$ |
| T_{STG} | Storage temperature range | -65 to +150 | $^\circ C$ |
| T_{SOLD} | Lead soldering temperature (10 seconds) | 300 | $^\circ C$ |

NOTES:

- Derate above $25^\circ C$ at the following rates:
 F package at $13.9mW/^\circ C$
 N package at $17.5mW/^\circ C$
 D package at $12.8mW/^\circ C$

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DC ELECTRICAL CHARACTERISTICS

$V_{CC+}=+15V$, $V_{CC-}=-15V$, SE5018. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, NE5018. $0^{\circ}C \leq T_A \leq 70^{\circ}C$, unless otherwise specified. ¹ Typical values are specified at $25^{\circ}C$.

| SYMBOL | PARAMETER | TEST CONDITIONS | NE/SE5018 | | | NE/SE5019 | | | UNIT |
|----------------|---|--|-----------|-------|------------|-----------|-------|-----------|------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Resolution | | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
| | Monotonicity | | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
| | Relative accuracy | | | | ± 0.19 | | | ± 0.1 | %FS |
| V_{CC+} | Positive supply voltage | | 11.4 | 15 | | 11.4 | 15 | | V |
| V_{CC-} | Negative supply voltage | | -11.4 | -15 | | -11.4 | -15 | | V |
| $V_{IN(1)}$ | Logic "1" input voltage | Pin 1=0V | 2.0 | | | 2.0 | | | V |
| $V_{IN(0)}$ | Logic "0" input voltage | Pin 1=0V | | | 0.8 | | | 0.8 | V |
| $I_{IN(1)}$ | Logic "1" input current | Pin 1=0V, $2V < V_{IN} < 18V$ | | 0.1 | 10 | | 0.1 | 10 | μA |
| $I_{IN(0)}$ | Logic "0" input current | Pin 1=0V, $-5V < V_{IN} < 0.8V$ | | -2.0 | -10 | | -2.0 | -10 | μA |
| V_{FS} | Full-scale output | Unipolar mode, $V_{REF}=5.000V$, all bits high, $T_A=25^{\circ}C$ | 9.50 | | 10.5 | 9.50 | | 10.5 | V |
| $+V_{FS}$ | Full-scale output | Bipolar mode, $V_{REF}=5.000V$ all bits high, $T_A=25^{\circ}C$ | 4.75 | | 5.25 | 4.75 | | 5.25 | V |
| $-V_{FS}$ | Negative full scale | Bipolar mode, $V_{REF}=5.000V$, all bits low, $T_A=25^{\circ}C$ | -5.25 | | -4.75 | -5.25 | | -4.75 | V |
| V_{ZS} | Zero-scale Output | Unipolar mode, $V_{REF}=5.000V$ all bits low, $T_A=25^{\circ}C$ | -30 | | +30 | -30 | | +30 | mV |
| I_{OS} | Output short circuit current | $T_A=25^{\circ}C$ $V_{OUT}=0V$ | | 15 | 40 | | 15 | 40 | mA |
| $PSR^{+(OUT)}$ | Output power supply rejection (+) | $V=-15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF IN}=5.000V$ | | 0.001 | 0.01 | | 0.001 | 0.01 | %FS %VS |
| $PSR^{-(OUT)}$ | Output power supply rejection (-) | $V+ = -15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF IN}=5.000V$ | | 0.001 | 0.01 | | 0.001 | 0.01 | %FS %VS |
| TC_{FS} | Full-scale temperature coefficient | $V_{REF IN}=5.000V$ | | 20 | | | 20 | | ppm/ $^{\circ}C$ |
| TC_{ZS} | Zero-scale temperature coefficient | | | 5 | | | 5 | | ppm/ $^{\circ}C$ |
| I_{REF} | Reference output current | | | | 3 | | | 3 | mA |
| I_{REFSC} | Reference short circuit current | $T_A=25^{\circ}C$ $V_{REF OUT}=0V$ | | 15 | 30 | | 15 | 30 | mA |
| $PSR^{+(REF)}$ | Reference power supply rejection (+) | $V=-15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF}=1.0mA$ | | 0.003 | 0.01 | | 0.003 | 0.01 | %VR/%VS |
| $PSR^{-(REF)}$ | Reference power supply rejection (-) | $V+ = -15V$, $-13.5V \leq V- \leq -16.5V$, $I_{REF}=1.0mA$ | | 0.003 | 0.01 | | 0.003 | 0.01 | %VR/%VS |
| V_{REF} | Reference voltage | $I_{REF}=1.0mA$ $T_A=25^{\circ}C$ | 4.9 | 5.0 | 5.25 | 4.9 | 5.0 | 5.25 | V |
| TC_{REF} | Reference voltage temperature coefficient | $I_{REF}=1.0mA$ | | 60 | | | 60 | | ppm/ $^{\circ}C$ |
| Z_{IN} | DAC $V_{REF IN}$ input impedance | $I_{REF}=1.0mA$, $T_A=25^{\circ}C$ | 4.15 | 5.0 | 5.85 | 4.15 | 5.0 | 5.85 | k Ω |
| I_{CC+} | Positive supply current | $V_{CC+}=15V$ | | 7 | 14 | | 7 | 14 | mA |
| I_{CC-} | Negative supply current | $V_{CC-}=-15V$ | | -10 | -15 | | -10 | -15 | mA |
| P_D | Power dissipation | $I_{REF}=1.0mA$, $V_{CC}=\pm 15V$ | | 255 | 435 | | 255 | 435 | mW |

NOTES:

1. Refer to Figure 1.

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AC ELECTRICAL CHARACTERISTICS¹

$V_{CC} = \pm 15V, T_A = 25^\circ C$

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | NE/SE5018/19 | | | UNIT |
|------------|--------------------------|-----------------|-----------------|--|--------------|-----|-----|---------|
| | | | | | Min | Typ | Max | |
| t_{SLH} | Settling time | $\pm 1/2LSB$ | Input | All bits low-to-high ² | | 1.8 | | μs |
| t_{SHL} | Settling time | $\pm 1/2LSB$ | Input | All bits high-to-low ³ | | 2.3 | | μs |
| t_{PLH} | Propagation delay | Output | Input | All bits switched low-to-high ² | | 300 | | ns |
| t_{PHL} | Propagation delay | Output | Input | All bits switched high-to-low ³ | | 150 | | ns |
| t_{PLSB} | Propagation delay | Output | Input | 1 LSB change ^{2, 3} | | 150 | | ns |
| t_{PLH} | Propagation delay | Output | \overline{LE} | Low-to-high transition ⁴ | | 300 | | ns |
| t_{PHL} | Propagation delay | Output | \overline{LE} | High-to-low transition ⁵ | | 150 | | ns |
| t_S | Setup time | \overline{LE} | Input | 1, 6 | 100 | | | ns |
| t_H | Hold time | Input | \overline{LE} | 1, 6 | 50 | | | ns |
| t_{PW} | Latch enable pulse width | | | 1, 6 | 150 | | | ns |

NOTES:

1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. For reference currents >3mA, use of an external buffer is required.

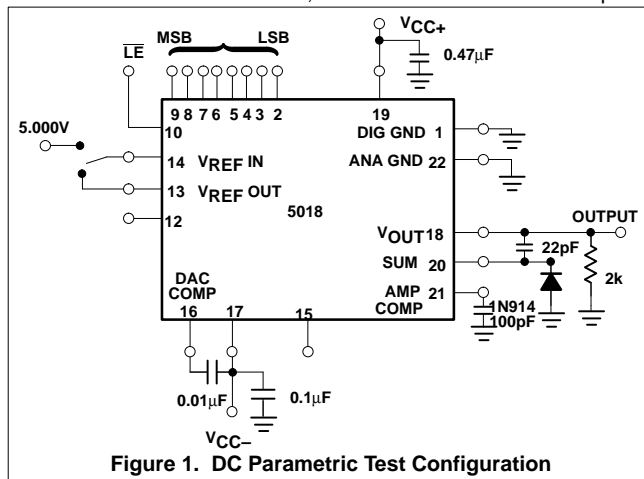


Figure 1. DC Parametric Test Configuration

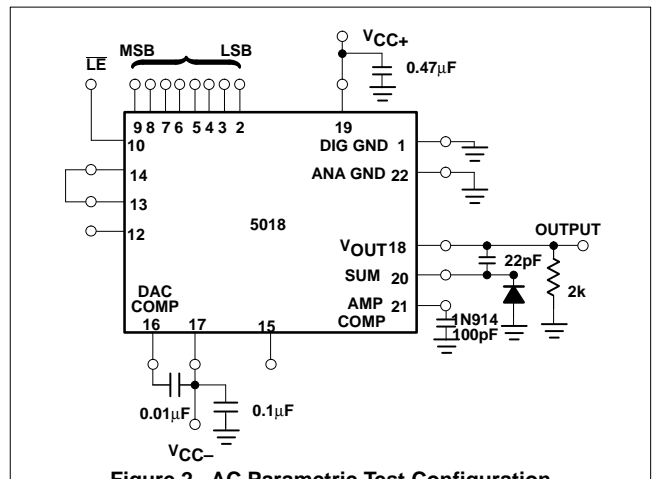


Figure 2. AC Parametric Test Configuration

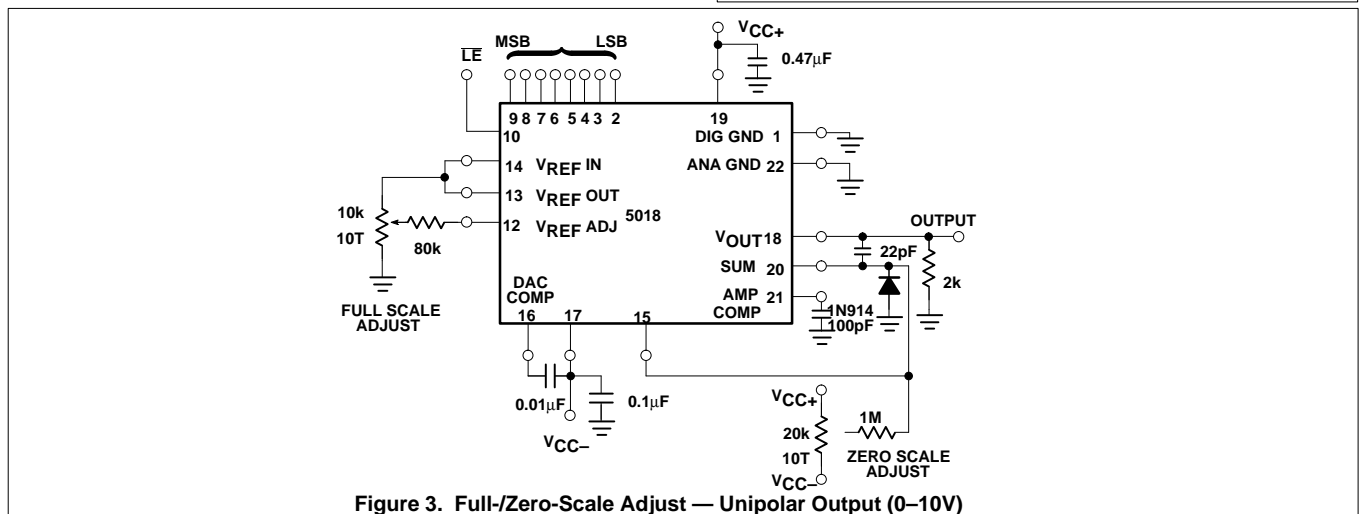


Figure 3. Full/Zero-Scale Adjust — Unipolar Output (0–10V)

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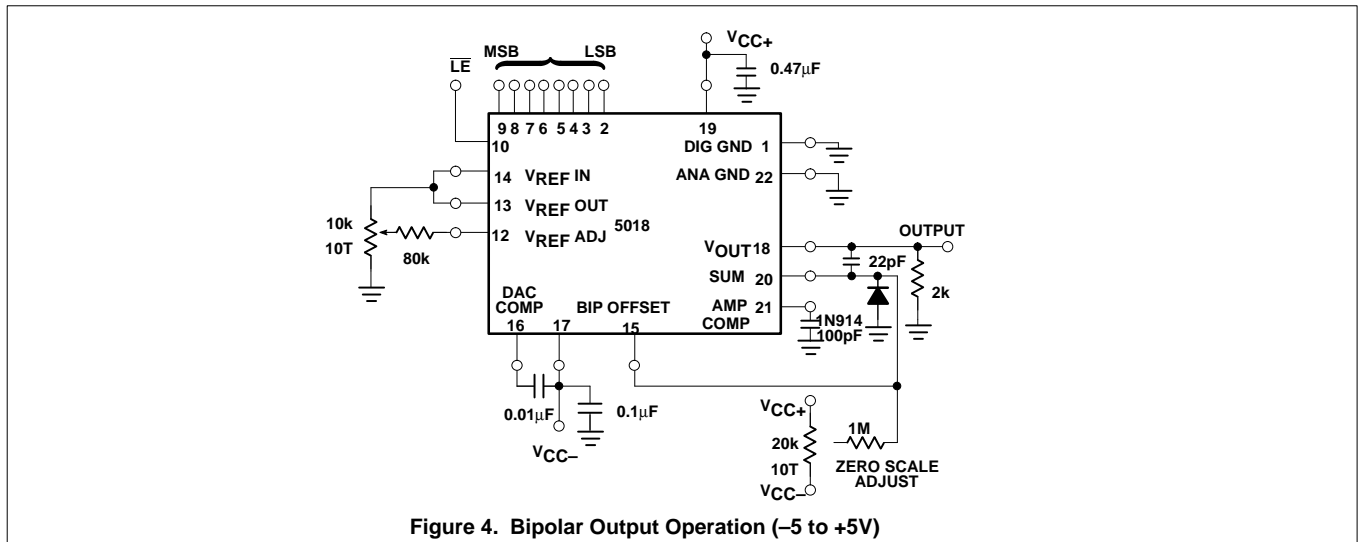


Figure 4. Bipolar Output Operation (-5 to +5V)

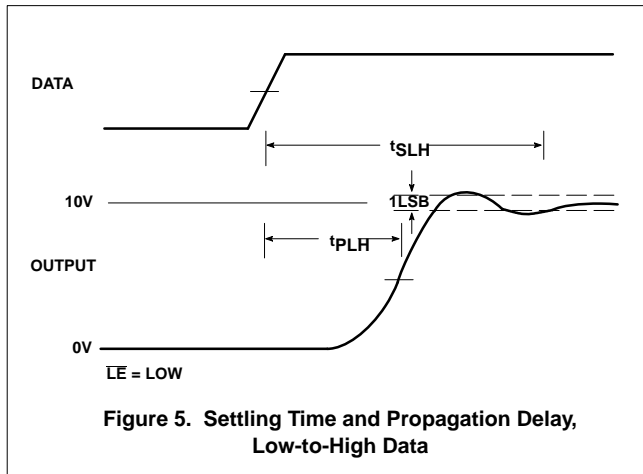


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

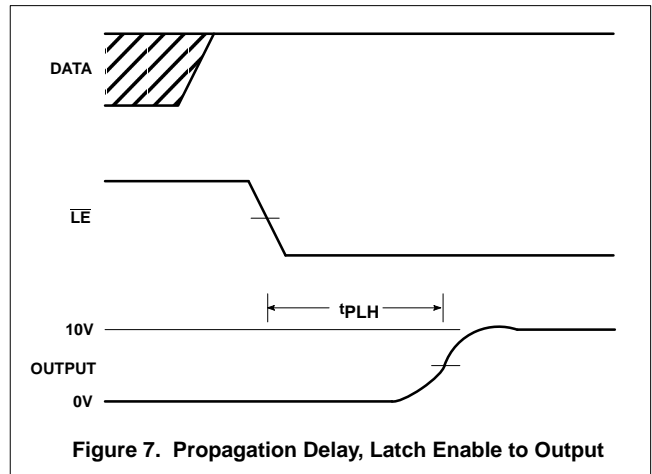


Figure 7. Propagation Delay, Latch Enable to Output

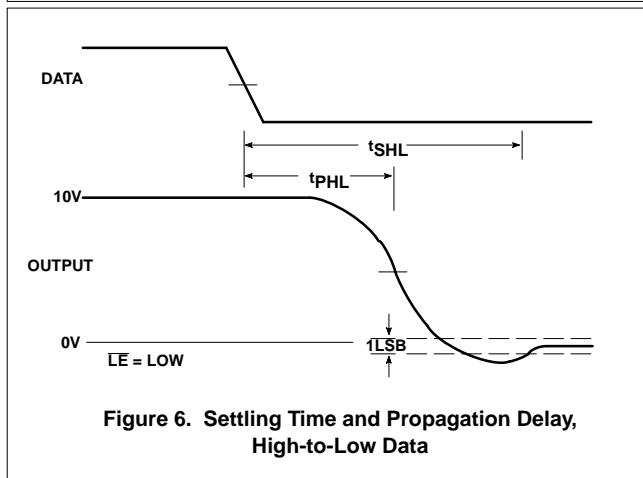


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

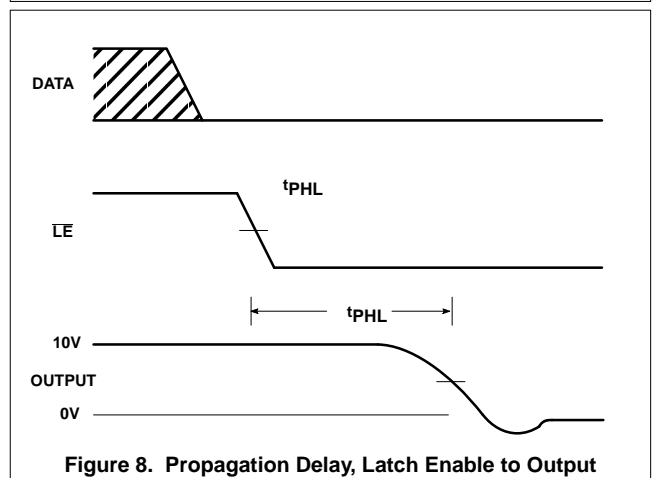


Figure 8. Propagation Delay, Latch Enable to Output

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