Data Sheet No. PD60184-D

International
IOR Rectifier

IR2167(S)

PFC BALLAST CONTROL IC

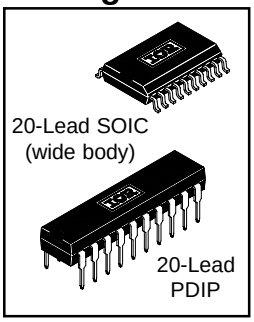
Features

- PFC, Ballast Control and Half Bridge Driver in One IC
- Critical Conduction Mode Boost Type PFC
- No PFC Current Sense Resistor Required
- Programmable Preheat Time & Frequency
- Programmable Ignition Ramp
- Programmable Over-Current
- Internal Fault Counter
- End-of-Life Protection
- Lamp Filament Sensing & Protection
- Capacitive Mode Protection
- Brown-Out Protection
- Dynamic Restart
- Automatic Restart for Lamp Exchange
- Thermal Overload Protection
- Programmable Deadtime
- Internal 15.6V Zener Clamp Diode on VCC
- Micropower Startup (150μA)
- Latch Immunity and ESD Protection

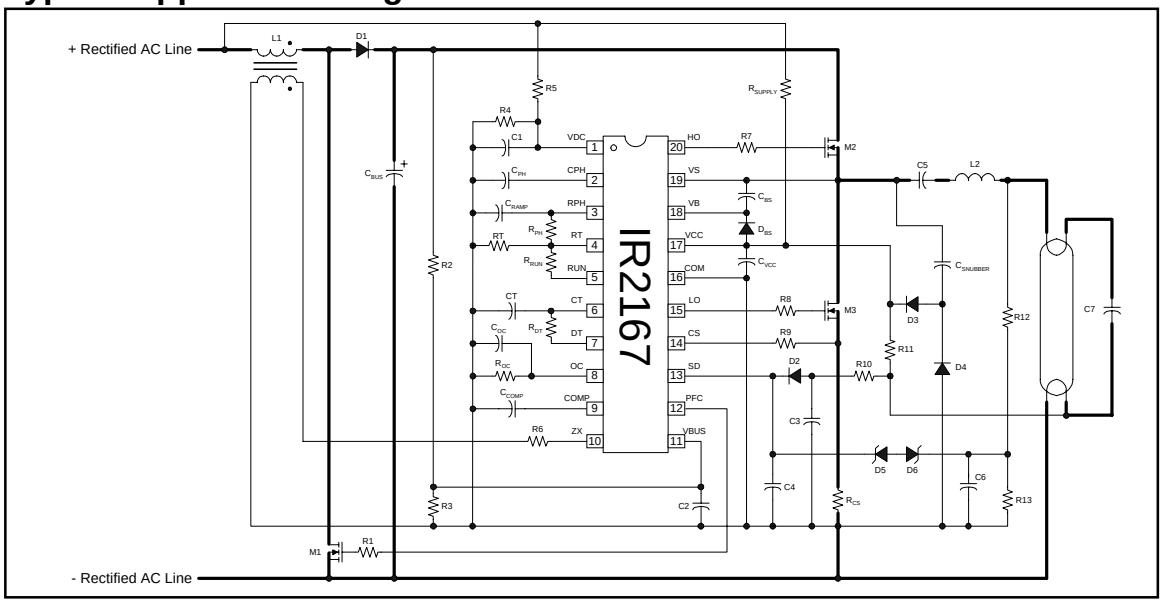
Description

The IR2167 is a fully integrated, fully protected 600V ballast control IC designed to drive all types of fluorescent lamps. PFC circuitry provides for high PF, low THD and DC Bus regulation. Externally programmable features such as preheat time & frequency, ignition ramp characteristics, and running mode operating frequency provide a high degree of flexibility for the ballast design engineer. Comprehensive protection features such as protection from failure of a lamp to strike, filament failures, low AC line conditions, thermal overload, or lamp failure during normal operation, as well as an automatic restart function, have been included in the design. The heart of the ballast control section is a variable frequency oscillator with externally programmmable deadtime. Precise control of a 50% duty cycle is accomplished using a T-flip-flop. The IR2167 is available in both 20-pin DIP and 20-pin wide body SOIC packages.

Packages



Typical Application Diagram



Please note that this datasheet contains advance information that could change before the product is released to production.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{PFC}	PFC gate driver output voltage		-0.3	V_{CC} + 0.3	
I_{OMAX}	Max. allowable output current (HO,LO,PFC) due to external power transistor miller effect		-500	500	mA
I_{RT}	R_T pin current		-5	5	
V_{CT}	C_T pin voltage		-0.3	6.5	V
V_{DC}	VDC pin voltage		-0.3	V_{CC} + 0.3	
I_{CPH}	CPH pin current		-5	5	mA
I_{RPH}	RPH pin current		-5	5	
I_{RUN}	RUN pin current		-5	5	
I_{DT}	Deadtime pin current		-5	5	
V_{CS}	Current sense pin voltage		-0.3	6.5	V
I_{CS}	Current sense pin current		-5	5	mA
I_{OC}	Over-current threshold pin current		-5	5	
I_{SD}	Shutdown pin current		-5	5	
V_{BUS}	DC bus sensing input voltage		-0.3	V_{CC}	V
I_{ZX}	PFC inductor current, zero crossing detection input		-5	5	mA
I_{COMP}	PFC error amplifier compensation current		-5	5	
I_{CC}	Supply current (note 1)		-20	20	
dV/dt	Allowable offset supply voltage slew ratet		-50	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(20 lead PDIP)	—	1.50	W
		(20 lead SOIC)	—	1.25	
Rth_{JA}	Thermal resistance, junction to ambient	(20 lead PDIP)	—	85	°C/W
		(20 lead SOIC)	—	90	
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead

Symbol	Definition	Min.	Max.	Units
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady state high side floating supply offset voltage	-3.0	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	Note 2	10	mA
V_{DC}	V_{DC} lead voltage	0	VCC	V
I_{SD}	Shutdown lead current	-1	1	mA
I_{CS}	Current sense lead current	-1	1	
C_T	C_T lead capacitance	220	—	pF
R_{DT}	Deadtime resistance	1.0	—	kΩ
I_{RT}	R_T lead current (Note 3)	-500	-50	uA
I_{RPH}	RPH lead current (Note 3)	0	450	
I_{RUN}	RUN lead current (Note 3)	0	450	
I_{ZX}	Zero crossing detection lead current	-1	1	mA
T_J	Junction temperature	-40	125	°C

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 16.9kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 2.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.4	11.4	12.5	V	V_{CC} rising from 0V
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	2.0	2.1	2.1		
I_{QCCUV}	UVLO mode quiescent current	—	250	400	µA	V_{CC} < V_{CCUV-}
I_{QCCFLT}	Fault-mode quiescent current	—	100	350		SD = 5V, CS = 2V or Tj > T_{SD}
I_{QCC}	Quiescent V_{CC} supply current	1.9	3.3	4.5	mA	R_T no connection, C_T connected to COM
I_{CC50K}	V_{CC} supply current, f = 48kHz	4.0	5.0	6.0		
V_{CLAMP}	V_{CC} zener clamp voltage	14.0	15.6	16.5	V	ICC = 10mA

Note 2: Sufficient current should be supplied to the VCC pin to keep the internal 15.6V zener clamp diode on this pin regulating its voltage.

Note 3: Due to the fact that the RT pin is a voltage-controlled current source, the total RT pin current is the sum of all of the parallel current sources connected to that pin. During the preheat mode, the total current flowing out of the RT pin consists of the RPH pin current plus the current due to the RT resistor. During the run mode, the total RT pin current consists of the RUN pin current plus the current due to the RT resistor.

Electrical Characteristics (cont.)

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 16.9kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 2.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

Floating Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{QBS0}	Quiescent V_{BS} supply current	—	0	10.0	µA	V_{HO} = V_S
I_{LK}	Offset supply leakage current	—	0	50		V_B = V_S = 600V

PFC Error Amplifier Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BUS}	VBUS sense input threshold	3.7	4.0	4.3		V
I_{VBUS}	VBUS sense input bias current	—	—	0.1		µA
gm	Error amplifier transconductance	40	90	130	µmho	RUN mode operation
I_{SOURCE}	Error amplifier output current sourcing	15	30	50	µA	V_{BUS} = 3V
I_{SINK}	Error amplifier output current sinking	5	30	50		V_{BUS} = 5V
$V_{OH(EA)}$	Error amplifier output voltage swing (Hi state)	12.5	13.5	14.5	V	V_{BUS} = 3V
$V_{0L(EA)}$	Error amplifier output voltage swing (Lo state)	—	0.25	0.4		V_{BUS} = 5V

PFC Over Voltage Comparator

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{0V}	Over voltage comparator threshold	4.0	4.3	4.5	V	

PFC Zero Current Detector

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{ZX}	ZX lead comparator threshold voltage	1.7	2.0	2.3	V	
V_{ZXhys}	ZX lead comparator hysterisis	400	300	300	mV	
$V_{ZXclamp+}$	ZX lead clamp voltage (high state)	6.0	7.5	9.0	V	I_{ZX} = 1mA

Oscillator, Ballast Control, I/O Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
f_{osc}	Oscillator frequency	41	44	47	kHz	R_T = 16.9kΩ, R_{DT} = 6.1kΩ, C_T=470pF
V_{CT+}	Upper C_T ramp voltage threshold	3.6	4.0	4.4	V	
V_{CT-}	Lower C_T ramp voltage threshold	1.8	2.0	2.2		
V_{RT}	R_T lead voltage	1.8	2.0	2.2		
t_{DLO}	LO output deadtime	2.0	2.4	2.6	µsec	
t_{DHO}	HO output deadtime	2.0	2.4	2.6		

Preheat Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{CPH+}	CPH lead charging current	2.5	2.8	3.2	µA	V_{CPH} = 0V
I_{CPH-}	CPH lead discharge current	50	175	350	nA	V_{CPH} = 0V
V_{CPHIGN}	CPH lead Ignition mode threshold voltage	3.6	4.1	4.4	V	
V_{CPHRUN}	CPH lead run mode threshold voltage	4.7	5.1	5.5		
$V_{CPHCLMP}$	CPH lead clamp voltage	6	10	11.5		I_{CPH} = 1µA

Electrical Characteristics (cont.)

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 16.9kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 2.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

RPH Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{RPHLK}	Open circuit RPH lead leakage current	—	0.1	—	µA	V_{RPH} =5V,V_{RPH} =6V

RUN Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{RUNLK}	Open circuit RUN lead leakage current	—	0.1	—	µA	V_{RUN} = 5V

Protection Circuitry Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{SDTH+}	Rising shutdown lead threshold voltage	4.8	5.25	5.4	V	
V_{SDHYS}	Shutdown lead threshold hysteresis	300	150	100	mV	
V_{SDEOL+}	Rising shutdown lead end-of-life threshold voltage	2.6	3.0	3.4	V	
V_{SDEOL-}	Falling shutdown lead end-of-life threshold voltage	0.7	1.0	1.3		
V_{CSTH+}	Over-current sense threshold voltage	1.05	1.2	1.35		
V_{CSTH-}	Under-current sense threshold voltage	0.14	0.23	0.28		
T_{CS}	Over-current sense propogation delay	50	350	550	nsec	Delay from CS to LO
V_{VDC+}	Low V_{BUS}/rectified line input upper threshold	4.8	5.2	5.7	V	
V_{VDC-}	Low V_{BUS}/rectified line input lower threshold	2.7	3.1	3.5		
T_{SD}	Thermal shutdown junction temperature	—	160	—	°C	Note 4

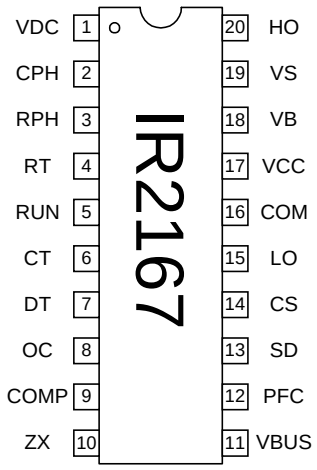
Gate Driver Output Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
VOL	Low level output voltage (PFC, LO or HO)	—	0	100	mV	I_O = 0
V_{OH}	High level output voltage (PFC, LO or HO)	—	0	100		V_{BIAS} - V_O, I_O = 0
t_r	Turn-on rise time (PFC, LO or HO)	50	85	200	nsec	
t_f	Turn-off fall time (PFC, LO or HO)	25	45	100		

Note 4: When the IC senses an overtemperature condition (Tj > 160ºC), the IC is latched off. In order to reset this Fault Latch, the SD lead must be cycled high and then low, or the V_{CC} supply to the IC must be cycled below the falling undervoltage lockout threshold (V_{CCUV-}).

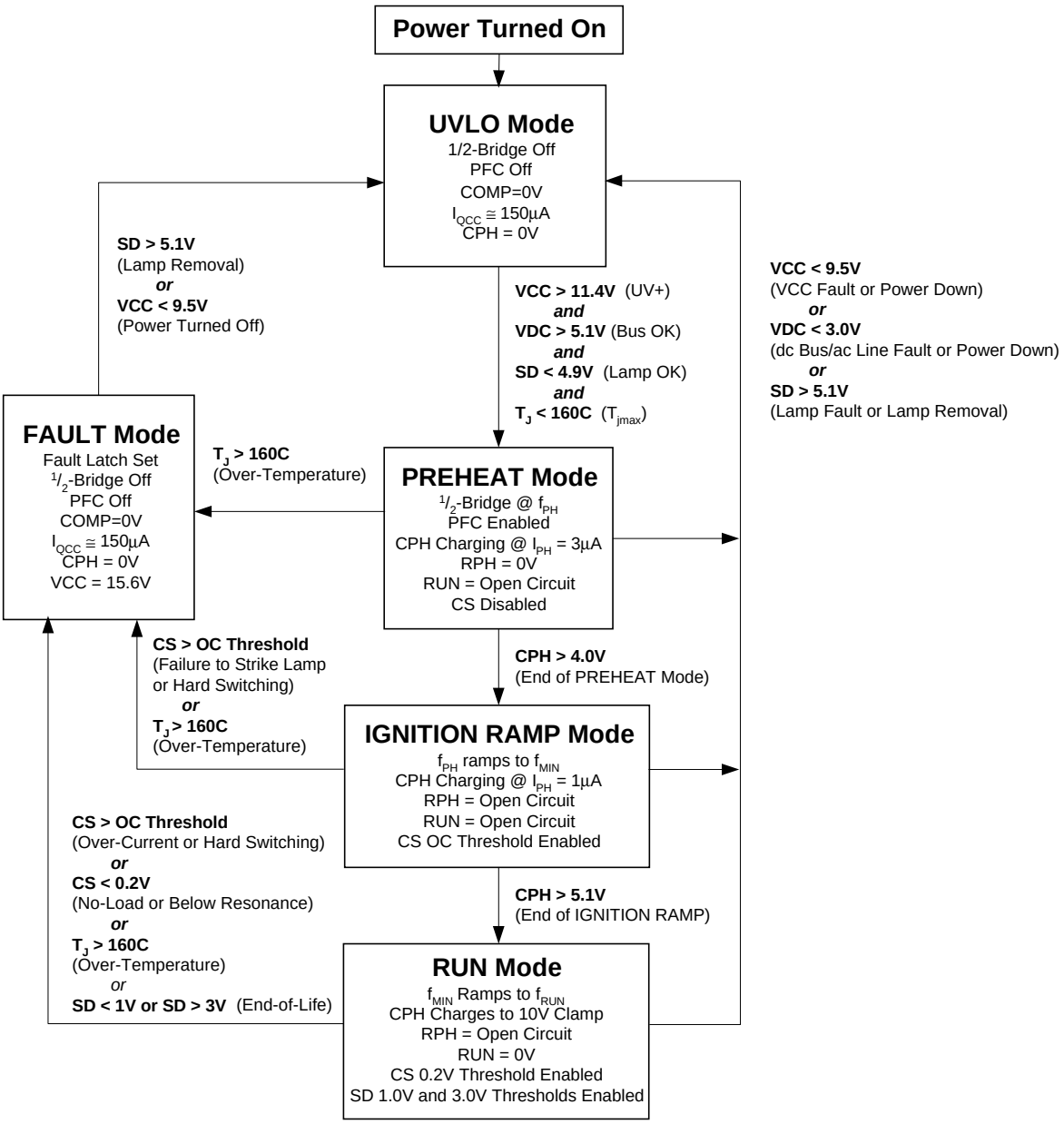
Lead Assignments

Pin Assignments

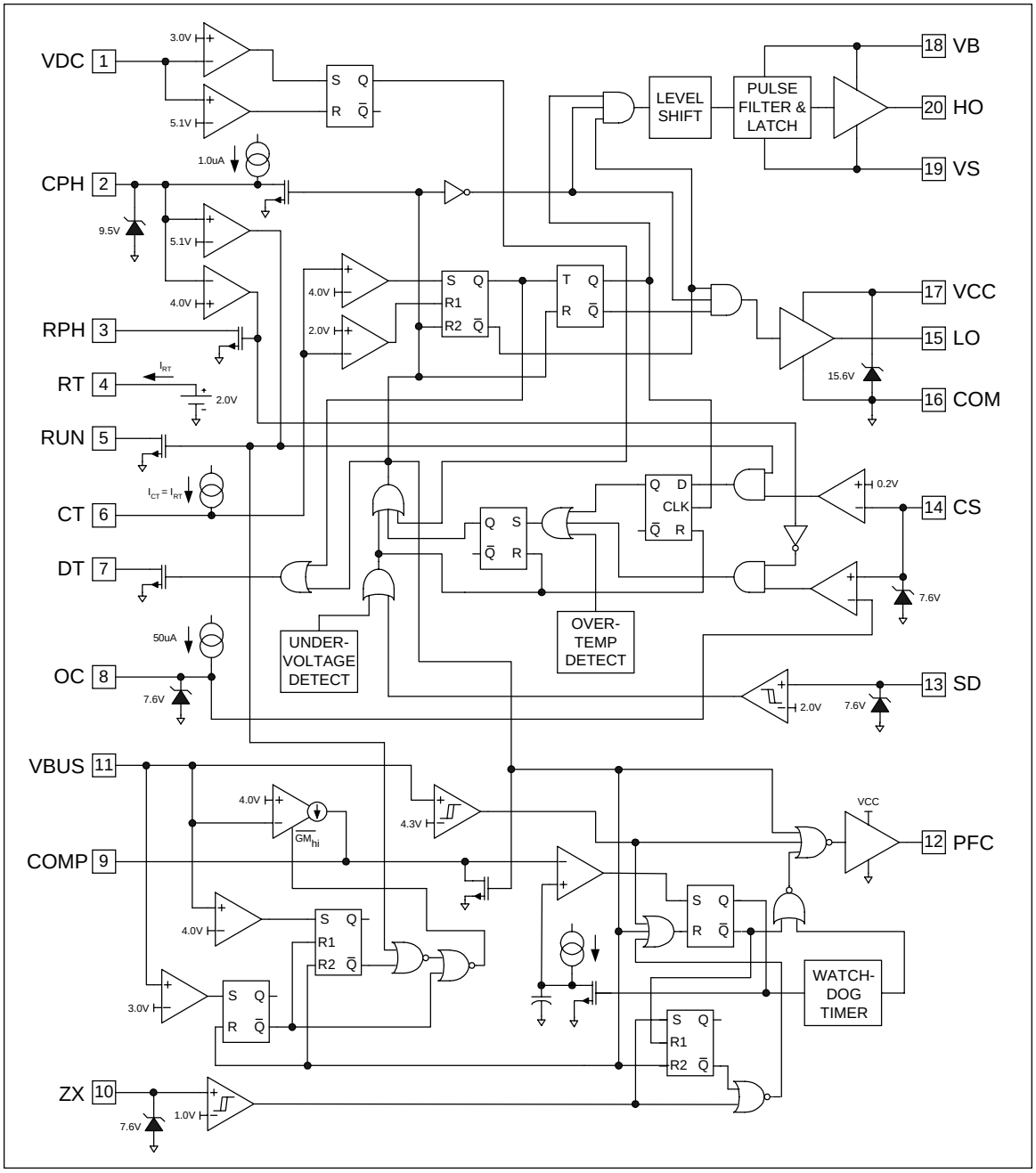


Pin #	Symbol	Description
1	VDC	DC Bus Sensing Input
2	CPH	Preheat Timing Capacitor
3	RPH	Preheat Frequency Resistor & Ignition Capacitor
4	RT	Oscillator Timing Resistor
5	RUN	Run Frequency Resistor
6	CT	Oscillator Timing Capacitor
7	DT	Deadtime Programming
8	OC	Over-current (CS+) Threshold Programming
9	COMP	Error Amplifier Compensation
10	ZX	Zero-Crossing, PFC Inductor
11	VBUS	Bus Voltage Sense Input
12	PFC	PFC Gate Driver Output
13	SD	Shutdown Input
14	CS	Current Sensing Input
15	LO	Low-Side Gate Driver Output
16	COM	IC Power & Signal Ground
17	VCC	Logic & Low-Side Gate Driver Supply
18	VB	High-Side Gate Driver Floating Supply
19	VS	High Voltage Floating Return
20	HO	High-Side Gate Driver Output

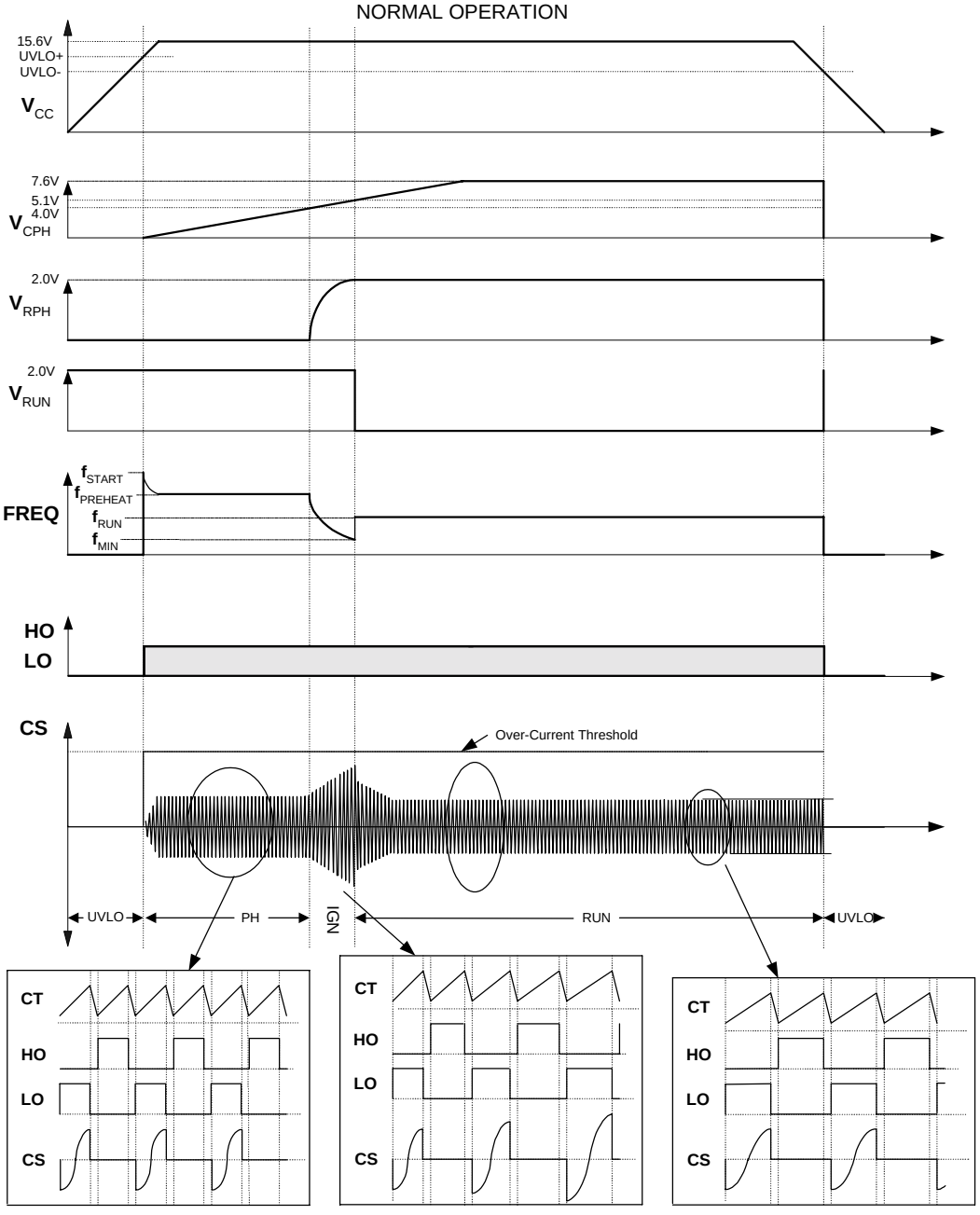
State Diagram



Functional Block Diagram

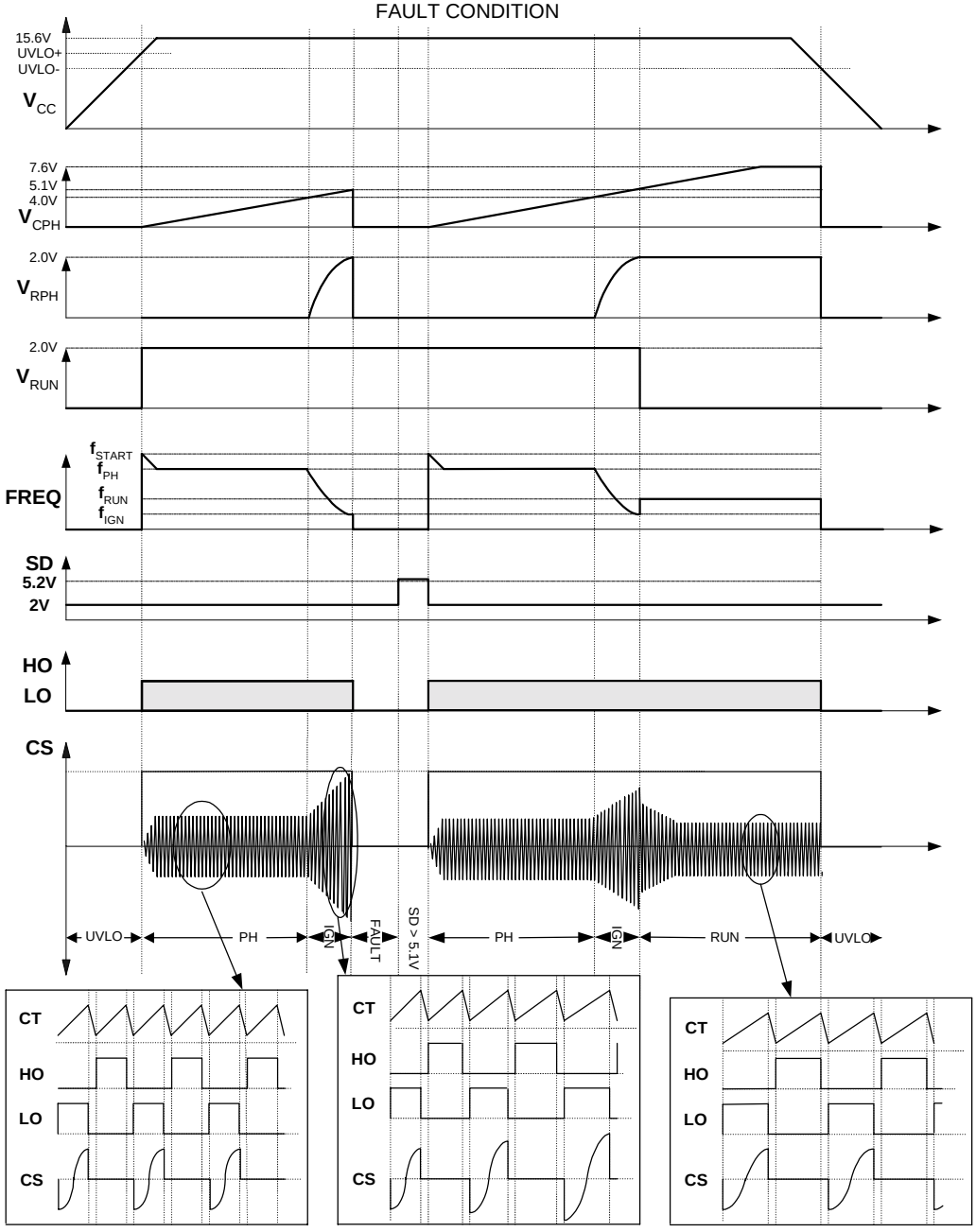


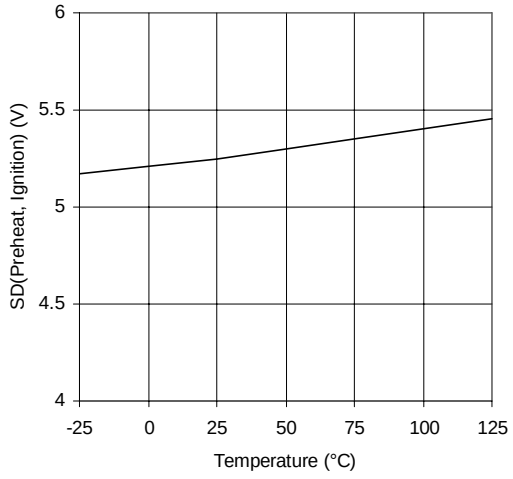
BALLAST CONTROL SECTION
TIMING DIAGRAMS
NORMAL OPERATION



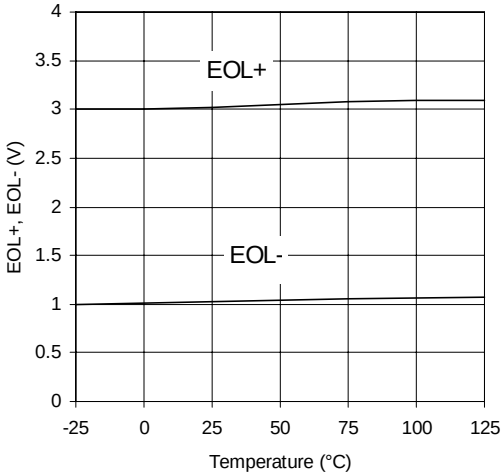
BALLAST CONTROL SECTION
TIMING DIAGRAMS

FAULT CONDITION

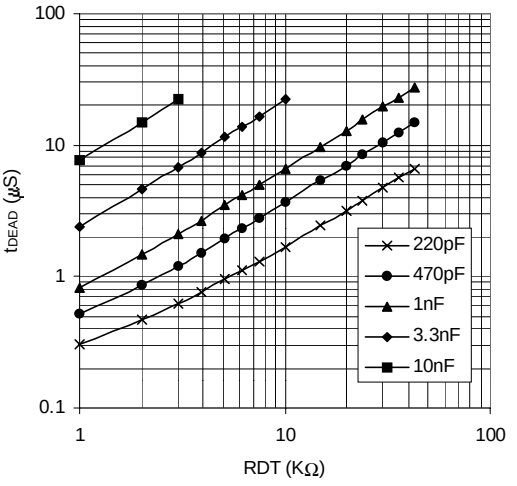




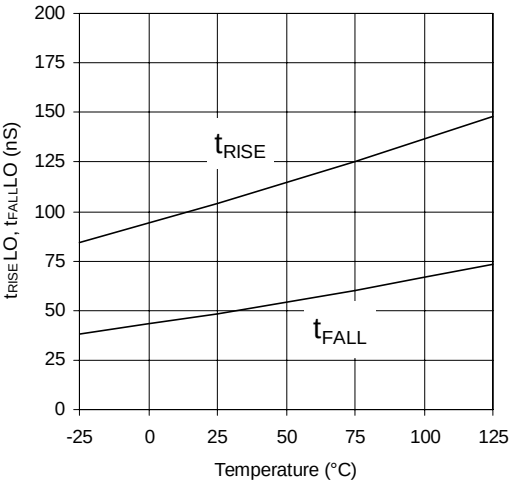
SD+ Threshold vs Temperature (IR2167)
(Preheat, Ignition)



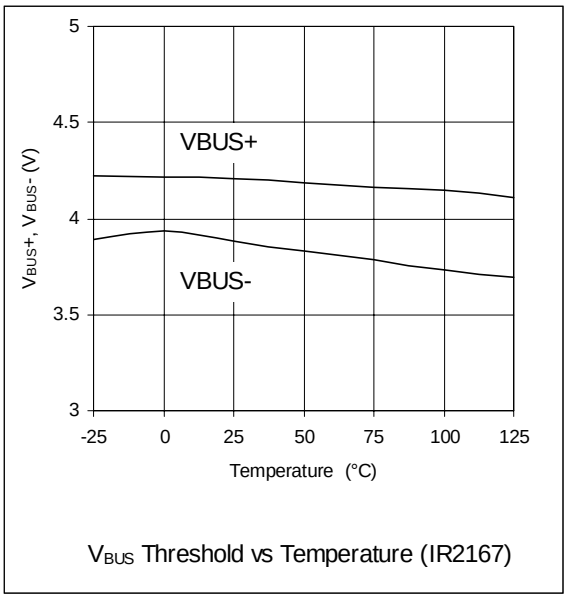
EOL+, EOL- Threshold vs Temperature (IR2167)
(Run Mode)



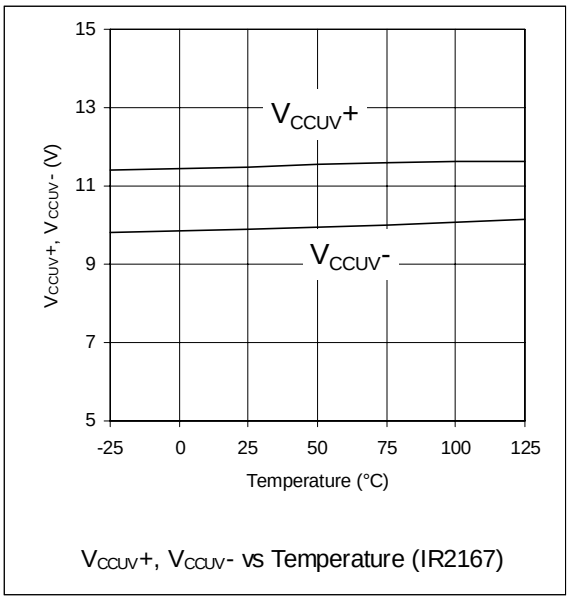
t_{DEAD} vs RDT (IR2167)



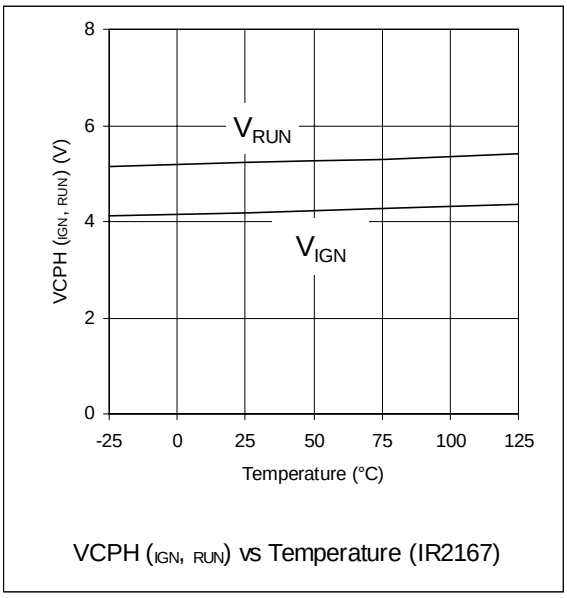
t_{RISE}LO, t_{FALL}LO vs Temperature (IR2167)



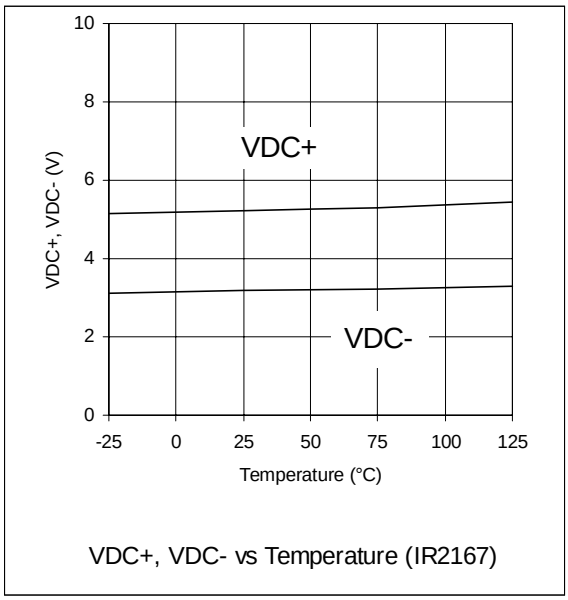
V_{BUS} Threshold vs Temperature (IR2167)



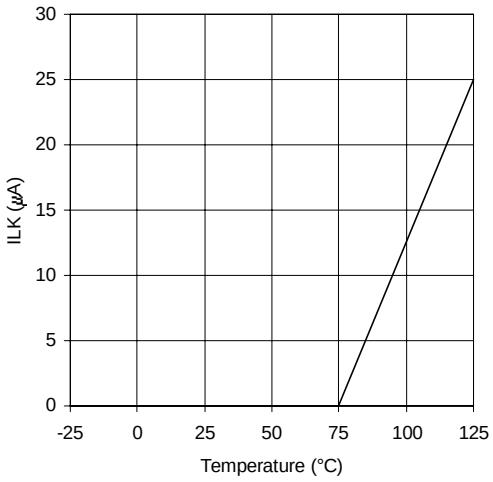
V_{CCUV}+, V_{CCUV}- vs Temperature (IR2167)



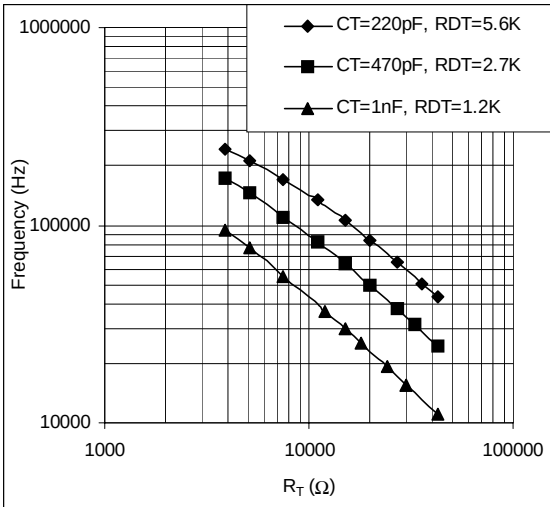
VCPH ($_{IGN, RUN}$) vs Temperature (IR2167)



VDC+, VDC- vs Temperature (IR2167)

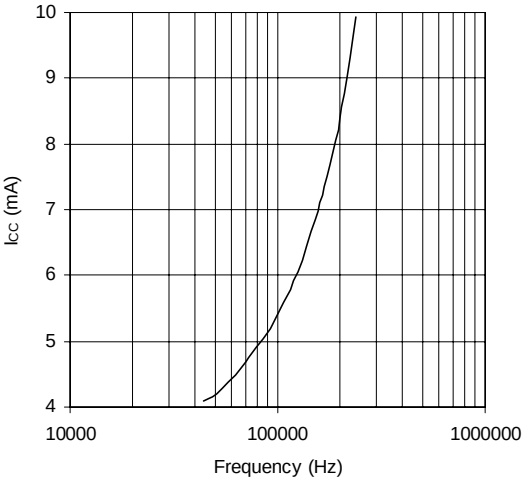


ILK vs Temperature (IR2167)



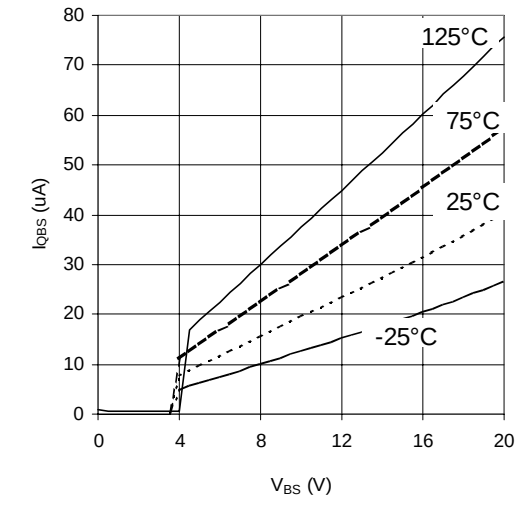
Frequency vs R_T (IR2167)

t_{DEAD}=1µsec

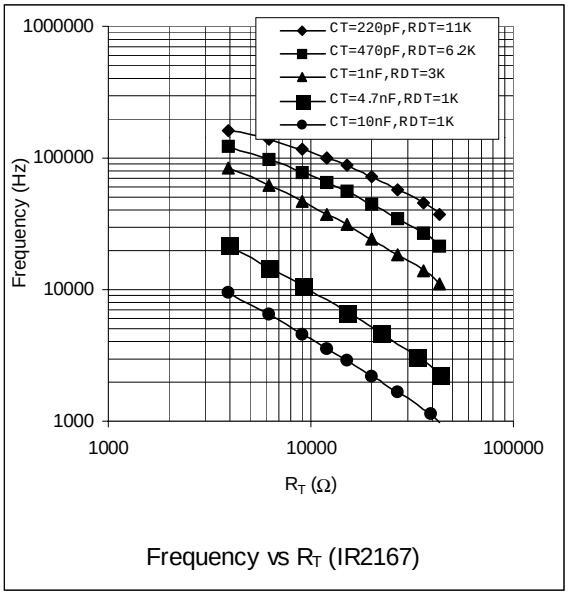


I_{CC} vs Frequency (IR2167)

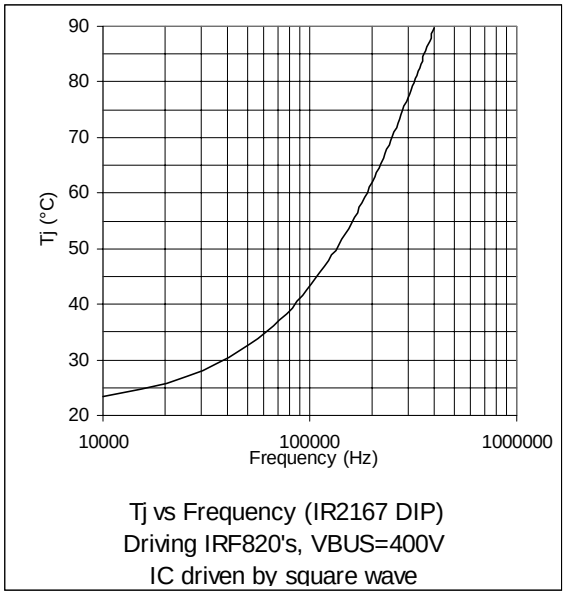
R_{DT}=5.6KΩ, CT=220pF



I_{QBS} vs V_{BS} vs Temperature (IR2167)



Frequency vs R_T (IR2167)



Tj vs Frequency (IR2167 DIP)
Driving IRF820's, VBUS=400V
IC driven by square wave

Functional Description

Under-voltage Lock-Out Mode (UVLO)

The under-voltage lock-out mode is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. (To identify the different modes of the IC, refer to the State Diagram shown on page 2 of this document). During under-voltage lock-out mode, the HO, LO and PFC driver outputs are low and the CT pin is connected to COM through resistor R_{DT} to disable the oscillator. Also, the internal supply to the RT pin circuitry is shut off and pins CPH, RUN, DT and COMP are internally pulled to COM. The IR2167 under-voltage lock-out mode is designed to maintain a very low supply current of less than 200µA, and to guarantee the IC is fully functional before the high side, low side and PFC drivers are activated. Figure 1 shows an efficient supply using the start-up current of the IR2167 together with a charge pump from the ballast stage (R_{SUPPLY}, C_{VCC}, D_{CP1} and D_{CP2}).

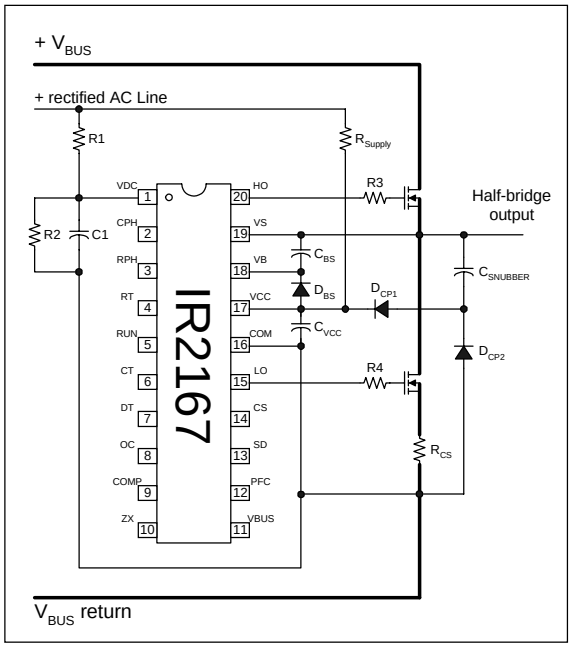


Figure 1: Start-up and supply circuitry

The Vcc capacitor (C_{VCC}) is charged by current through supply resistor (R_{SUPPLY}) minus the start-up current drawn by the IC. The value of (R_{SUPPLY}) is chosen to provide 2X the maximum start-up current to guarantee ballast start-up at low line input voltage. Once the capacitor voltage on the VCC pin reaches the start-up threshold, the SD lead is below 5.1 volts and V_{VDC} is greater than 5.1V, the IC turns on and LO and HO begin to oscillate. PFC does not begin to oscillate until the IC reaches Preheat Mode.

Preheat Mode Startup Mode

The IR2167 enters Preheat mode when VCC exceeds the UVLO positive-going threshold. Before Preheat mode begins, the CPH and RPH pins are connected to COM. (See Figure 3). As Preheat begins, the external capacitor C_{PH} is charged up by an internal 3µA current source. C_{PH} determines the preheat time which continues until the voltage on the CPH pin charges to 4.0V. Preheat mode is defined as the state the IC is in when the lamp filaments are being heated to their correct emission temperature. This is necessary for maximizing lamp life and reducing the required ignition voltage. At the onset of Preheat Mode, C_{VCC} begins to discharge due to the increase in IC operating current (Figure 2) above the available current through resistor R_{SUPPLY}. However, the half-bridge output also begins to oscillate and the charge pump, consisting of **$C_{SNUBBER}$, D_{CP1} and D_{CP2},** supply the current to charge capacitor C_{VCC} and thus the voltage to the IC. The VCC voltage supplied to the IC is

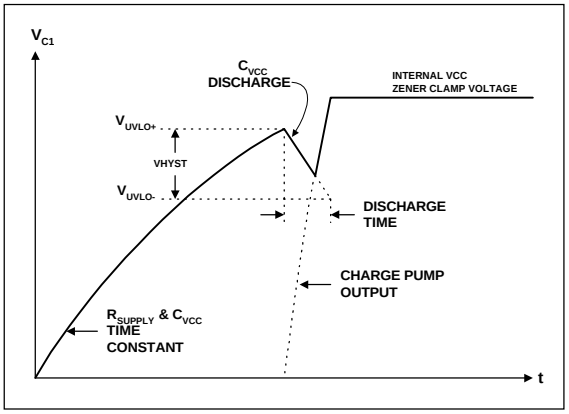


Figure 2: Supply Capacitor (CVCC) voltage

limited by the internal 15.6V zener clamp. C_{VCC} and **$C_{SNUBBER}$** must be selected such that enough supply current

is available over all ballast operating conditions. Bootstrap diode (D_{BS}) and supply capacitor (C_{BS}) comprise the supply voltage for the high-side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on HO, the first pulse from the output drivers comes from the LO pin.

The Preheat mode oscillation frequency of the half-bridge output is determined by the parallel combination of R_{PH} and R_T with the values of C_T, R_{DT} and an internal circuit as shown in Figure 3. Note that at the onset of Preheat mode the initial startup frequency is much higher than the preheat frequency. The half-bridge output frequency then ramps down from this initial start-up frequency to the Preheat mode frequency. This is to ensure that the instantaneous voltage across the lamp during the first few cycles of operation does not exceed the strike potential of the lamp

Ignition Mode

When the CPH pin charges up to 4.0V, ignition mode begins. At this time, the output of COMP2 (figure 3) goes low, M1 turns off and CRAMP begins to charge. CRAMP determines the time it takes for the oscillator to ramp down from the Preheat frequency to the Ignition Mode frequency. Once the voltage on the RPH lead reaches 2.0V, external resistor RPH has no effect on the frequency that is now determined by external components RT, CT and RDT. This is the minimum frequency. By this time, the oscillator will have ramped down toward the resonance of the load circuit causing the lamp to ignite.

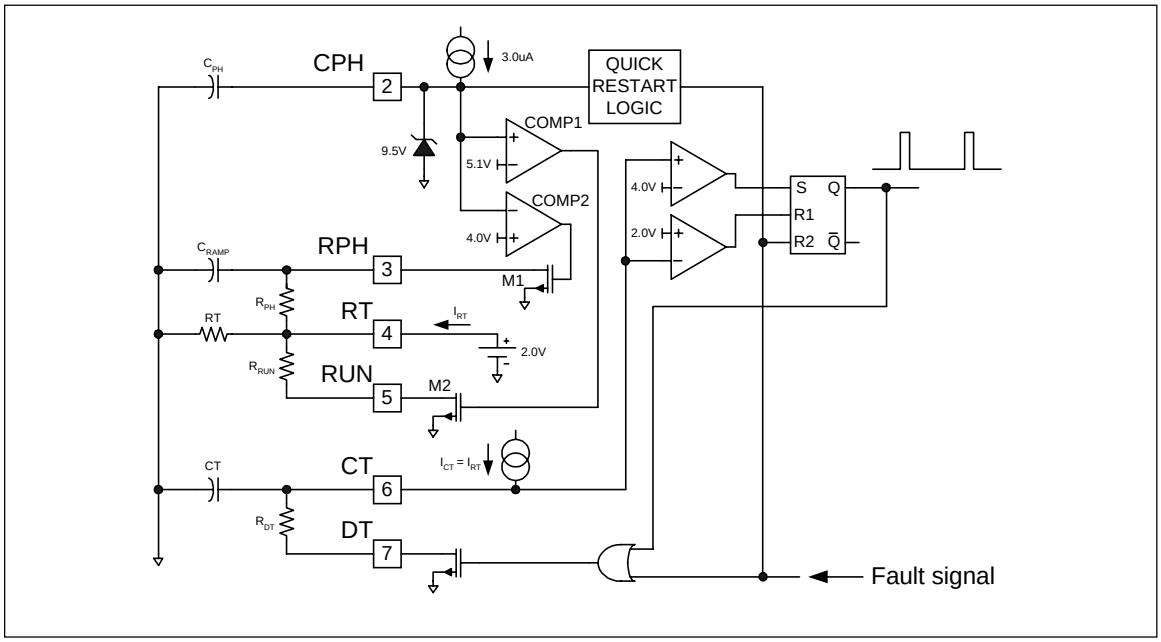


Figure 3: Oscillator section block diagram with external component connection

Run Mode

When the voltage on the CPH pin reaches 5.1V, the IC enters Run mode. At this time, the output of COMP1 (figure 3) goes high which turns M2 on and pulls the RUN pin to COM. The frequency is now controlled by external components R_T, R_{RUN}, C_T and R_{DT}. In certain cases it is necessary to have the run frequency higher than the ignition frequency to control the power used by the load. Figure 4 shows the ballast control sequence explained in the previous paragraphs

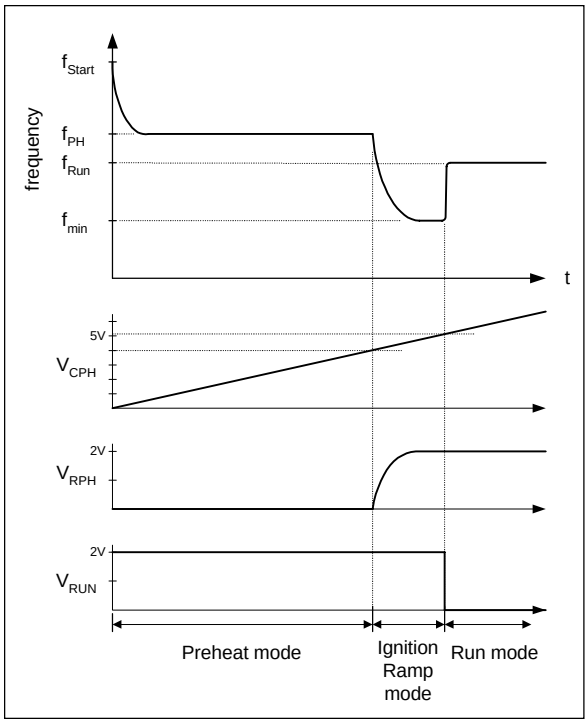


Figure 4: IR2167 Ballast Control Sequence

The control sequence used in the IR2167 allows the Run mode operating frequency of the ballast to be higher than the ignition frequency (i.e., fstart > fph > frun > fign). This control sequence is recommended for lamp types where the ignition frequency is too close to the run frequency to ensure proper lamp striking for all production resonant LC component tolerances (please note that it is possible to use the IR2167 in systems where fstart > fph > fign > frun, simply by leaving the RUN pin open).

The heart of this controller is an oscillator that resembles those found in many popular PWM voltage regulator ICs. In its simplest form, this oscillator consists of a timing resistor and capacitor connected to ground. The voltage across the timing capacitor C_T is a sawtooth, where the rising portion of the ramp is determined by the current in the RT lead, and the falling portion of the ramp is determined by an external deadtime resistor R_{DT}. The oscillograph in Figure 5 illustrates the relationship between the oscillator capacitor waveform and the gate driver outputs.

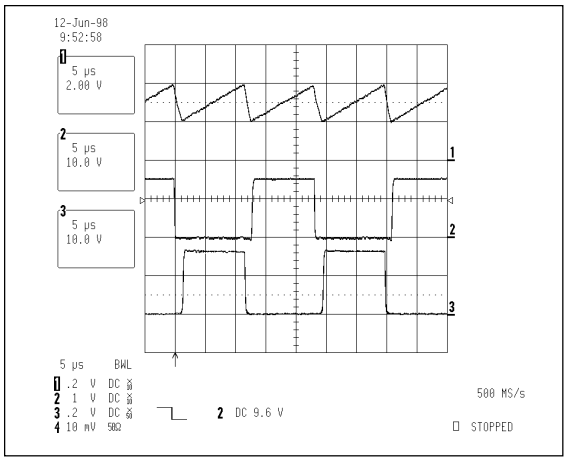


Figure 5: Oscillator Waveforms

This falling portion of the sawtooth waveform is referred to as deadtime, during which both HO and LO outputs are low. The deadtime can be programmed by means of the external R_{DT} resistor.

The RT input is a voltage-controlled current source, where the voltage is regulated to be approximately 2.0V. In order to maintain proper linearity between the RT pin current and the CT capacitor charging current, the value of the RT pin current should be kept between 50µA and 500µA. The RT pin can also be used as a feedback point for closed loop control.

PFC Section

In most AC to DC power converters it is necessary to have the circuit act as a pure resistive load to the AC input line voltage. To achieve this, active power factor correction (PFC) can be implimented which, for an AC input line voltage, produces an AC input line current. It is also important to produce a sinusoidal input current which has a low total harmonic distortion (THD) and a high power factor (PF) (See Figure 6).

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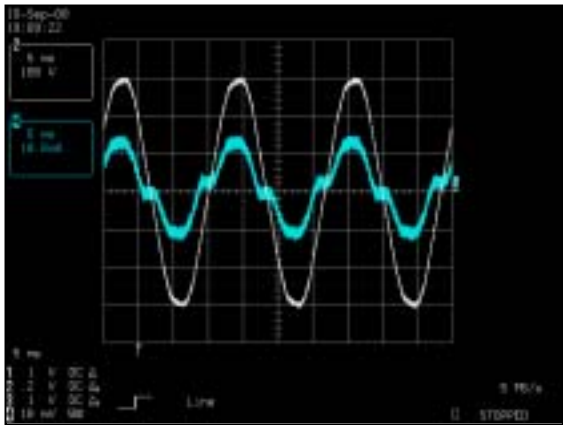


Figure 6: Input Voltage & Current
PF=0.96, THD=22%

The approach used in the IR2167 is classified as running in critical conduction mode, in which the inductor current discharges to zero with each switching cycle. There is no need to sense the rectified AC line input voltage because it is already sinusoidal. Therefore, the inductor current will naturally follow the sinusoidal voltage envelope as the PFC MOSFET is turned on and off at a much higher frequency (>10KHz) than the line input frequency (50 to 60Hz). The circuit compares the DC Bus voltage to a fixed reference voltage to determine the on-time of the PFC MOSFET. The off-time is determined by the time it takes the L_{PFC} current to drop to zero. This zero current level is detected by a secondary winding in L_{PFC} that is connected to the ZX pin. The result is a system where the switching frequency is free-running and constantly changing from a high frequency near the zero crossing of the AC input line voltage, to a lower frequency at the peaks. (See Figures 7, 8 & 9).

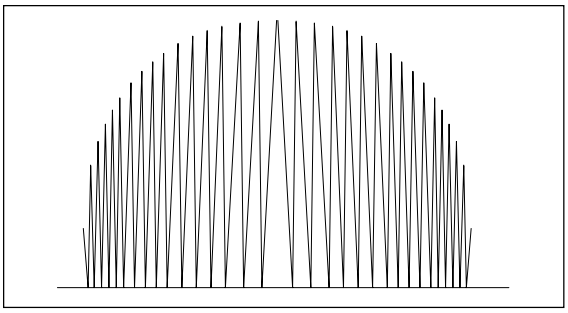


Figure 7: Inductor Current

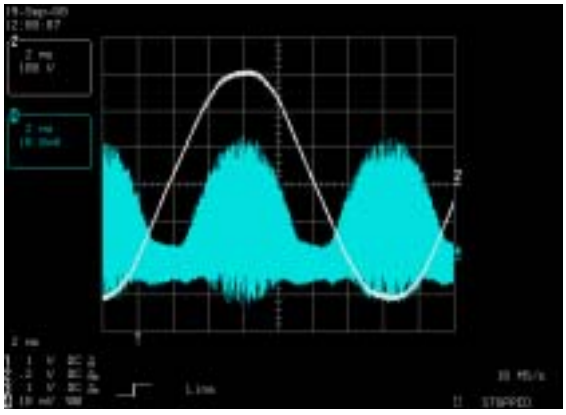


Figure 8: Boost Inductor Envelope & Line Voltage

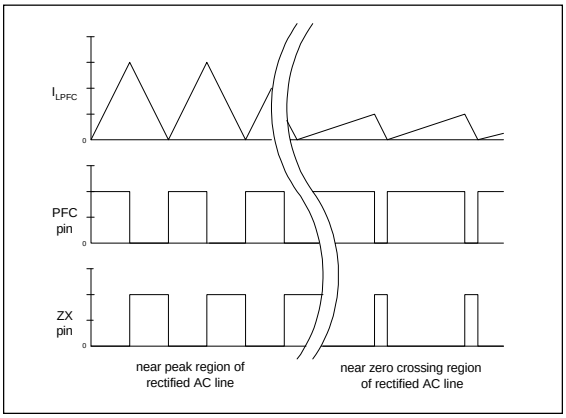


Figure 9: Boost FET On Time vs Line Input

As the external capacitor on the COMP pin begins to charge, the PFC MOSFET on time duration increases. The gain of OTA1 is at its maximum value (See Figures 10 & 11). Maximum gain is desireable to raise the Bus voltage to its nominal value as quickly as possible. When the voltage at the VBUS pin reaches 3V, the gain of OTA1 decreases to its nominal value. The BUS voltage continues to increase to its nominal value at which time the voltage measured at the VBUS pin equals 4V. The gain of OTA1 now increases to its maximum value and remains there until the Run mode. This is necessary because if VBUS overshoots its nominal value, the circuit can react quickly to correct the error. Also, during ignition, there is a sudden increase in load current which can cause the Bus voltage to sag. With maximum gain, OTA1 can quickly restore the DC Bus voltage to its nominal value.

When the AC line voltage is applied to the ballast, V_{CC} rises to 15V. The PFC section is not enabled until the beginning of the Preheat mode of operation. By not enabling the PFC section until the beginning of the Preheat mode, the DC Bus voltage in the ballast is not yet boosted to its nominal running value. This helps alleviate the initial flash of the lamp when the half-bridge driver section first begins to switch.

When the PFC circuit is first enabled, (See Figure 10), the voltage at the VBUS and COMP pins is low. The PFC MOSFET is turned on with minimum on time and L_{PFC} is shorted to ground and begins charging. The PFC MOSFET then turns off and L_{PFC} begins to discharge into the DC BUS capacitor.

COMP4 has a 4.3V threshold with hysteresis so that if the voltage at the VBUS pin overshoots the 4.0V threshold, the PFC MOSFET will not turn on again until the voltage at the VBUS pin drops to approximately 4.0V. This effectively limits ths maximum bus voltage to approximately 8% greater than the regulated level.

In some instances, the line voltage may be too high. This causes the AC rectified line current to directly charge the DC Bus capacitor without being boosted. Since the current never drops to zero, the ZX pin never goes high and the PFC MOSFET never turns on. The Watch Dog Timer circuit provides a pulse to turn on the PFC MOSFET if no pulse is detected at the ZX pin for 500mS. This enables the PFC circuitry to regulate the DC Bus voltage at its nominal value

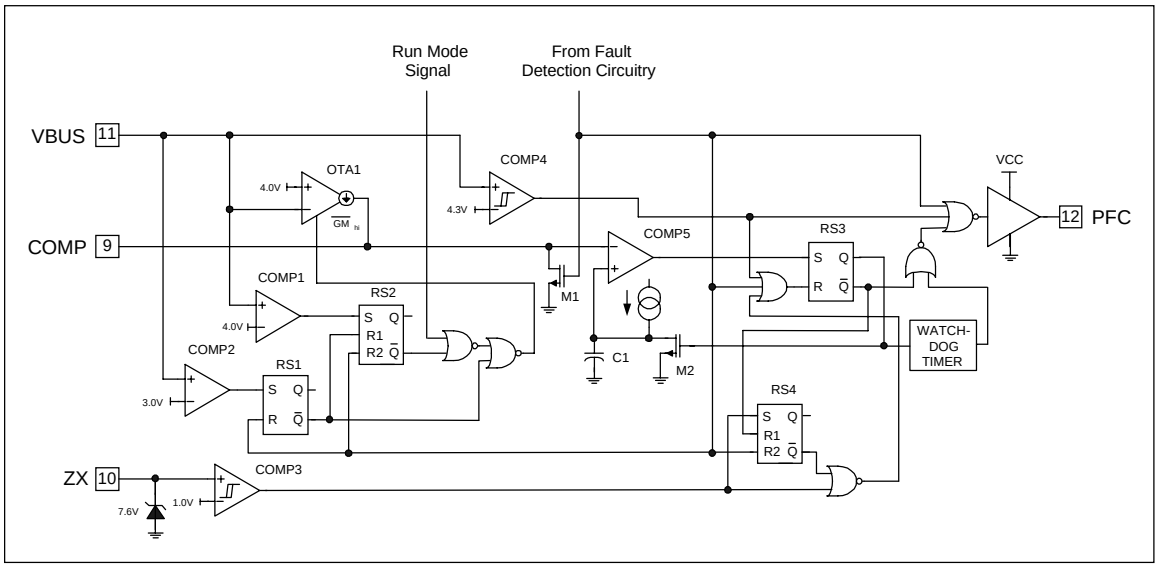
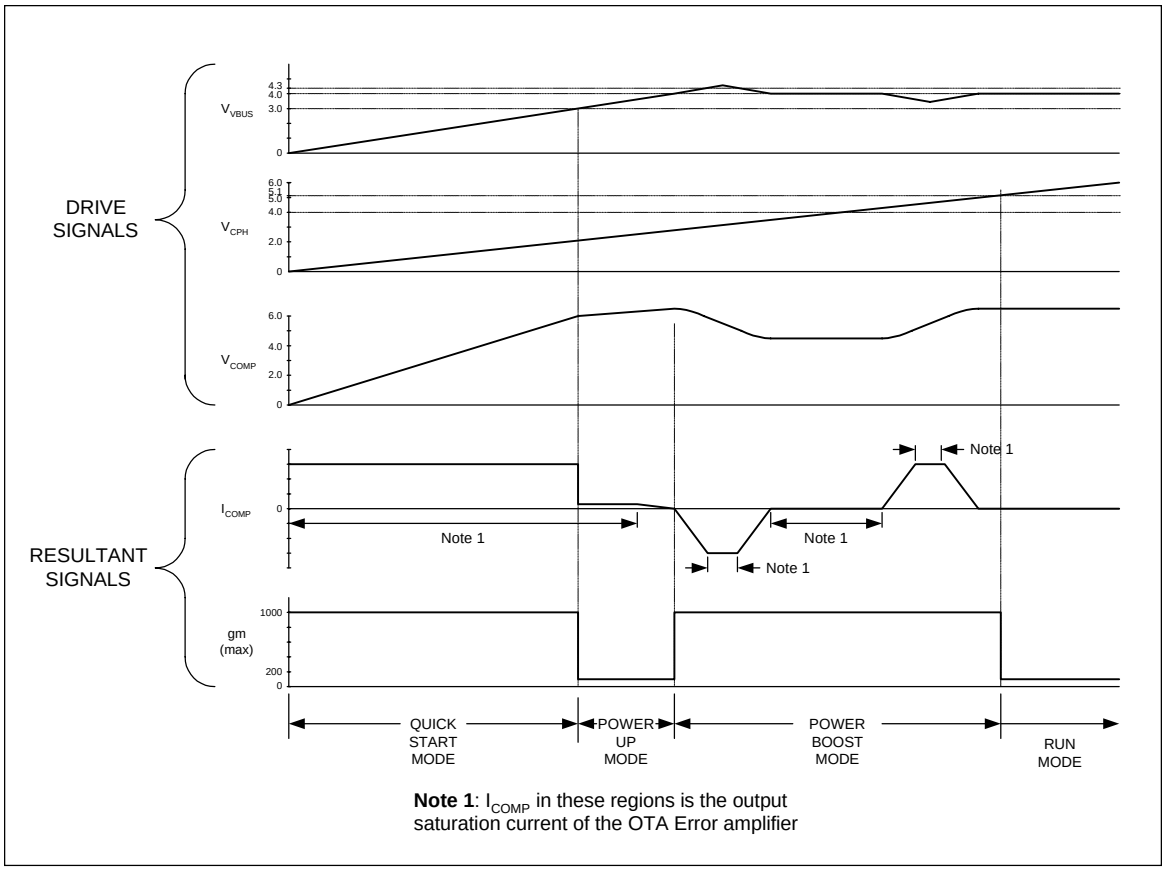


Figure 10: PFC Section



Note 1: I_{COMP} in these regions is the output saturation current of the OTA Error amplifier

Figure 11: PFC Timing Sequence

Lamp Protection & Automatic Restart Circuitry Operation

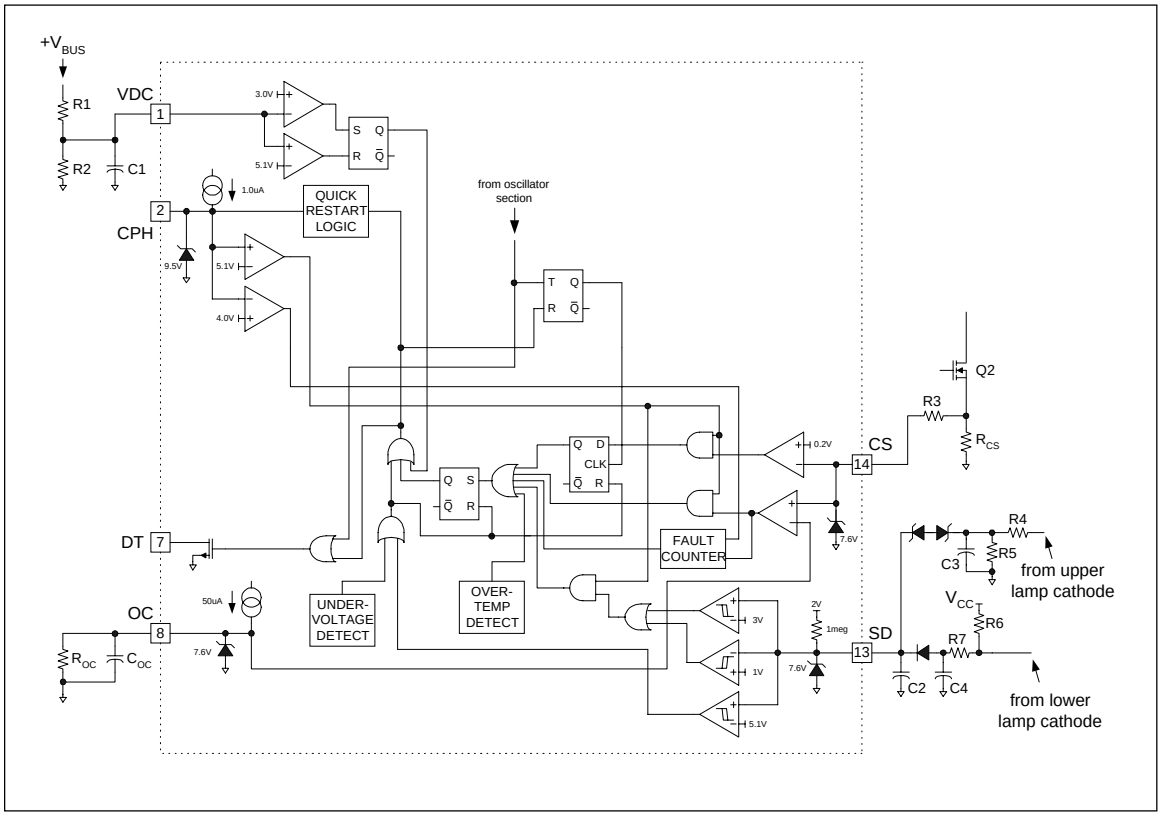


Figure 12: Lamp Protection & Automatic Restart circuitry block diagram with external component connection

Sensing the AC Line Voltage

The first of these protection pins senses the voltage on the AC line by means of an external resistor divider (R1, R2 and capacitor C1) and an internal comparator with hysterisis. When power is first supplied to the IC at system startup, three conditions are required before oscillation is initiated: 1.) the voltage on the VCC pin must exceed the rising undervoltage lockout threshold (11.5V), 2.) the voltage at the VDC pin must exceed 5.1V, and 3.) the voltage on the SD pin must be below approximately 4.85V. If a low ac line condition occurs during normal operation, or if power to the ballast is shut off, the ac line will collapse prior to the VCC of the chip (assuming theVCC is derived from a charge pump off of the output of the half-bridge). In this case, the voltage on the VDC pin will shut the oscillator off, thereby protecting the power transistors from potentially hazardous hard switching. Approximately 2V of hysterisis has been designed into the internal comparator sensing the VDC pin, in order to account for variations in the ac line voltage under varying load conditions. When the ac line recovers, the chip re-starts from the beginning of the control sequence, as shown in timing diagram (See Figure 13).

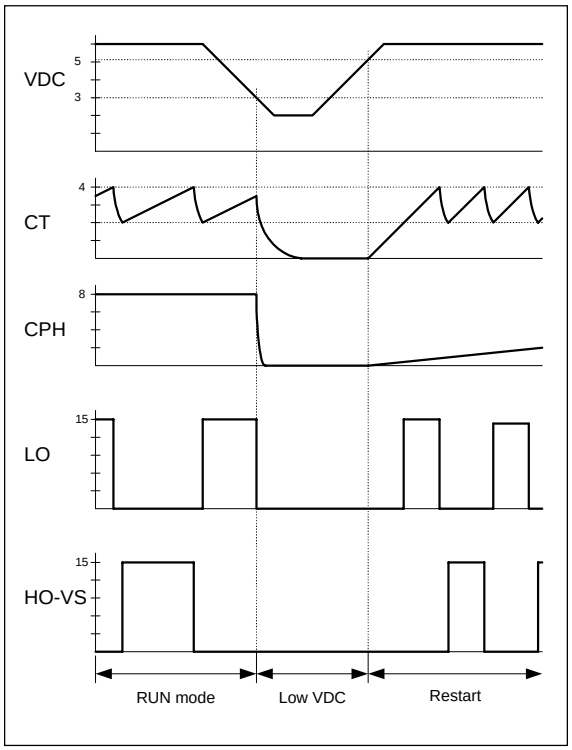


Figure 13: VDC lead fault and auto restart

automatically restarts the lamp in the proper manner.

In the Run mode there are two additional thresholds enabled on the SD pin: 1V and 3V. These thresholds form a window and during normal lamp running the voltage appearing at the SD pin is maintained within these two levels. As a lamp nears its end-of-life, its running voltage will increase and the signal applied to the SD pin detects this by exceeding the window threshold width. The oscillator is disabled, both gate driver outputs are pulled low, and the chip is put into the micropower mode.

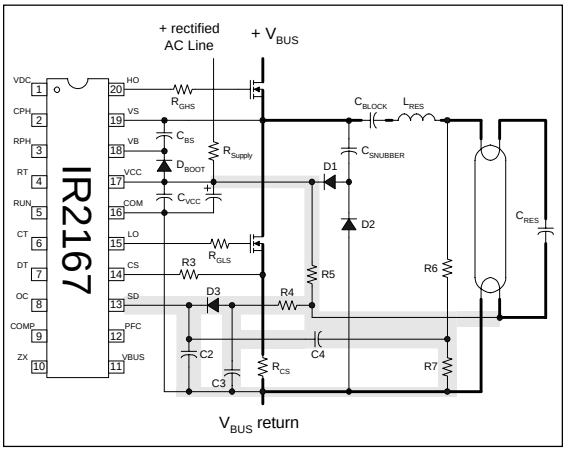


Figure 14: Lamp presence detection circuit connection (shaded area)

Lamp Presence and End-of-Life Detection

The second protection pin, SD, is used for both shutdown and end-of-life detection. The SD pin would normally be connected to an external circuit that senses the presence of the lamp(s) and the voltage appearing across the lamp(s). An example circuit for a single lamp is shown in Figure 14. During all modes of operation if the SD pin exceeds 5.1V (approximately 150mV of hysterisis is included to increase noise immunity), signaling either a lamp fault or lamp removal, the oscillator is disabled, both gate driver outputs are pulled low, and the chip is put into the micropower mode. Since a lamp fault would normally lead to a lamp exchange, when a new lamp is inserted in the fixture, the SD pin would be pulled back to near ground potential. Under these conditions a reset signal would restart the chip from the beginning of the control sequence, as shown in the timing diagram in Figure 15. Thus, for a lamp removal and replacement, the ballast

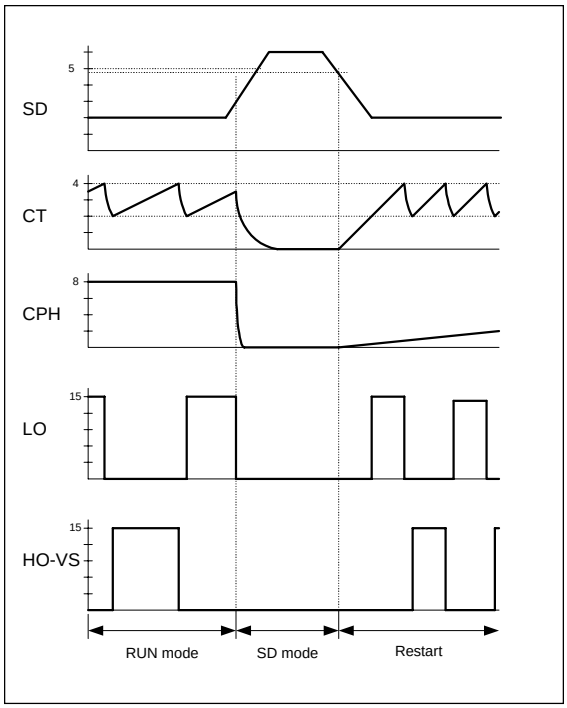


Figure 15: SD lead fault and auto restart

Half-Bridge Current Sensing and Protection

The third pin used for protection is the CS pin, which is normally connected to a resistor in the source of the lower power MOSFET, as shown in Figure 16. The CS pin is used to sense fault conditions such as failure of a lamp to strike, over-current during normal operation, hard switching, no load, and operation below resonance. If any one of these conditions is sensed, the fault latch is set, the oscillator is disabled, the gate driver outputs go low, and the chip is put into the micropower mode. The CS lead performs its sensing functions on a cycle-by-cycle basis in order to maximize ballast reliability.

For the over-current, failure-to-strike, and hard switching fault conditions, an externally programmable, positive-going CS+ threshold is enabled at the end of the preheat time. The level of this positive-going threshold is determined by the value of the resistor R_{OC}. The value of the resistor R_{OC} is determined by the following formula:

$$R_{OC} = \frac{V_{CS+}}{55E-6}, \quad \text{or}$$

$$V_{CS+} = 55E-6 \cdot R_{OC}$$

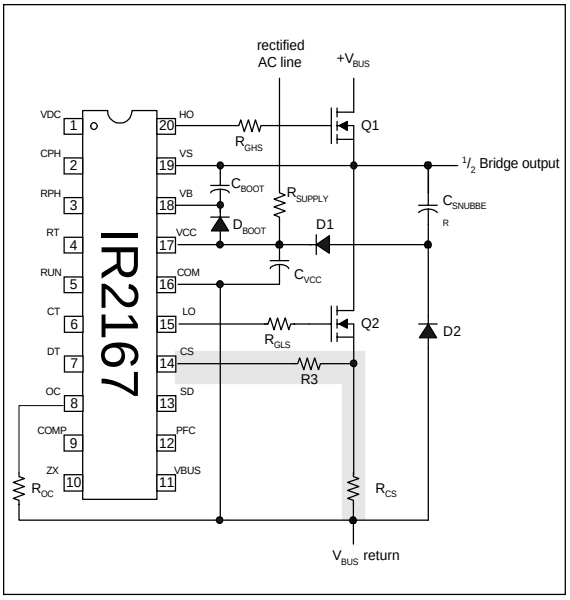


Figure 16: Half-bridge current sensing circuit connection (shaded area)

For the under-current and under-resonance conditions, there is a negative-going CS- threshold of 0.2V which is enabled at the onset of the run mode. The sensing of this CS- threshold is synchronized with the falling edge of the LO output.

Figures 17, 18 and 19 are oscillographs of fault conditions. Figure 17 shows a failure of the lamp to strike, Figure 18 shows a hard switching condition and Figure 19 shows an under-current condition.

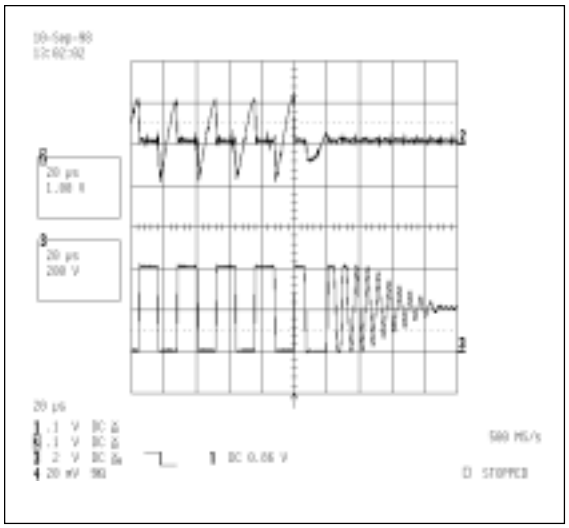


Figure 17: Failure of lamp to strike

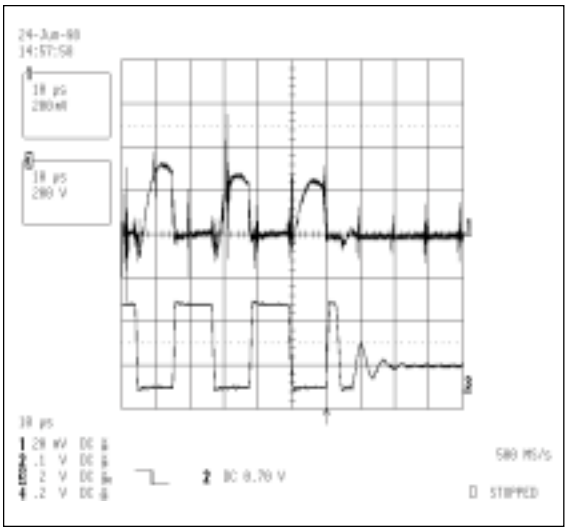


Figure 19: Operation below resonance

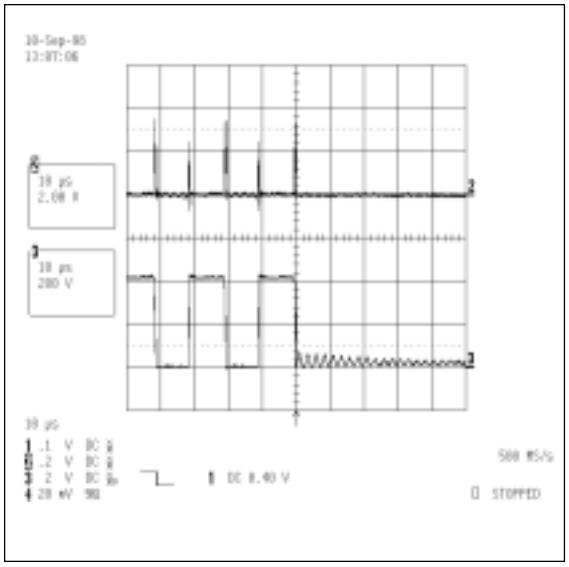


Figure 18: Hard switching condition

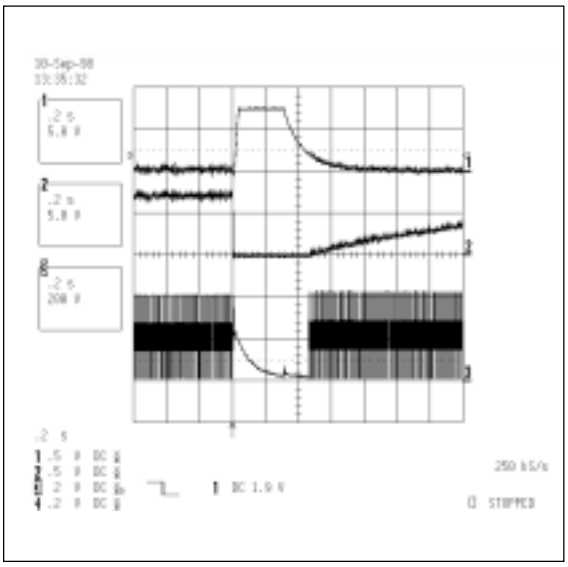


Figure 20: Auto restart for lamp replacement

Recovery from such a fault condition is accomplished by cycling either the SD pin or the VCC pin. (See Figure 20). When a lamp is removed, the SD pin goes high, the fault latch is reset, and the chip is held off in an unlatched state. Lamp replacement causes the SD pin to go low again, reinitiating the startup sequence. The fault latch can also be reset by the undervoltage lockout signal, if VCC falls below the lower undervoltage threshold.

Bootstrap Supply Considerations

Power is normally supplied to the high-side circuitry by means of a simple charge pump from VCC, as shown in Figure 21.

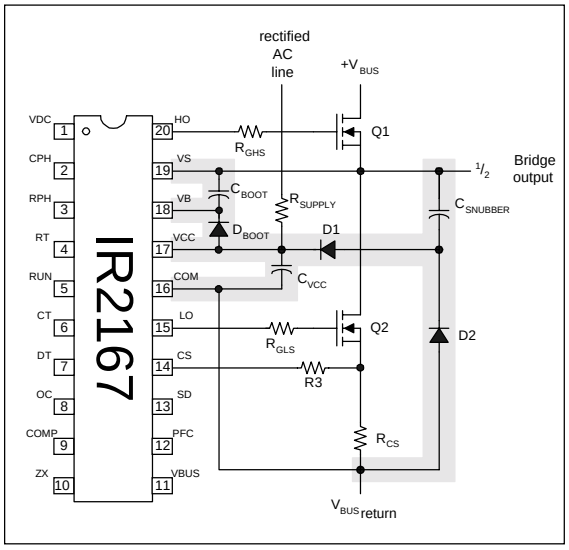


Figure 21 : Typical bootstrap supply connection with VCC charge pump from half-bridge output (shaded area)

A high voltage, fast recovery diode D_{BOOT} (the so-called bootstrap diode) is connected between VCC (anode) and VB (cathode), and a capacitor C_{BOOT} (the so-called bootstrap capacitor) is connected between the VB and VS leads. During half-bridge switching, when MOSFET Q2 is on and Q1 is off, the bootstrap capacitor C_{BOOT} is charged from the VCC decoupling capacitor, through the bootstrap diode D_{BOOT}, and through Q2. Alternately, when Q2 is off and Q1 is on, the bootstrap diode is reverse-biased, and the bootstrap capacitor (which 'floats' on the source of the upper power MOSFET) serves as the power supply to the upper gate driver CMOS circuitry. Since the quiescent current in this CMOS circuitry is very low (typically 45µA in the on-state), the majority of the drop in the VBS voltage when Q1 is on occurs due to the transfer of charge from the bootstrap capacitor to the gate of the power MOSFET.

Design Equations

Note: The results from the following design equations can differ slightly from experimental measurements due to IC tolerances, component tolerances, and oscillator over- and under-shoot due to internal comparator response time.

Step 1: Program Maximum Ignition Voltage

Maximum lamp voltage is required during ignition. This will vary depending on the type of lamp, but 1600V is typical for a T8 lamp. As the frequency decreases from the preheat frequency to the resonant frequency, the voltage across the lamp increases. During ignition, only R_T along with C_T and D_T determine the frequency. R_{PH} and R_{RUN} are not connected to COM at this time. The value of R_T should be chosen so that the desired ignition voltage is reached. The RT pin current and timing capacitor charging current are both approximately:

$$I_{CT} = I_{RT} = \frac{2.0V}{R_T}$$

The value of this current should be kept between 50 µA and 500 µA. The value for C_T is computed as follows:

$$C_T = \frac{1}{R_T}\left(\frac{1}{2\,f_{ign}} - td\right)$$

And the ignition mode frequency is:

$$f_{IGN} = \frac{1}{2\left(R_T C_T + td\right)}$$

$$R_T = \frac{1}{C_T}\left(\frac{1}{2\,f_{ign}} - td\right)$$

Deadtime is equal to:

$$td = 0.69 \cdot R_{DT} \cdot C_T$$

The following graphs, figures 22 and 23, illustrate the relationship between the effective resistance (i.e. the parallel combination of resistors which programs the CT capacitor charging current) and the operating frequency.

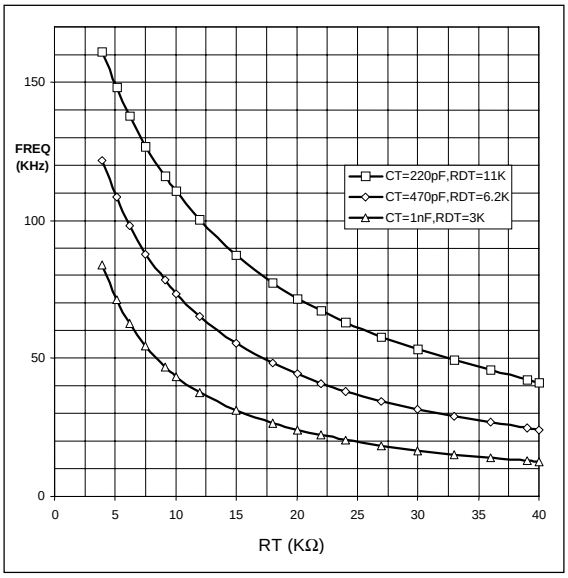


Figure 22: f_{OSC} vs effective R_T (t_{DEAD}=2.0µsec)

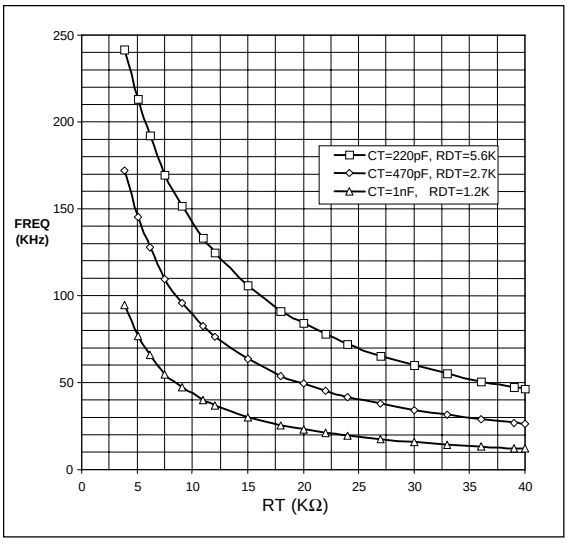


Figure 23: f_{OSC} vs effective R_T (t_{DEAD}=1.0µsec)

Figure 24 illustrates the relationship between deadtime vs R_{DT}.

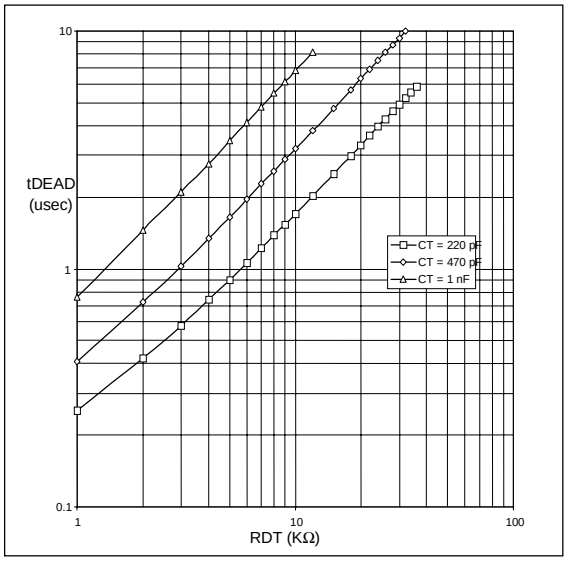


Figure 24: Deadtime vs RDT

Step 2: Program Maximum Ignition Current

The ignition current should be limited to the rating of the lamp resonant inductor and the half-bridge MOSFETS. The saturation current of the lamp resonant inductor should be much lower than the current rating of the MOSFETS. Under worst case conditions, the lamp resonant inductor should not be allowed to saturate. This current is controlled by the CS pin and the OC pin. The OC lead has an internal 50µA current source. This current through external resistor R_{OC} determines the threshold on the CS pin.

$$R_{OC} = \frac{V_{CS} +}{55E-6} or$$

$$V_{CS} + = 55E-6-R_{OC}$$

If the current through external resistor R_{CS} exceeds a predetermined value, the IC shuts off.

Step 3: Program Preheat Frequency

The preheat frequency is determined by the parallel combination of R_{PH} and R_T along with C_T and R_{DT}. The frequency should be chosen so that the voltage across the lamp is much lower than the ignition voltage but still provides adequate heating of the filaments. During preheat, the current through the filaments is constant. However, as the filaments heat up, their resistance increases. This results in an increase in the voltage measured across the filaments, which indicates the hot to cold ratio.

$$f_{PH} = \frac{1}{2 \cdot \left(\frac{R_T \cdot R_{PH}}{R_T + R_{PH}} \cdot C_T + td \right)}$$

$$R_{PH} = \frac{\frac{1}{C_T}\left(\frac{1}{2 f_{ph}} - td \right)}{1 - \frac{1}{R_T \cdot C_T}\left(\frac{1}{2 f_{ph}} - td \right)}$$

4:1 is an acceptable ratio for proper heating

Step 4: Program preheat time

The preheat time is determined by external capacitor C_{PH}. The preheat time required for a 4:1 hot to cold ratio can be observed by measuring the voltage across the filaments. The preheat time is calculated as follows:

$$t_{PH} = 4.0E6 \cdot C_{PH}$$

The IR2167 is held in preheat until C_{PH} is charged to 4.0V.

Step 5: Program the ignition mode time

The difference in time between the preheat mode and the run mode is the ignition mode. The rate at which the frequency changes from preheat to run is determined by external resistor R_{RAMP}.

Step 6. Program the run frequency

The run mode begins when external resistor R_{PH} is charged to 5.1V. At this time, the run frequency is determined by the parallel combination of RT and R_{RUN} along with R_{DT} and C_T. The run frequency can be programmed above or below the ignition frequency. f_{RUN} is determined by the following equation:

$$f_{RUN} = \frac{1}{2 \cdot \left(\frac{R_T \cdot R_{RUN}}{R_T + R_{RUN}} \cdot C_T + td \right)}$$

$$R_{RUN} = \frac{\frac{1}{C_T}\left(\frac{1}{2 f_{RUN}} - td \right)}{1 - \frac{1}{R_T \cdot C_T}\left(\frac{1}{2 f_{RUN}} - td \right)}$$

Component Selection Tips

Supply Bypassing and pc Board Layout Rules

Component selection and placement on the pc board is extremely important when using power control ICs. V_{CC} should be bypassed to COM as close to the IC terminals as possible with a low ESR/ESL capacitor, as shown in Figure 25.

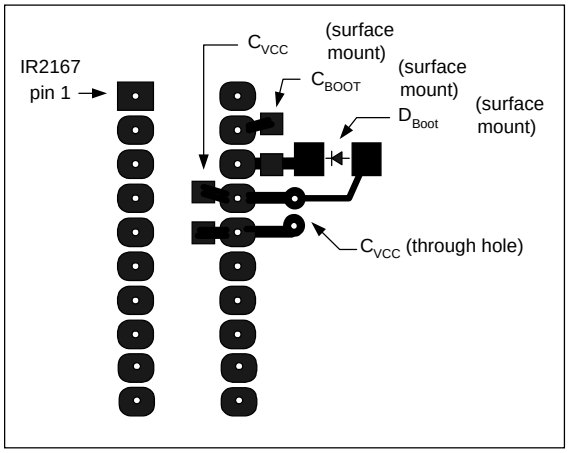


Figure 25: Supply bypassing PCB layout example

A rule of thumb for the value of this bypass capacitor is to keep its minimum value at least 2500 times the value of the total input capacitance (Ciss) of the power transistors being driven. This decoupling capacitor can be split between a higher valued electrolytic type and a lower valued ceramic type connected in parallel, although a good quality electrolytic (e.g., 10µF) placed immediately adjacent to the VCC and COM terminals will work well.

In a typical application circuit, the supply voltage to the IC is normally derived by means of a high value startup resistor (1/4W) from the rectified line voltage, in combination with a charge pump from the output of the half-bridge. With this type of supply arrangement, the internal 15.6V zener clamp diode from VCC to COM will determine the steady state IC supply voltage.

Connecting the IC Ground (COM) to the Power Ground

Both the low power control circuitry and low side gate driver output stage grounds return to this lead within the IC. The COM lead should be connected to the bottom terminal of the current sense resistor in the source of the low side power MOSFET using an individual pc board trace, as shown in Figure 26. In addition, the ground return path of the timing components and V_{CC} decoupling capacitor should be connected directly to the IC COM lead, and not via separate traces or jumpers to other ground traces on the board.

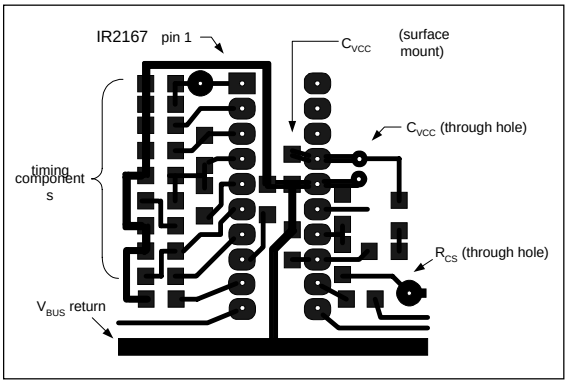
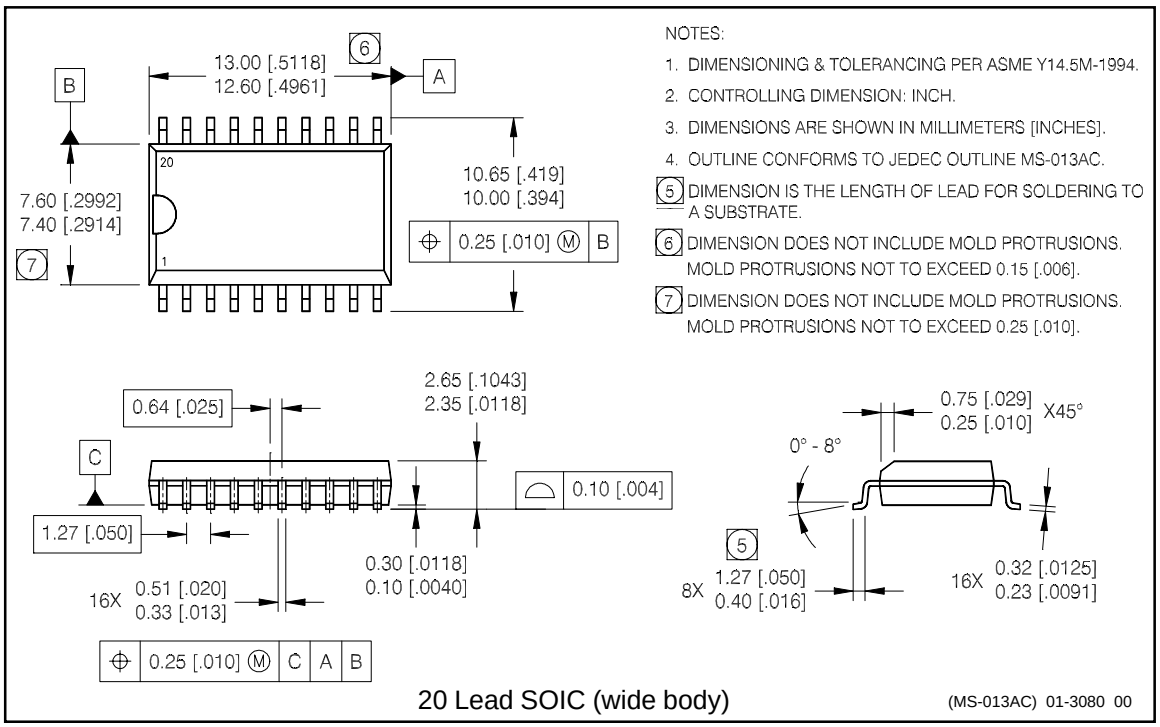


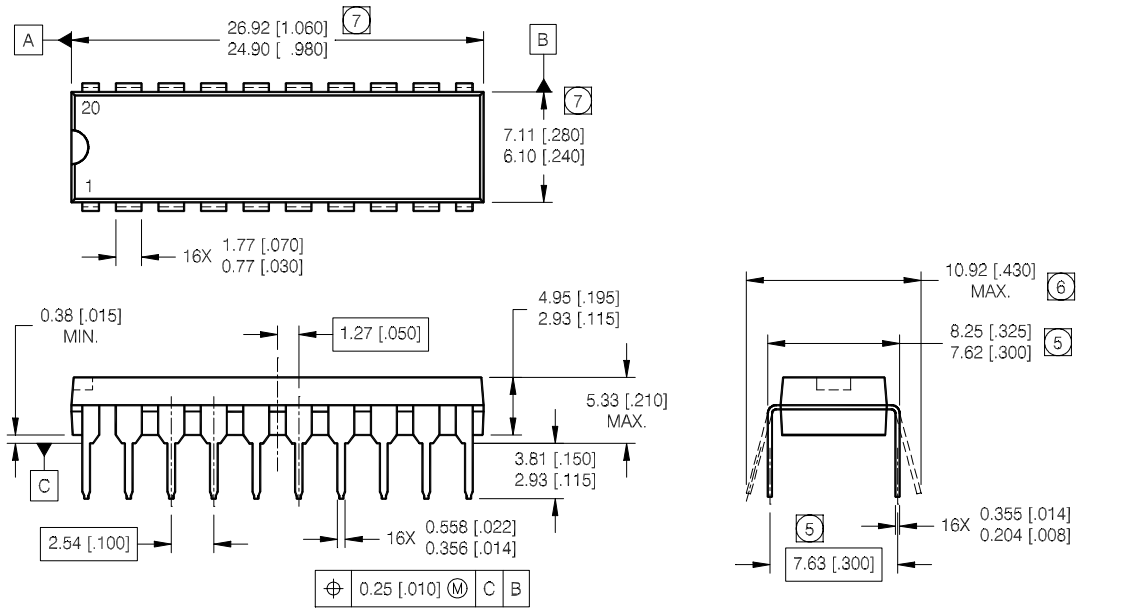
Figure 26: COM lead connection PCB layout example

These connection techniques prevent high current ground loops from interfering with sensitive timing component operation, and allows the entire control circuit to reject common-mode noise due to output switching.

Caseoutline



Caseoutline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AD.

5 DIMENSION MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

6 DIMENSION MEASURED AT LEAD TIPS WITH THE LEADS UNCONSTRAINED.

7 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

20 Lead PDIP (MS-001AD) 01-3079 00