LR4089B/LR4089BN

Tone Dialer LSI

DESCRIPTION

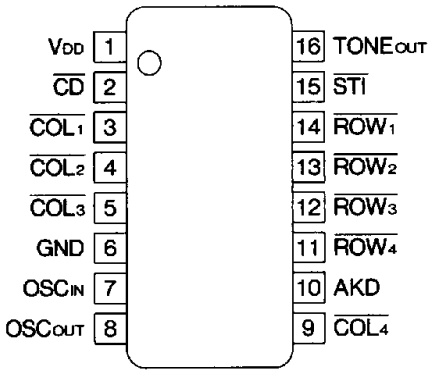
The LR4089B/LR4089BN are monolithic tone dialer LSI that uses an inexpensive crystal reference to provide eight audio sinusoidal frequencies. Dual-Tone Multi-Frequency signals are obtained by mixing these frequencies.

FEATURES

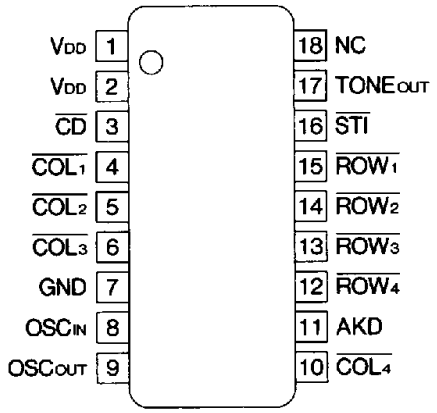
- Tone output : bipolar
  Mute output : N-channel open-drain
- Uses either a standard 2-of-8 matrix keyboard or a single contact keyboard
- Uses a 3.579 545 HMz color-burst crystal oscillator as a frequency reference
- Direct telephone-line operation
- Standard Dual-Tone-Multi-Frequency (DTMF) telephone dialing
- Generates signal tones
- On-chip regulation of dual and single tone amplitudes
- Packages :
  LR4089B : 16-pin DIP(DIP016-P-300B)
  LR4089BN : 18-pin MFP(MFP018-P)

PIN CONNECTIONS

16-PIN DIP TOP VIEW



18-PIN MFP



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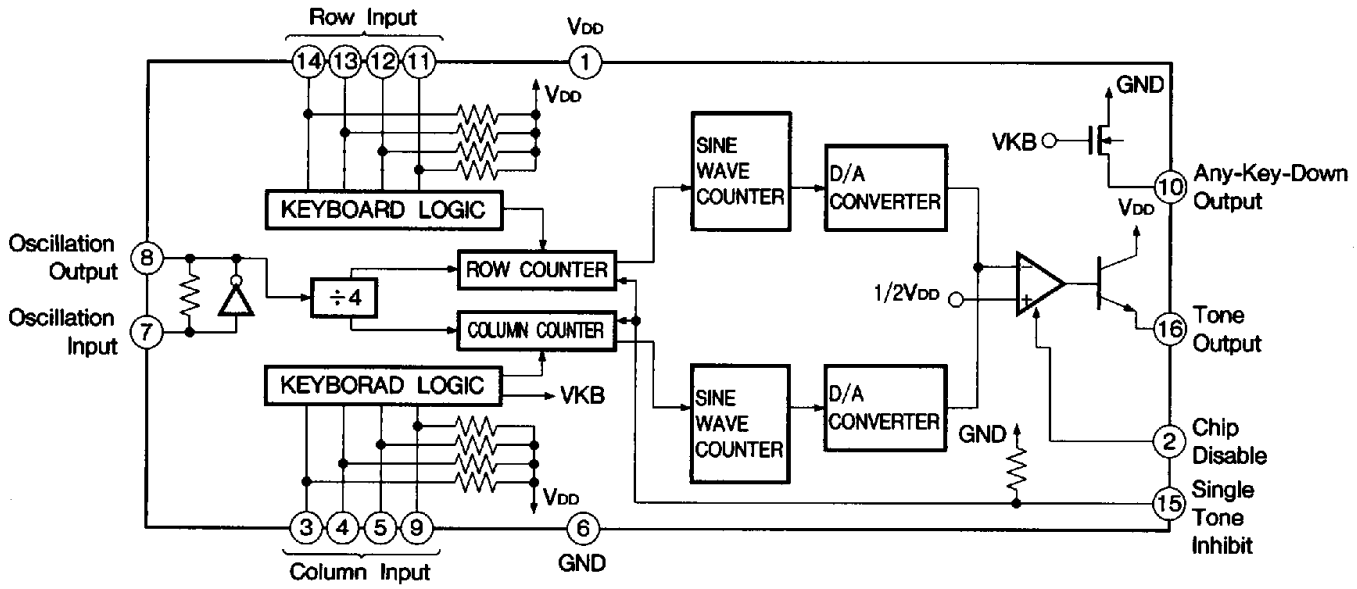
BLOCK DIAGRAM



NOTE :
Pin numbers apply to the 16-pin DIP.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{DD}	6.2	V	1
Operating temperature	Topr	−30 to +60	°C	
Storage temperature	Tstg	−55 to +150	°C	
Power dissipation	P_D	500	mW	2
Pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

NOTES :

1. Referenced to GND.
2. Ta = 25°C
3. The maximum applicable voltage on any pin with respect to GND.
4. The maximum applicable voltage on any pin with respect to V_{DD}.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}	2.5 to 6.0	V

ELECTRICAL CHARACTERISTICS

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input low voltage		V_{INL}		GND		0.3V_{DD}	V	1
Input high voltage		V_{INH}		0.7V_{DD}		V_{DD}	V	1
Input resistance		R_I	Ta = 25°C	20		200	kΩ	1, 2
TONE DISABLE input voltage		V_{INTD}		GND		0.3V_{DD}	V	
TONE output level		V_{OUT}	V_{DD} = 3.4 to 3.6 V, R_L = 10 kΩ	−10		−7.0	dBm	3, 11
Pre-emphasis				2.4	2.7	3.0	dB	4
TONE output distortion			V_{DD} = 2.5 to 6.0 V			−20	dB	5
Output rise time		tr			2.8	5.0	ms	6, 7
AKD output sink current		$I_{AKD\ ON}$	V_{OUT} = 0.5 V	500			μA	8
AKD output off current		$I_{AKD\ OFF}$	V_{OUT} = 5.0 V			2	μA	8
Supply current	During operation	I_{OP}	V_{DD} = 3.5 V			2.0	mA	9
	During standby	I_{SB}	V_{DD} = 6.0 V			3.0	μA	10
Tone input level (no key input)						−80	dBm	

NOTES :

1. Applies to $\overline{ROW}$ and $\overline{COL}$ input pins.
2. Applies to $\overline{STI}$ and $\overline{CD}$ input pins.
3. Applies to low group single tone signals.
4. Level ratio of high group tone signals to low group tone signals.
5. Unnecessary frequency component against basic tone signal total power (RMS) of $\overline{ROW}$ and $\overline{COL}$.
6. Rise time for tone output to reach 90% of maximum amplitude after key input.
7. Crystal resonator parameters : Rs = 100 Ω, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, F = 3.579 545 MHz.
8. AKD output is an N-channel open drain output.
9. In single key input, $\overline{CD}$ = "1", $\overline{STI}$ = "0".
10. During stand-by, $\overline{CO}$ = "1", $\overline{STI}$ = "0".
11. 0 dBm = 0.775 V (See TEST CIRCUIT)

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FUNCTIONAL DESCRIPTION

The Sharp LR4089B/LR4089BN are monolithic integrated circuits fabricated using the CMOS process. The LR4089B/LR4089BN use an inexpensive crystal reference oscillator to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing. The LR4089B/LR4089BN are designed specifically for integrated tone-dialer applications that require the following :

- Fixed supply operation
- Chip Disable input
- Stable output tone level
- An Any-Key-Down output
- Negative-true keyboard input

Keyboard entries select the ratios needed to divide the 3.579 545 MHz oscillator reference in order to obtain the required audio frequencies. These digital signals are then processed by a conventional R-2R ladder network. The tone output is a stair-step approximation of a sine wave, and requires little or no filtering for low-distortion applications.

The on-chip operational amplifier, that provides the current-to-voltage transformation for D/A conversion, also sums the high and low group signals to obtain the required dual tone. The accuracy of this type of tone generator is such that no frequency adjustment is needed to meet standard DTMF specifications.

Output Waveforms

The row and column output waveforms are shown in Fig. 1 and 2. These waveforms are digitally synthesized using on-chip D/A converters. Distortion measurements of these unfiltered waveforms shows a typical distortion of 7% or less. The on-chip operational amplifier of the LR4089B/LR4089BN mixes the row and column tones to form a dualtone waveform. Frequency analysis of this waveform shows harmonic and intermodulation distortion components to be typically −30 dB with respect to the strongest fundamental (column) tone.

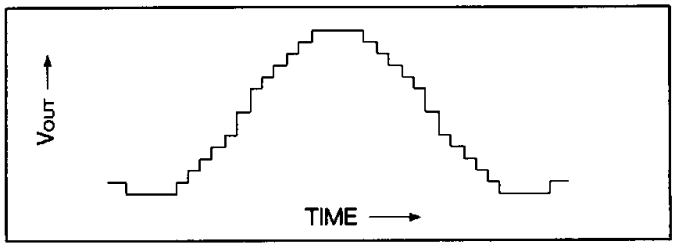

Fig. 1 Typical Sine Wave Output-Row Tones

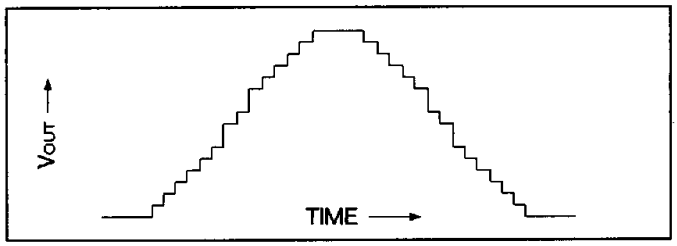

Fig. 2 Typical Sine Wave Output-Column Tones

PIN DESCRIPTIONS (Applied to LR4089B)

$\overline{\text{ROW}}$ and $\overline{\text{COLUMN}}$ Inputs (Pins 11, 12, 13, 14 and Pins 3, 4, 5, 9)

Each keyboard input is standard CMOS with a pull-up resistor to the V_{DD} supply. These inputs may be controlled by a keyboard or by electronic means. Open collector TTL or standard CMOS logic may be used for electronic control. The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1 kΩ as a valid key closure.

With $\overline{\text{Single Tone Inhibit}}$ at V_{DD}, connection of GND to a single column will cause the generation of that column tone. Connection of GND to more than one column will result in no tones being generated.

The application of GND to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to GND for row tones to be generated. If a single row tone is desired, it may be generated by tying any two column pins and the desired row pin to GND. Dual tones will be generated if a single row pin and a single column pin are connected to GND.

Keyboard configuration and electronic input are shown below.

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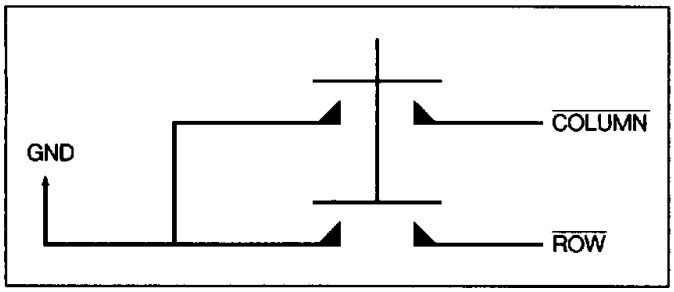

Fig. 3 Keyboard Configuration

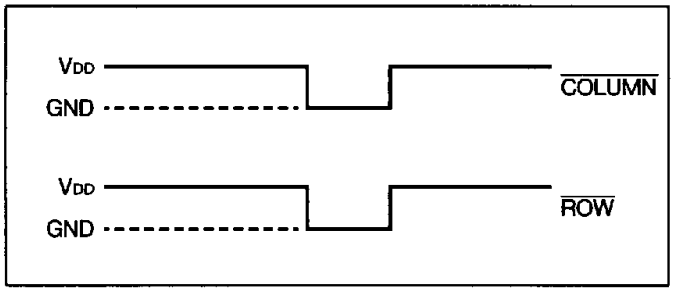

Fig. 4 Electronic Input

Chip Disable Input (Pin 2)

The Chip Disable input is used to disable tone generation when the keyboard is used for functions other than DTMF signaling. It is a pulled up to the VDD supply. When tied to the GND supply, tones are inhibited, but all other chip functions operate normally.

Any-Key-Down Output (Pin 10)

The Any-Key-Down output is used to control receiver and/or transmitter switching and other desired functions.

It switches to the GND supply when a keyboard button is pushed; otherwise it is left open circuit. The AKD output switches regardless of the state of the Chip Inhibit and Single Tone Disable inputs.

Single Tone Inhibit (Pin 15)

The Single Tone Inhibit input is used to inhibit all but dual tone generation. It is pulled down to the GND supply and, when floating or tied to GND, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally. When forced to the VDD supply, single or dual tones may be generated as described under row and column Inputs.

Oscillator (Pin 7 and 8)

The network contains an on-board inverter with sufficient loop-gain to provide oscillation when used with a low-cost television color-burst crystal. The inverter's input is OSCIN (pin 7) and output is OSCOUT (pin 8). The circuit, designed to work with a 3.579 545 MHz crystal, produces the frequencies shown in Table 1.

Crystal frequency deviations will be reflected in the tone output frequency.

Table 1 DTMF Output Frequencies

	STANDARD DTMF (Hz)	LR4089B TONE OUTPUT FREQUENCY USING A 3.579545 MHz CRYSTAL	STANDARD DEVIATION (%)
f_1	697	701.3	+0.62
f_2	770	771.4	+0.19
f_3	852	857.2	+0.61
f_4	941	935.1	−0.63
f_5	1209	1215.9	+0.57
f_6	1336	1331.7	−0.32
f_7	1477	1471.9	−0.35
f_8	1633	1645.0	+0.73

Tone Output (Pin 16)

The Tone Output pin is connected internally in the LR4089B to the emitter of an NPN transistor whose collector is tied to VDD.

The on-chip operational amplifier, which mixes the row and cloumn tones together and provides output level regulation, supplies the input to this transistor.

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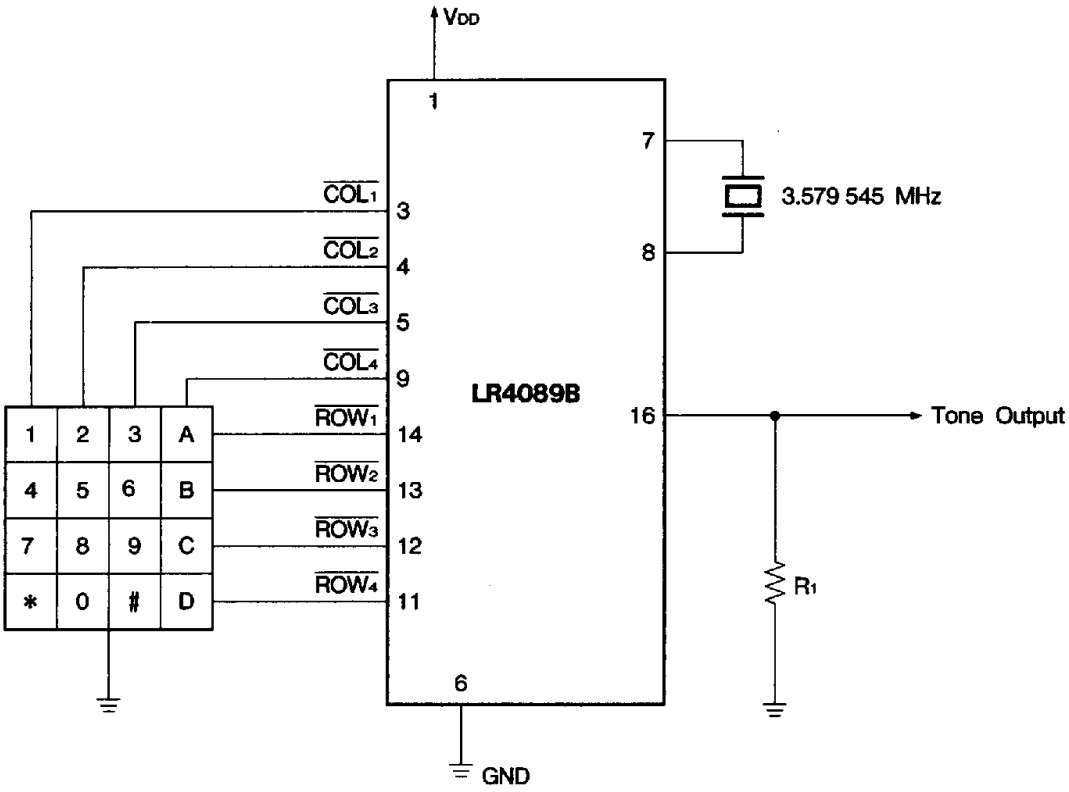
TEST CIRCUIT



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