MN3644D

2048-Bit High-Responsivity CCD Linear Image Sensor with Internal Clock Driver

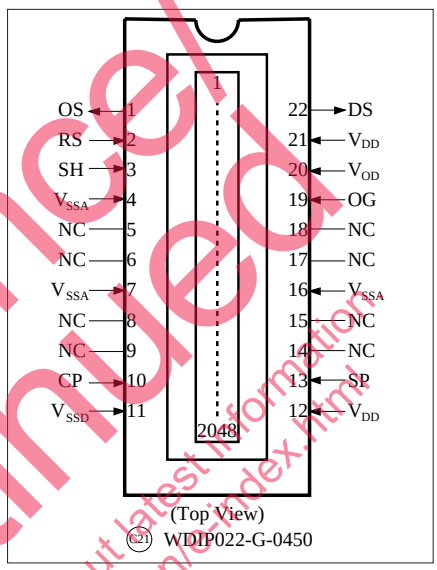
■ Overview

The MN3644D is a high responsivity CCD linear image sensor having floating photodiodes in the photodetector region, CCD analog shift registers for read out, and a built-in clock driver.
It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

■ Features

- 2048 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Since a clock driver circuit is built in, it is possible to drive this device using CMOS or TTL 5V logic.
- Large signal output of typically 1500mV at saturation can be obtained.
- Because a sample hold circuit is built in, the output waveform makes signal processing easy.
- Since a compensation output pin (DS) is provided in addition to the signal output pin (OS), it is possible to obtain a signal with a high S/N ratio by carrying out differential amplification of the OS and DS outputs.
- Operation with a single +12V positive power supply.

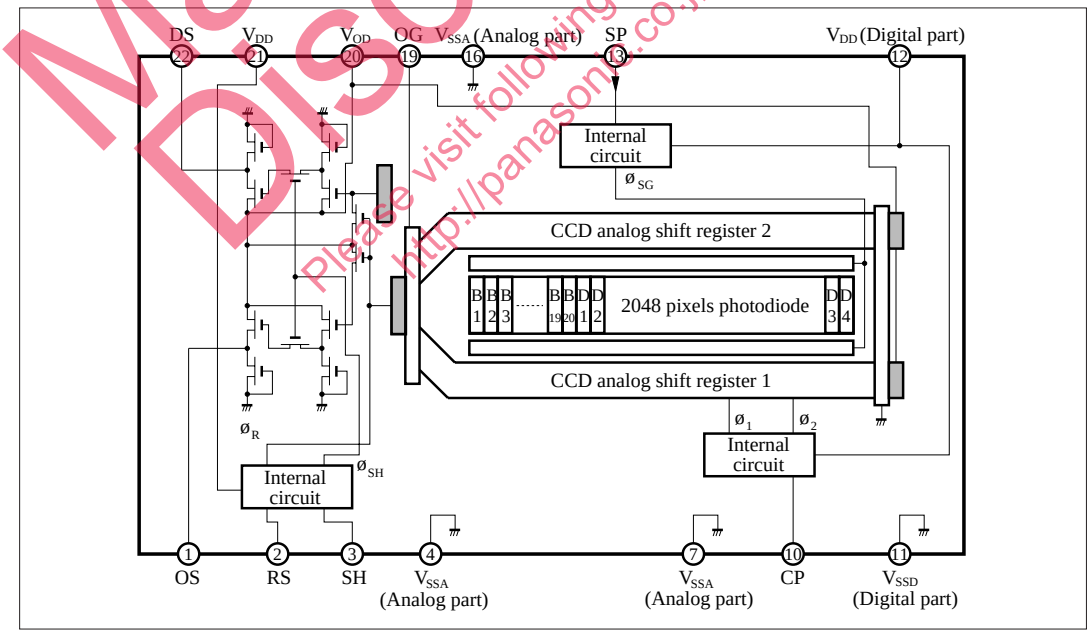
■ Pin Assignments



■ Application

- Barcode readers
- Measurement of position and dimensions of objects.

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C, V_{SSA}=V_{SSD}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +17	V
	V_{OD}	– 0.3 to +17	V
Input pin voltage	V_I	– 0.3 to +17	V
Output pin voltage	V_O	– 0.3 to +17	V
Operating temperature range	T_{opr}	–20 to + 60	˚C
Storage temperature range	T_{stg}	–40 to +100	˚C

■ Operating Conditions

• Voltage conditions (Ta=–20 to +60˚C, V_{SSA}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Internal clock driver power supply voltage	V_{DD}	V_{OD}=V_{DD}	11.4	12.0	13.6	V
CCD output circuit power supply voltage	V_{OD}		11.4	12.0	13.6	V
Output gate voltage	V_{OG}		4.2	4.5	5.1	V
Shift register clock High level	V_{CPH}		4.5	5.0	5.5	V
Shift register clock Low level	V_{CPL}		0	—	0.5	V
Shift clock High level	V_{SPH}		4.5	5.0	5.5	V
Shift clock Low level	V_{SPL}		0	—	0.5	V
Reset clock High level	V_{RSH}		4.5	5.0	5.5	V
Reset clock Low level	V_{RSL}		0	—	0.5	V
Rimple hold clock High level	V_{SHH}		4.5	5.0	5.5	V
Rimple hold clock Low level	V_{SHL}		0	—	0.5	V

• Timing conditions

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	f_C =1/2T, f_R =1/T=data rate	40	—	750	kHz
Reset clock frequency	f_R		80	—	1500	kHz
Shift register clock rise time	t_{Cr}		0	15	50	ns
Shift regisster clock fall time	t_{Cf}		0	15	50	ns
Shift clock rise time	t_{Sr}		0	15	50	ns
Shift clock fall time	t_{Sf}		0	15	50	ns
Shift clock set up time	t_{Ss}		0	400	1000	ns
Shift clock pulse width	t_{Sw}		10	12	50	ns
Shift clock hold time	t_{Sh}		0	1	10	ns
Reset clock rise time	t_{Rr}		0	15	50	ns
Reset clock fall time	t_{Rf}		0	15	50	ns
Reset clock set up time	t_{Rs}		0.7T	—	—	ns
Reset clock pulse width	t_{Rw}		100	150	—	ns
Reset clock hold time	t_{Rh}		0	10	—	ns
Sample hold clock rise time	t_{Hr}		0	15	50	ns
Sample hold clock fall time	t_{Hf}		0	15	50	ns
Sample hold clock set up time	t_{HS}		350	—	—	ns
Sample hold clock pulse width	t_{HW}		100	150	—	ns
Sample hold clock hold time	t_{Hh}		100	—	—	ns

• Clock input capacitance (Ta=–20 to +60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	C_{CP}	f =1MHz	—	10	—	pF
Shift clock input capacitance	C_{SP}		—	10	—	pF
Reset clock input capacitance	C_{RS}		—	10	—	pF
Sample hold clock input capacitance	C_{SH}		—	10	—	pF

• DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{CC}	V_{DD}=V_{OD}=+12V, f_R=500kHz	—	15	30	mA
Output gate leak current	I_{OG}	V_{OG}=+4.5V	—	—	1	mA

■ Optical Characteristics

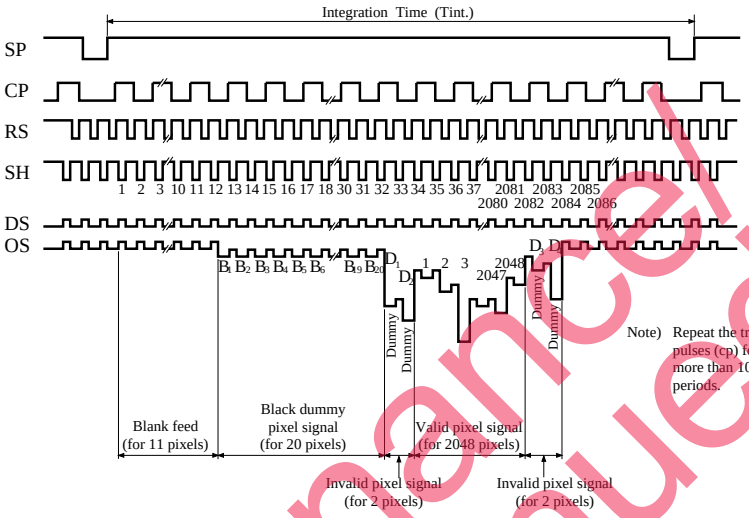
Parameter	Symbol	Condition	min	typ	max	Unit
Saturation output voltage	V_{SAT}		1000	1500	—	mV
Saturation exposure	SE		3.0	—	—	mlx·s
Output voltage at constant exposure (Responsivity)	$V_{CEmin.}$	1.5mlx·s	345	—	495	mV
Photoresponse non-uniformity	PRNU	1.5mlx·s	—	—	20	%
Bit non-uniformity	BNU	1.5mlx·s	—	—	±10	%
Odd/even bit non-uniformity	O/E	1.5mlx·s	—	1	5	%
Dark signal output voltage	Vd	Dark condition	—	10	20	mV
Shift register total transfer efficiency	STTE	1.5mlx·s	92	99	—	%
Modulation transfer function (f_{NYq}=Nyquist spatial frequency)	MTFR	Space frequency $1 \times f_{NVq}$	—	64	—	%
		Space frequency $1/2 \times f_{NVq}$	—	84	—	%
		Space frequency $1/3 \times f_{NVq}$	—	97	—	%

■ Pin Descriptions

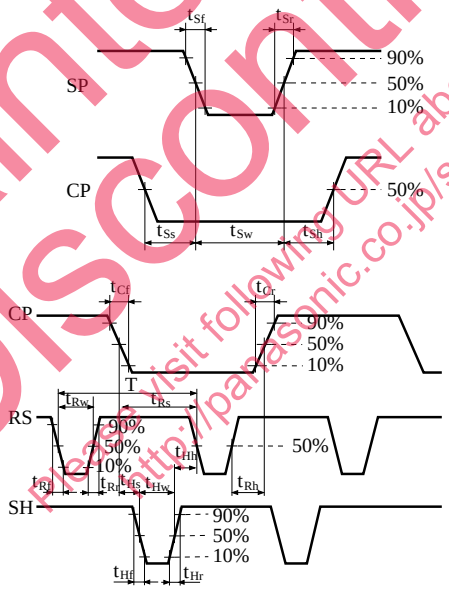
Pin No.	Symbol	Pin name	Condition
1	OS	Signal output	
2	RS	Reset clock	
3	SH	Sample hold clock	
4	V_{SSA}	Analog ground	Connected to the substrate.
5	NC	Non connection	
6	NC	Non connection	
7	V_{SSA}	Analog ground	Connected to the substrate.
8	NC	Non connection	
9	NC	Non connection	
10	CP	CCD shift register clock	
11	V_{SSD}	Digital ground	Ground pin for the internal clock driver.
12	V_{DD}	Internal clock driver power supply	
13	SP	Shift clock	
14	NC	Non connection	
15	NC	Non connection	
16	V_{SSA}	Analog ground	Connected to the substrate.
17	NC	Non connection	
18	NC	Non connection	
19	OG	Output gate	
20	V_{OD}	CCD Output part power supply	
21	V_{DD}	Internal clock driver power supply	
22	DS	Compensation output	

■ Timing Diagram

(1) I/O timing



(2) Drive timing



■ Construction of the Image Sensor

The MN3644D can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11µm floating photodiode and a 3µm channel stopper for each pixel, and 2048 of these devices are linearly arranged side by side at a pitch of 14µm.
- The photo detector's windows are 14µm × 200µm rectangle and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 20 optically shielded pixels (black reference pixels) which serve as the black reference.

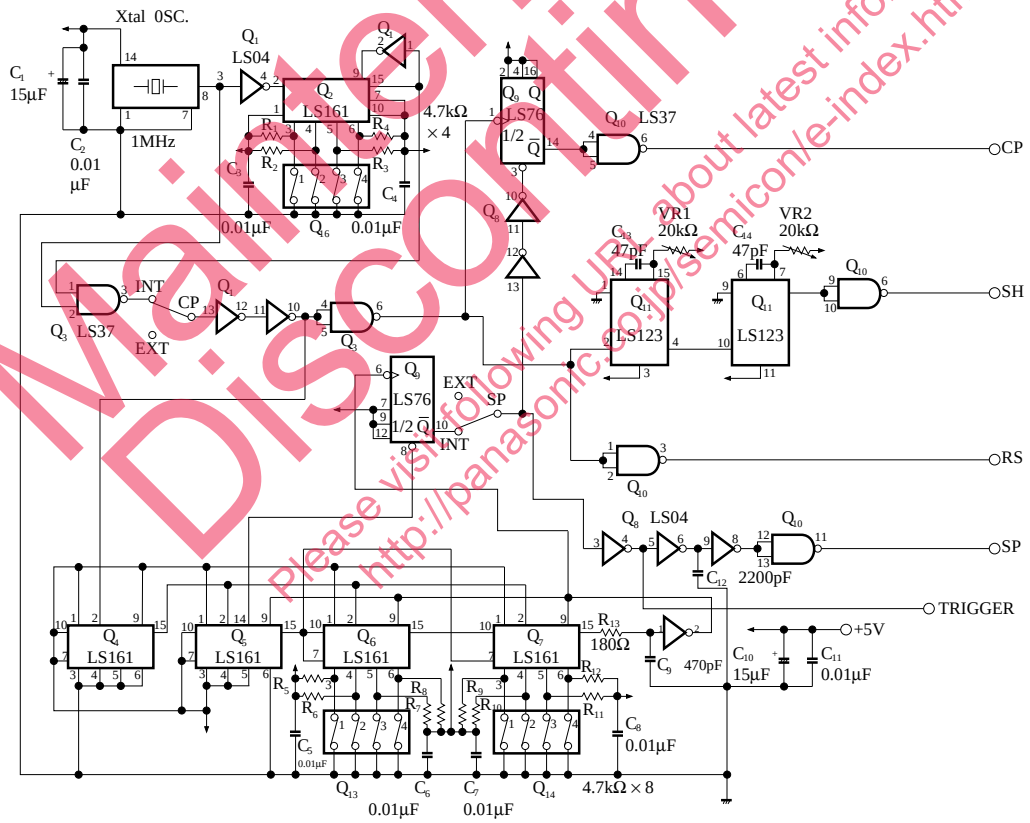
b) CCD Transfer region (shift register)

- The light output that has been photoelectrically converted is transferred to the CCD transfer for each odd and even pixel at the timing of the shift clock (SP). The optical signal charge transferred to this analog shift register is successively transferred out and guided to the output region.
- A buried type CCD that can be driven by a two phase clock ($ø_1$, $ø_2$) is used for the analog shift register. The 2-phase clock is being generated based on the CCD shift register clock (CP) by the built-in clock driver circuit.

c) Output region

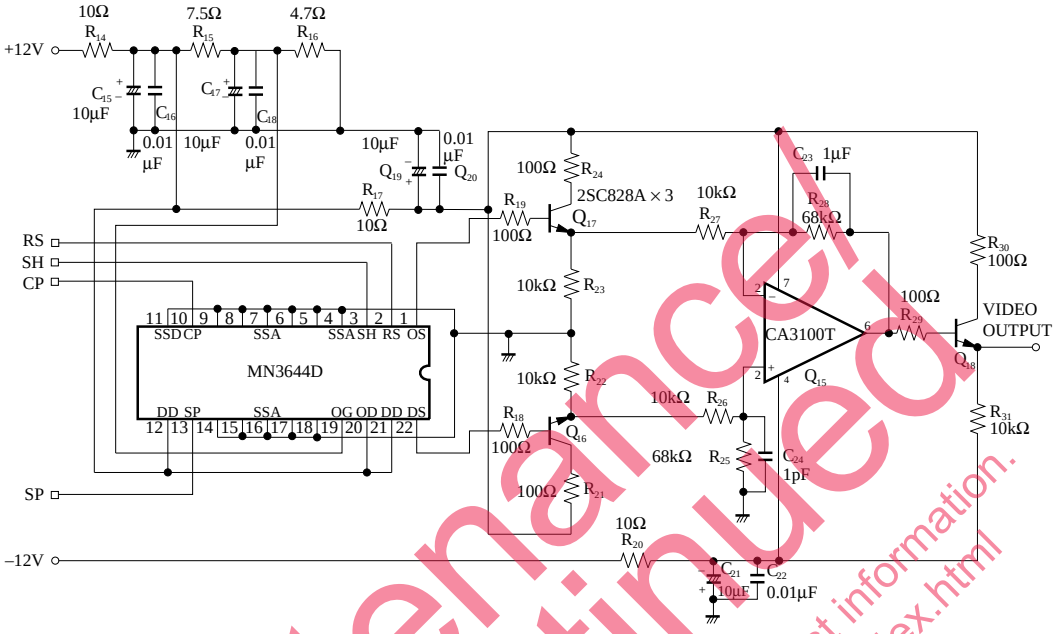
- The signal charge transferred to the output region is sent to the detector region, passed through a sample hold circuit, and is impedance converted by a source follower amplifier.
- The DC level component and the clock noise component not containing optical signals are output from the DS pin.
- By carrying out differential amplification of the two outputs OS and DS externally, it is possible to obtain an output signal with a high S/N ratio by reducing the clock noise, etc.

■ Drive Circuit Diagram (Digital Section)



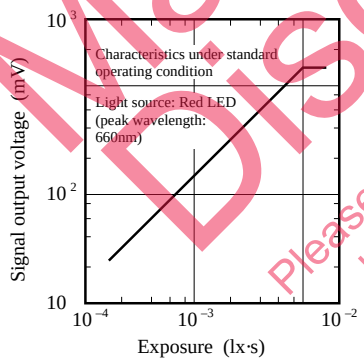
- Connect a 0.01µF capacitor between the V_{CC} and GND pins of each TTL.
- Set VR_1 and VR_2 so that an optimum sample hold operation can be performed.

■ Drive Circuit Diagram (Analog Section)

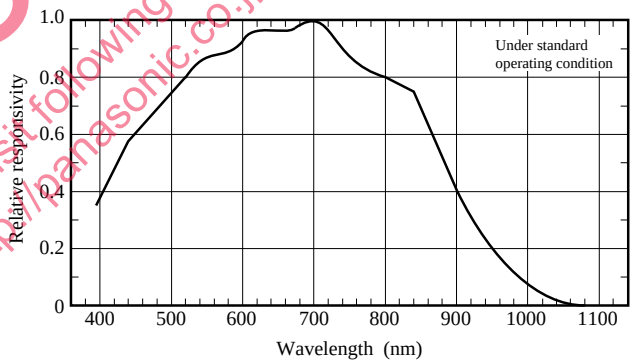


■ Graphs and Characteristics

Photoelectric Conversion Characteristics



Spectral Response Characteristics



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