

# MN3610

## 2048-Bit CCD Linear Image Sensor

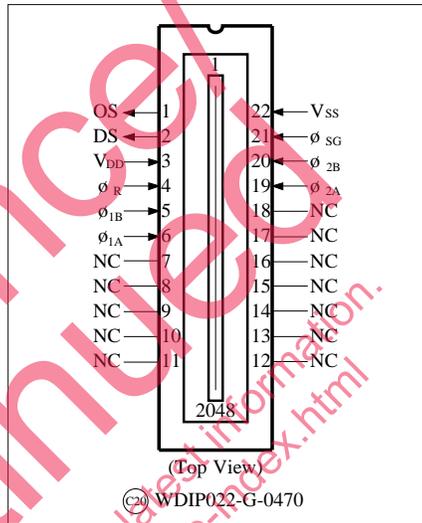
### ■ Overview

The MN3610 is a 2048-pixel high sensitivity CCD linear image sensor combining photo-sites using low dark output floating photodiodes and CCD analog shift registers for read out. It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

### ■ Features

- 2048 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Use of photodiodes with a new structure has made the dark output voltage very low.
- Has a smooth spectral characteristics that is close to the sensitivity of the human eye in the entire visible region.
- Large signal output of typically 2300mV at saturation can be obtained.
- Since a compensation output pin (DS) is provided in addition to the signal output pin (OS), it is possible to obtain a signal with a high S/N ratio by carrying out differential amplification of the OS and DS outputs.
- Operation with a single +12V positive power supply.

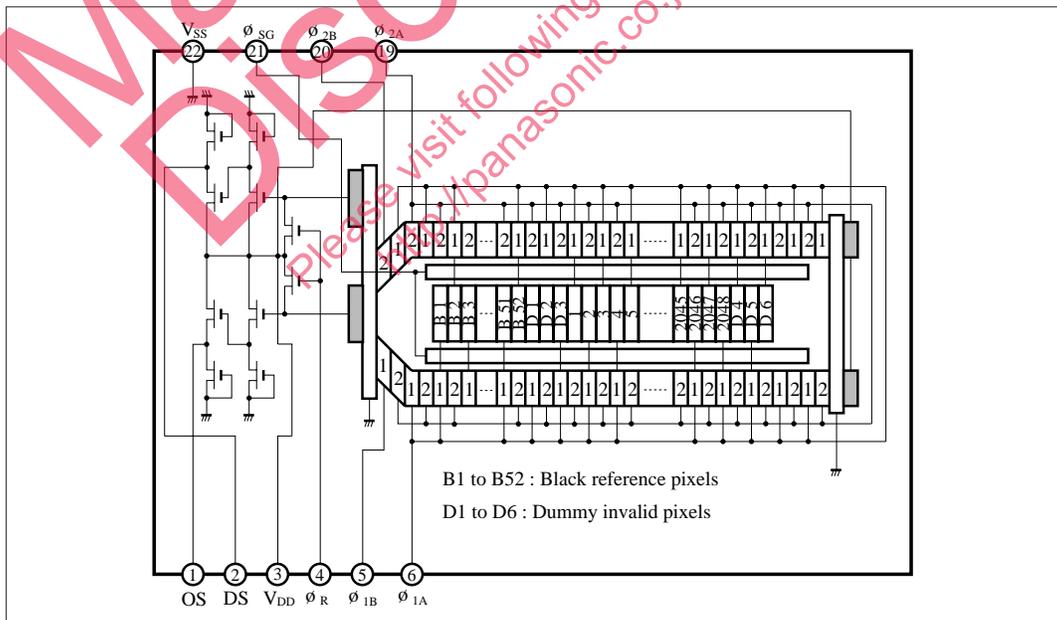
### ■ Pin Assignments



### ■ Application

- Graphic and character read out in fax machines, image scanners, etc.
- Measurement of position and dimensions of objects.

### ■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C, Vss=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V <sub>DD</sub>	-0.3 to +17	V
Input pin voltage	V <sub>I</sub>	-0.3 to +17	V
Output pin voltage	V <sub>O</sub>	-0.3 to +17	V
Operating temperature range	T <sub>opr</sub>	-20 to +60	°C
Storage temperature range	T <sub>stg</sub>	-40 to +100	°C

■ Operating Conditions

- Voltage conditions (Ta=-20 to +60°C, Vss=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V <sub>DD</sub>		11.4	12.0	13.0	V
CCD shift register clock High level	V <sub>sH</sub>		V <sub>DD</sub> -1	V <sub>DD</sub>	V <sub>DD</sub>	V
CCD shift register clock Low level	V <sub>sL</sub>		0	0.5	0.8	V
Shift gate clock High level	V <sub>SH</sub>		V <sub>DD</sub> -1	V <sub>DD</sub>	V <sub>DD</sub>	V
Shift gate clock Low level	V <sub>SL</sub>		0	0.5	0.8	V
Reset gate clock High level	V <sub>RH</sub>		V <sub>DD</sub> -1	V <sub>DD</sub>	V <sub>DD</sub>	V
Reset gate clock Low level	V <sub>RL</sub>		0	0.5	0.8	V

- Timing conditions (Ta=-20 to +60°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f <sub>c</sub>	f <sub>c</sub> =1/2T	—	0.5	—	MHz
Reset clock frequency	f <sub>R</sub>	See drive timing diagram. f <sub>R</sub> =1/T	—	1.0	—	MHz
Shift register clock rise time	t <sub>cr</sub>		0	100	—	ns
Shift register clock fall time	t <sub>cf</sub>		0	100	—	ns
Shift clock rise time	t <sub>sr</sub>		0	50	—	ns
Shift clock fall time	t <sub>sf</sub>		0	50	—	ns
Shift clock set up time	t <sub>ss</sub>		0	100	—	ns
Shift clock pulse width	t <sub>sw</sub>		200	1000	—	ns
Shift clock hold time	t <sub>sh</sub>		0	100	—	ns
Reset clock rise time	t <sub>Rr</sub>		0	20	—	ns
Reset clock fall time	t <sub>Rf</sub>		0	20	—	ns
Reset clock set up time	t <sub>Rs</sub>		0.7T	—	—	ns
Reset clock pulse width	t <sub>Rw</sub>		40	250	—	ns
Reset clock hold time	t <sub>Rh</sub>		10	250	—	ns

### ■ Electrical Characteristics

- Clock input capacitance (Ta=-20 to+60°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	C <sub>1A</sub> , C <sub>2A</sub>	V <sub>IN</sub> =12V f =1MHz	—	450	—	pF
Shift register final stage clock input capacitance	C <sub>1B</sub> , C <sub>2B</sub>		—	10	—	pF
Reset clock input capacitance	C <sub>R</sub>		—	10	—	pF
Shift clock input capacitance	C <sub>S</sub>		—	150	—	pF

- DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I <sub>DD</sub>	V <sub>DD</sub> =+12V	—	5	12	mA

- AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output delay time	t <sub>os</sub>		—	50	—	ns

### ■ Optical Characteristics

<Inspection conditions >

- Ta=25°C, V<sub>DD</sub>=12V, V<sub>OH</sub>=V<sub>SH</sub>=V<sub>RH</sub>=12V (pulse), f<sub>C</sub>=0.5MHz, f<sub>R</sub>=1MHz, T<sub>int</sub> (accumulation time)=10ms
- Light source: Daylight type fluorescent lamp
- Optical system: A slit with an aperture dimensions of 20mm × 20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- Load resistance = 100k Ohms
- specifications apply to the 2048 valid pixels excluding the dummy pixels D1 to D6.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R		6.4	7.4	8.4	V/lx·s
Photo response non-uniformity	PRNU	Note 1	—	—	10	%
Odd/even bit non-uniformity	O/E	Note 2	—	—	3	%
Saturation output voltage	V <sub>SAT</sub>	Note 3	1.7	2.3	—	V
Saturation exposure	SE	Note 3	0.20	0.30	—	lx · s
Dark signal output voltage	V <sub>DRK</sub>	Dark condition, see Note 4	—	0.2	1.0	mV
Dark signal output non-uniformity	DSNU	Dark condition, see Note 4	—	0.1	2.0	mV
Shift register total transfer efficiency	STTE		92	—	—	%
Output impedance	Z <sub>o</sub>		—	—	1	k Ω
Dynamic range	DR	Note 5	—	11500	—	
Signal output pin DC level	V <sub>OS</sub>	Note 6	3.5	4.5	6.0	V
Compensation output pin DC level	V <sub>DS</sub>	Note 6	3.5	4.5	6.0	V
Signal and compensation output pin DC level difference	V <sub>OS</sub> -V <sub>DS</sub>	Note 6	—	20	100	mV

Note 1) The photo response non-uniformity (PRNU) is defined by the following equation, where X<sub>ave</sub> is the average output voltage of the 2048 valid pixels and Δx is the absolute value of the difference between X<sub>ave</sub> and the voltage of the maximum (or minimum) output pixel, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

$$PRNU = \frac{\Delta x}{X_{ave}} \times 100 (\%)$$

The incident light intensity shall be 50% of the standard saturation light intensity.

Note 2) The odd/even bit non-uniformity (O/E) is defined by the following equation, where X<sub>ave</sub> is the average output voltage of the 2048 valid pixels and X<sub>n</sub> is the output voltage of the 'n'th pixel, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

$$O/E = \frac{\sum_{n=1}^{2047} |X_n - X_{n+1}|}{2047 \times X_{ave}} \times 100 (\%)$$

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■ Optical Characteristics (continued)

In other words, this is the value obtained by dividing the average of the output difference between the odd and even pixels by the average output voltage of all the valid pixels. The incident light intensity shall be 50% of the standard saturation light intensity.

Note 3) The Saturation output voltage ( $V_{SAT}$ ) is defined as the output voltage at the point when the linearity of the photoelectric characteristics cannot be maintained as the incident light intensity is increased. (The light intensity of exposure at this point is called the saturation exposure.)

Note 4) The dark signal output voltage ( $V_{DRK}$ ) is defined as the average output voltage of the 2048 pixels in the dark condition at  $T_a=25^\circ\text{C}$  and  $T_{int}=10\text{ms}$ . Normally, the dark output voltage doubles for every 8 to  $10^\circ\text{C}$  rise in  $T_a$ , and is proportional to  $T_{int}$ .

The dark signal output non-uniformity (DSNU) is defined as the difference between the maximum output voltage among all the valid pixels and  $V_{DRK}$  in the dark condition at  $T_a=25^\circ\text{C}$  and  $T_{int}=10\text{ms}$ .



Note 5) The dynamic range is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

Note 6) The signal output pin DC level ( $V_{OS}$ ) and the compensation output pin DC level ( $V_{DS}$ ) are the voltage values shown in the following figure.



■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS	Signal output	
2	DS	Compensation output	
3	V <sub>DD</sub>	Power supply	
4	$\phi_R$	Reset clock	
5	$\phi_{1B}$	CCD Final stage clock (Phase 1)	
6	$\phi_{1A}$	CCD Clock (Phase 1)	
7	NC	Non connection	
8	NC	Non connection	
9	NC	Non connection	
10	NC	Non connection	
11	NC	Non connection	
12	NC	Non connection	
13	NC	Non connection	
14	NC	Non connection	
15	NC	Non connection	
16	NC	Non connection	
17	NC	Non connection	
18	NC	Non connection	
19	$\phi_{2A}$	CCD Clock (Phase 2)	
20	$\phi_{2B}$	CCD Final stage clock (Phase 2)	
21	$\phi_{SG}$	Shift gate clock	
22	V <sub>SS</sub>	Ground	

Note) Connect all NC pins externally to V<sub>SS</sub>.

■ Construction of the Image Sensor

The MN3610 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11µm floating photodiode and a 3µm channel stopper for each pixel, and 2048 of these devices are linearly arranged side by side at a pitch of 14µm.
- The photo detector's windows are 14µm × 14µm squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 52 optically shielded pixels (black dummy pixels) which serve as the black reference.

b) CCD Transfer region (shift register)

- The light output that has been photoelectrically converted is

transferred to the CCD transfer for each odd and even pixel at the timing of the shift clock ( $\phi_{SG}$ ). The optical signal electric charge transferred to this analog shift register is successively transferred out and guided to the output region.

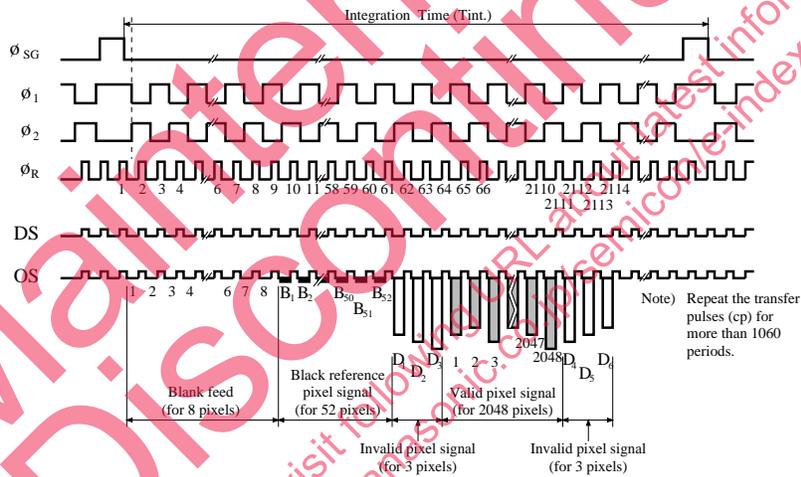
- A buried type CCD that can be driven by a two phase clock ( $\phi_1, \phi_2$ ) is used for the analog shift register.

c) Output region

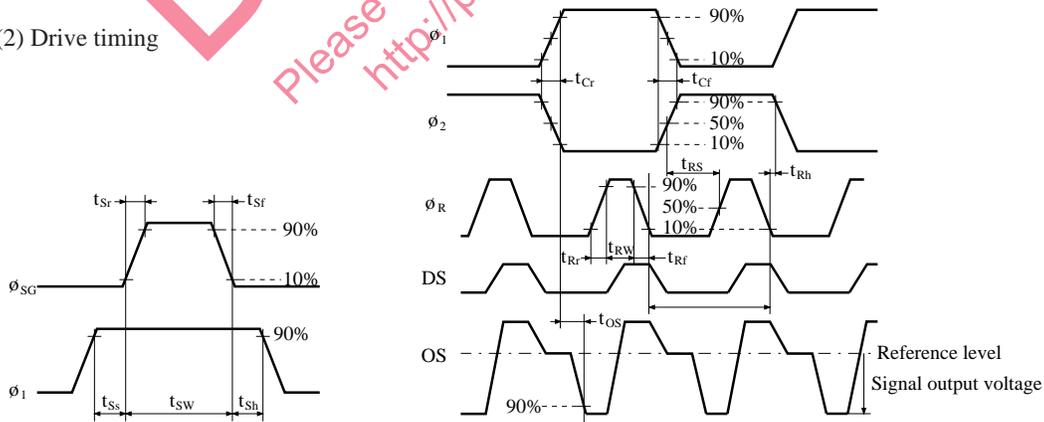
- The signal charge that is transferred to the output region is sent to the detector where impedance transformation is done using two source follower stages.
- The DC level component and the clock noise component not containing optical signals are output from the DS pin.
- By carrying out differential amplification of the two outputs OS and DS externally, it is possible to obtain an output signal with a high S/N ratio by reducing the clock noise, etc.

■ Timing Diagram

(1) I/O timing

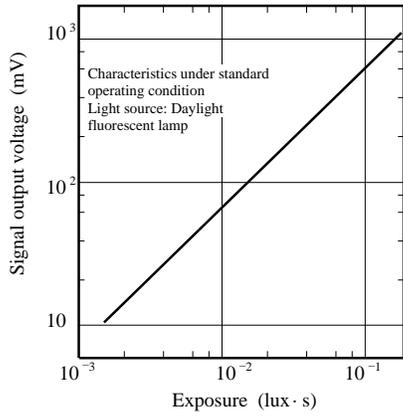


(2) Drive timing

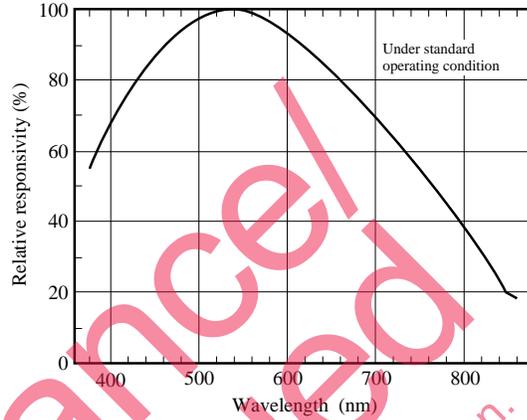


■ Graphs and Characteristics

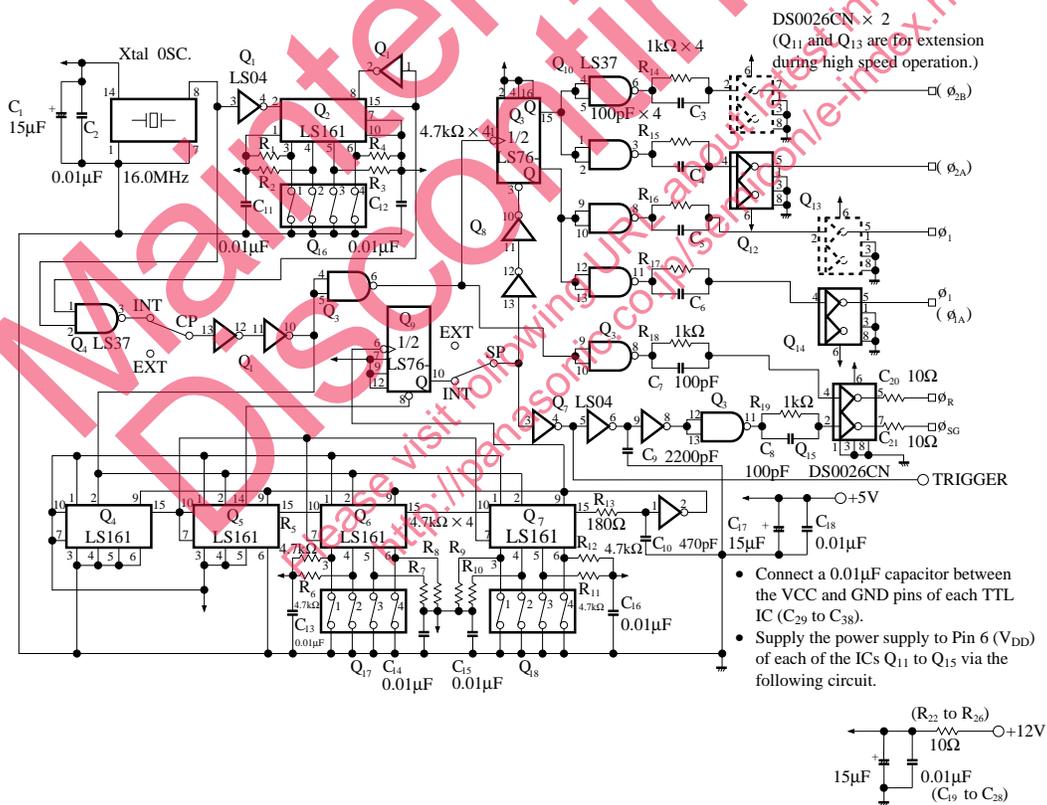
Photoelectric Conversion Characteristics



Spectral Response Characteristics



■ Drive Circuit Diagram (Digital Section)





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