

5000-BIT  $\times$  3 CCD COLOR LINEAR IMAGE SENSOR

The  $\mu$ PD3725A is a high sensitivity 5000-bit  $\times$  3 CCD (Charge Coupled Device) color linear image sensor which changes optical images to electrical signal and has the function of color separation.

The  $\mu$ PD3725A has 3 rows of 5000-bit photocell array and 6 rows of 2500-bit charge transferred register, so it is suitable for high resolution color image scanners and digital color copiers.

## FEATURES

- Valid photocell : 5000-bit  $\times$  3
- Photocell's pitch : 14  $\mu$ m
- Line distance : 112  $\mu$ m (8 lines) R(red) bit-G(green) bit, Gbit-B(blue)bit
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance  $10^7$ lx $\cdot$ Hour)
- Resolution : 16 dot/mm across the shorter side of a B4-size (257  $\times$  364 mm) sheet
- Drive clock level : CMOS output under 5 V operation
- Data rate : 16 MHz MAX.
- High speed scan : 320  $\mu$ s/line
- Power supply : +12 V

CHANGED POINTS from the  $\mu$ PD3725D-01

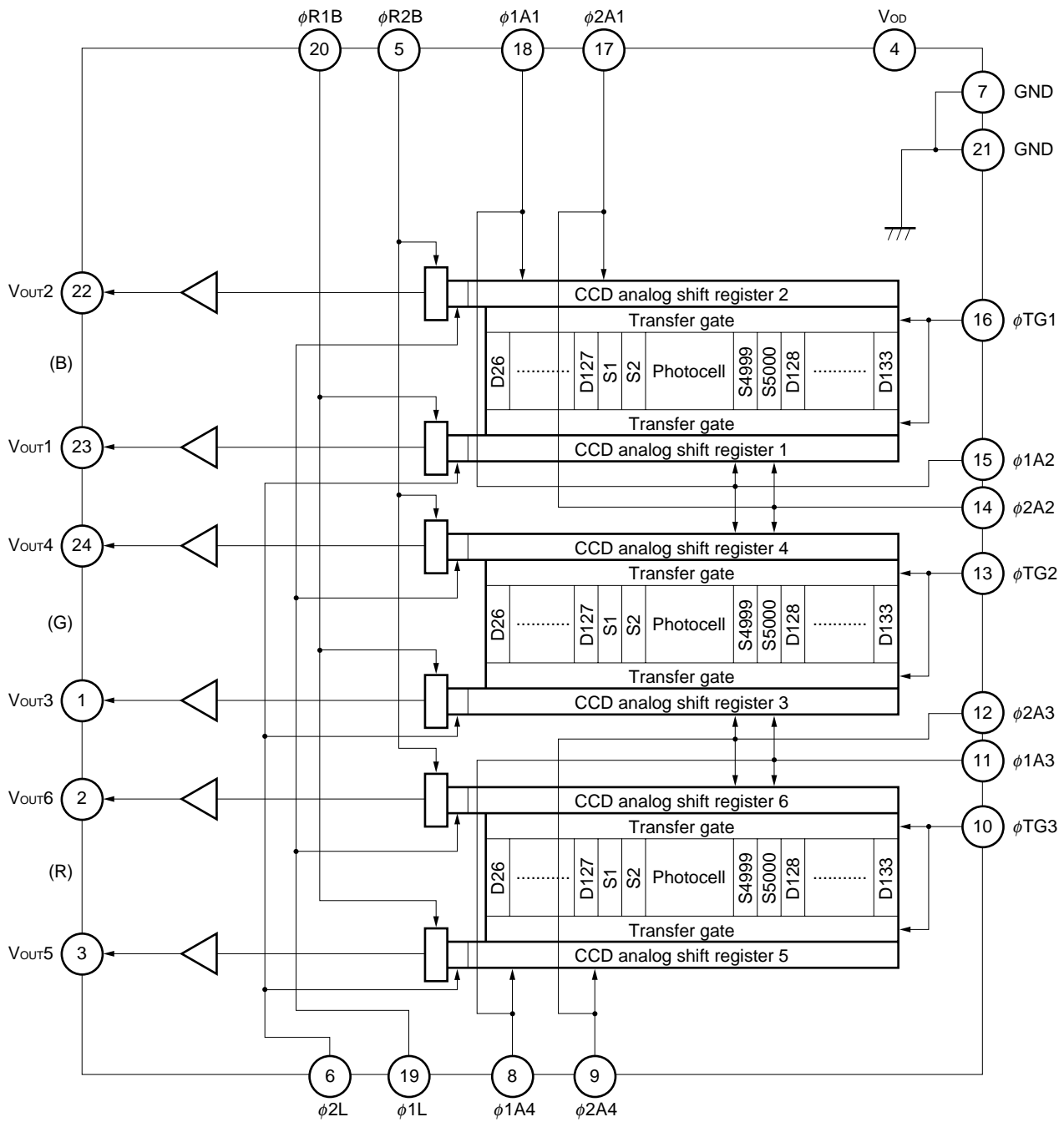
- Pins 18 and 15, 17 and 14, 11 and 8, 12 and 9 are each connected inside of the device (refer to **BLOCK DIAGRAM**).
- The specification of the total transfer efficiency (TTE) is improved from 92 % to 93.5 % (MIN.) (refer to **ELECTRICAL CHARACTERISTICS**).

## ORDERING INFORMATION

Part Number	Package
$\mu$ PD3725AD	CCD linear image sensor 24-pin ceramic DIP (600 mil)

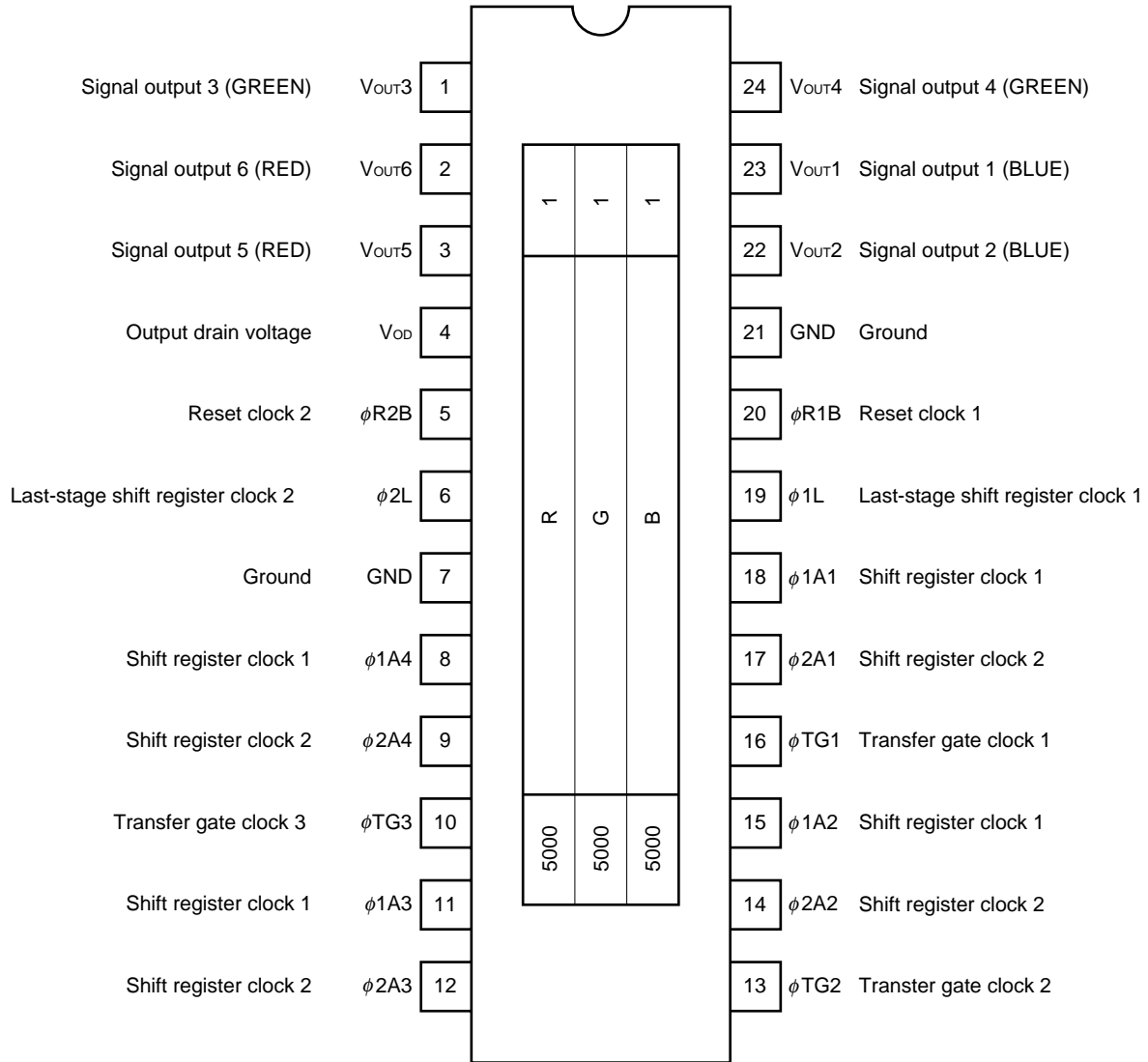
The information in this document is subject to change without notice.

BLOCK DIAGRAM

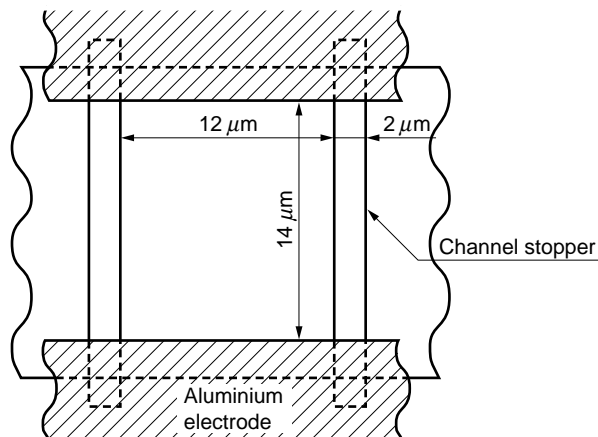


**PIN CONFIGURATIONS (Top View)**

**CCD linear image sensor 24-pin ceramic DIP (600 mil)**



**PHOTOCELL STRUCTURE DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25 °C)**

Parameter	Symbol	Ratings	Unit
Output drain voltage	V <sub>OD</sub>	-0.3 to +15	V
Shift register clock voltage	V <sub>φ1</sub> , V <sub>φ2</sub>	-0.3 to +15	V
Reset signal voltage	V <sub>φR1B</sub> , V <sub>φR2B</sub>	-0.3 to +15	V
Transfer gate signal voltage	V <sub>φTG</sub>	-0.3 to +15	V
Operating ambient temperature	T <sub>A</sub>	-25 to +60	°C
Storage temperature	T <sub>stg</sub>	-40 to +100	°C

**Caution** Exposure to Absolute Maximum Rating for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = +25 °C)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V <sub>OD</sub>	11.4	12.0	12.6	V
Shift register clock signal high level	V <sub>φ1H</sub> , V <sub>φ2H</sub>	4.5	5	5.5	V
Shift register clock signal low level	V <sub>φ1L</sub> , V <sub>φ2L</sub>	-0.3	0	+0.5	V
Reset signal high level	V <sub>φR1BH</sub> , V <sub>φR2BH</sub>	4.5	5	5.5	V
Reset signal low level	V <sub>φR1BL</sub> , V <sub>φR2BL</sub>	-0.3	0	+0.5	V
Transfer gate signal high level	V <sub>φTGH</sub>	4.5	5	5.5	V
Transfer gate signal low level	V <sub>φTGL</sub>	-0.3	0	+0.5	V
Data rate	2 × f <sub>φR1B</sub> , 2 × f <sub>φR2B</sub>	—	2	16	MHz

**Remark** φ1: φ1A1 to φ1A4, φ1L  
 φ2: φ2A1 to φ2A4, φ2L

## ELECTRICAL CHARACTERISTICS

$T_A = +25\text{ }^\circ\text{C}$ ,  $V_{OD} = 12\text{ V}$ ,  $f_{\phi R1B}$ ,  $f_{\phi R2B} = 1\text{ MHz}$ , data rate = 2 MHz, storage time = 10 ms,  
light source: 3200 K halogen lamp +C-500S (infrared cut filter,  $t = 1\text{ mm}$ ), input signal clock = 5  $V_{p-p}$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	$V_{sat}$		1.0	1.3	–	V
Saturation exposure	SER			0.3		$\text{l}\cdot\text{s}$
	SEG			0.3		$\text{l}\cdot\text{s}$
	SEB			0.6		$\text{l}\cdot\text{s}$
Photo response non-uniformity	PRNU	$V_{OUT} = 500\text{ mV}$		$\pm 6$	$\pm 15$	%
Average dark signal	ADS	Light shielding		0.1	5	mV
Dark signal non-uniformity	DSNU	Light shielding	–5	0.5	+5	mV
Power consumption	$P_W$			300	500	mW
Output impedance	$Z_O$			0.5	1	$\text{k}\Omega$
Response	$R_R$		2.71	3.87	5.03	$\text{V}/\text{l}\cdot\text{s}$
	$R_G$		2.66	3.80	4.91	$\text{V}/\text{l}\cdot\text{s}$
	$R_B$		1.45	2.07	2.70	$\text{V}/\text{l}\cdot\text{s}$
Image lag	IL	$V_{OUT} = 500\text{ mV}$		2	5	%
Offset level <sup>Note 1</sup>	$V_{OS}$		4	6	8	V
Output fall delay time <sup>Note 2</sup>	$t_d$		33	40	47	ns
Total transfer efficiency	TTE	$f_{\phi R1B}$ , $f_{\phi R2B} = 8\text{ MHz}$ , data rate = 16 MHz	93.5	98		%
Register imbalance	RI	$V_{OUT} = 500\text{ mV}$	0.0		4.0	%
Red response peak				630		nm
Green response peak				540		nm
Blue response peak				460		nm
Dynamic range	DR	$V_{sat}/\text{DSNU}$		2600		times
Reset feed through noise	RFSN	Light shielding		300	500	mV

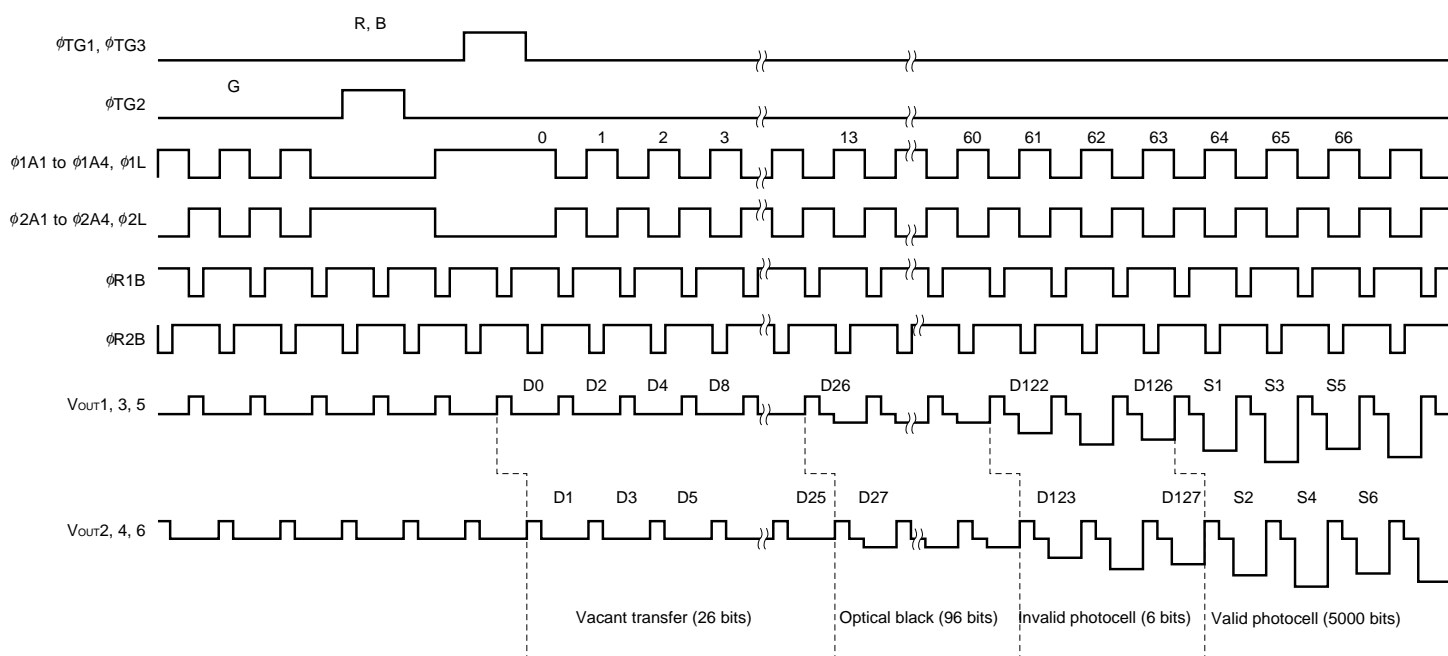
**Notes 1.** Refer to **TIMING CHART 3, 5.**

**2.** Each fall delay time of  $\phi 1L$  and  $\phi 2L$  ( $t_{11}$ ,  $t_{27}$  and  $t_{11}$ ,  $t_{37}$ ) is the TYP. value (refer to **TIMING CHART 3, 5**).

## INPUT PIN CAPACITANCE

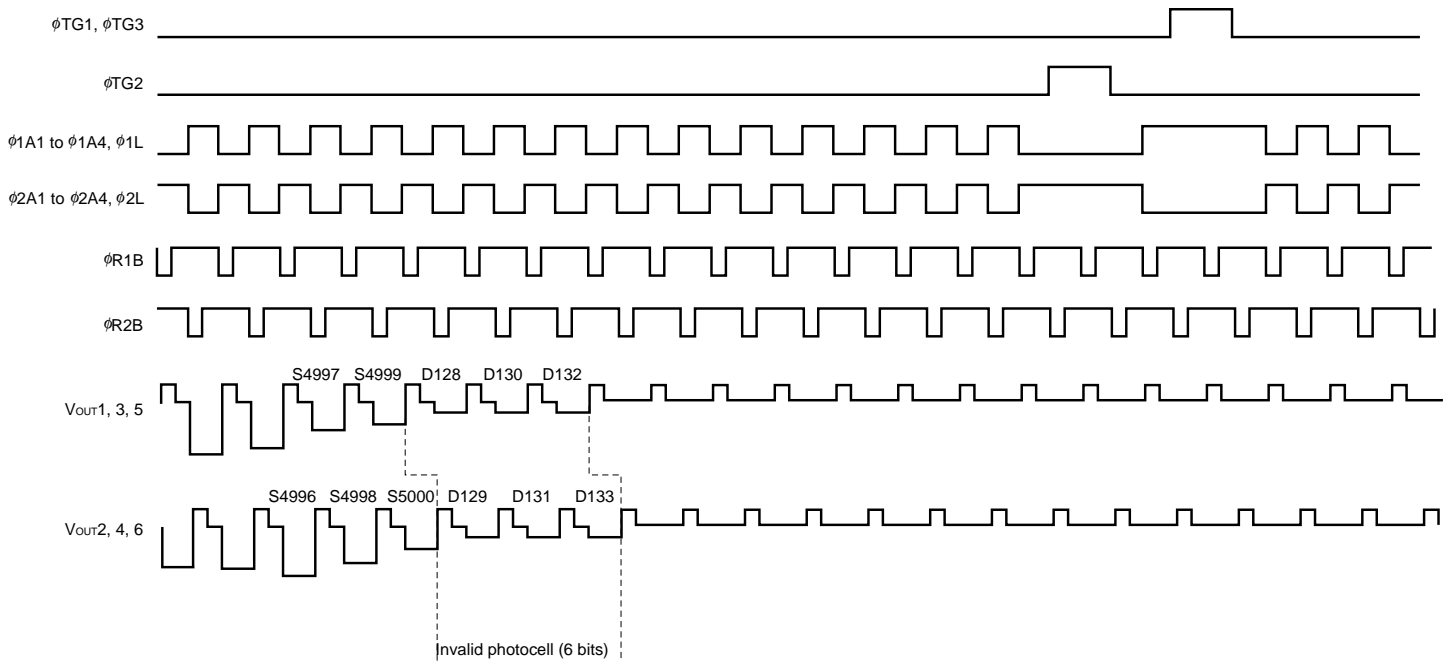
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Transfer gate pin capacitance	$C_{\phi_{TG}}$	$\phi_{TG1}$	16		300	450	pF
		$\phi_{TG2}$	13				
		$\phi_{TG3}$	10				
Reset clock pin capacitance	$C_{\phi_R}$	$\phi_{R1B}$	20		50	80	pF
		$\phi_{R2B}$	5				
Last stage shift register clock pin capacitance	$C_{\phi_L}$	$\phi_{1L}$	19		100	150	pF
		$\phi_{2L}$	6				
Shift register clock pin capacitance A	$C_{\phi_A}$	$\phi_{1A1}$	18		250	380	pF
		$\phi_{1A4}$	8				
		$\phi_{2A1}$	17				
		$\phi_{2A4}$	9				
Shift register clock pin capacitance B	$C_{\phi_B}$	$\phi_{1A2}$	15		500	750	pF
		$\phi_{1A3}$	11				
		$\phi_{2A2}$	14				
		$\phi_{2A3}$	12				

**TIMING CHART 1**



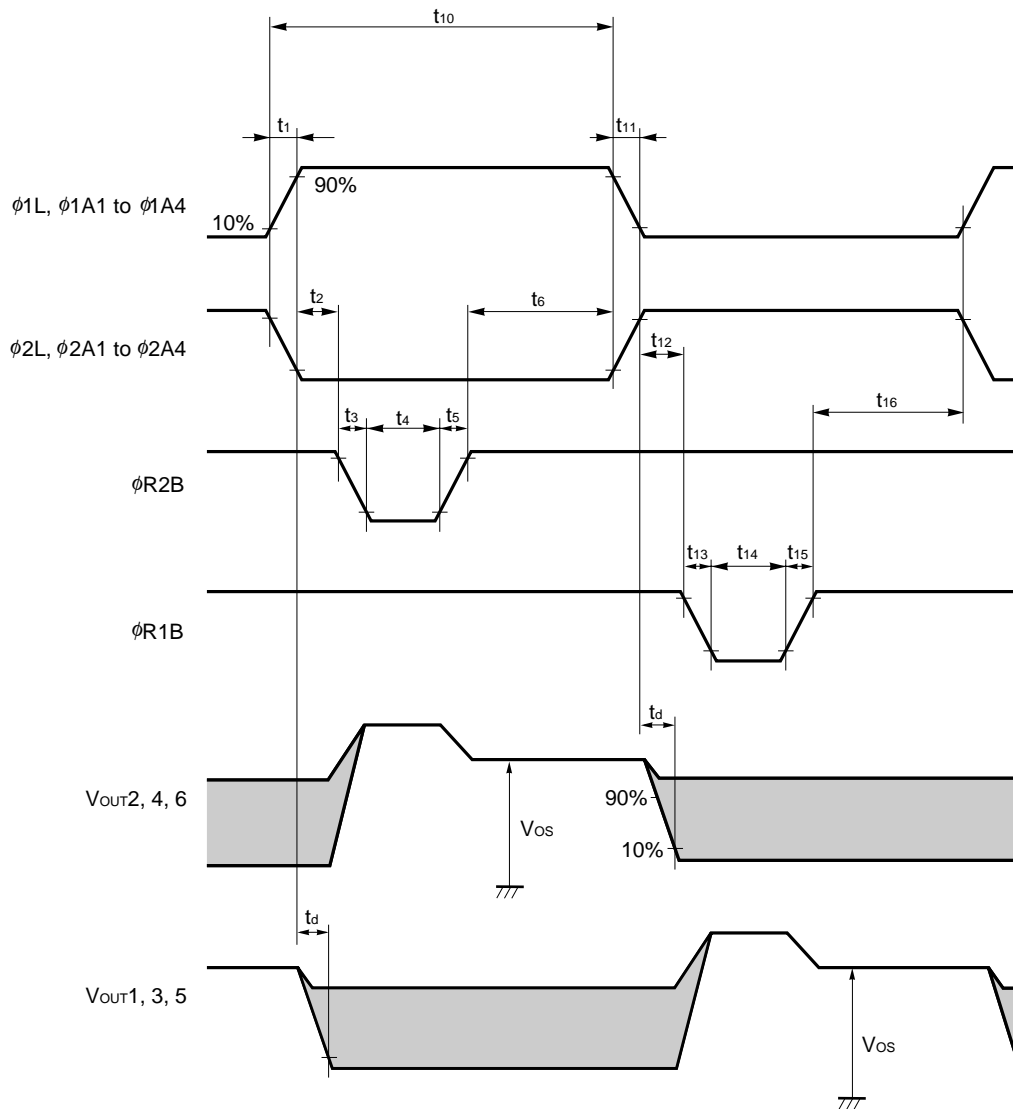
**Caution** Pins 18 ( $\phi 1A1$ ) and 15 ( $\phi 1A2$ ), 11 ( $\phi 1A3$ ) and 8 ( $\phi 1A4$ ) are each connected inside of the device, so do not input different timings to them.  
 And also pins 17 ( $\phi 2A1$ ) and 14 ( $\phi 2A2$ ), 12 ( $\phi 2A3$ ) and 9 ( $\phi 2A4$ ) are each connected inside of the device, so do not input different timings to them (refer to BLOCK DIAGRAM).

## TIMING CHART 2

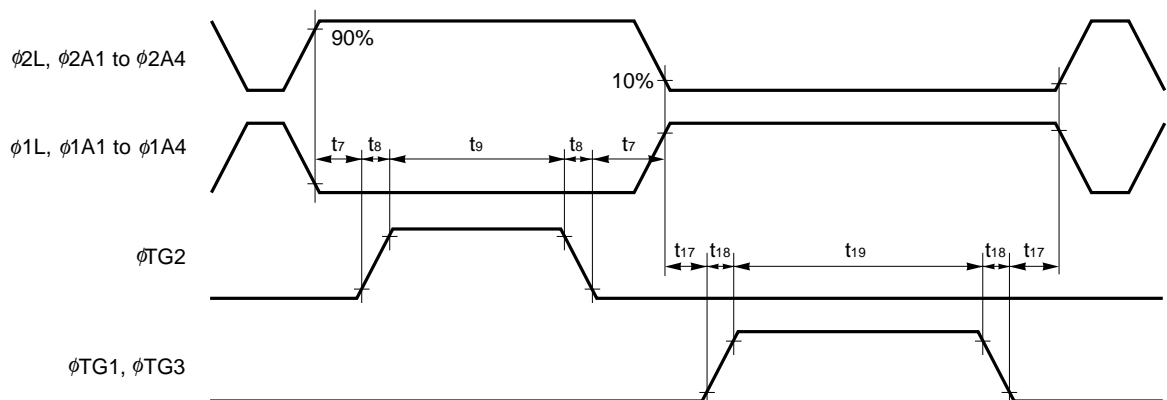




TIMING CHART 3 (Usual speed drive  $f_{\phi R1B}, f_{\phi R2B} = 1$  to 5 MHz)



TIMING CHART 4

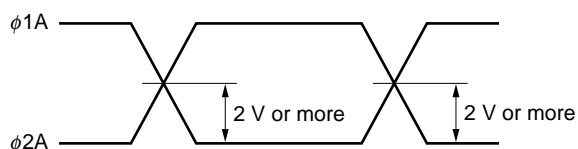


Recommended Timing

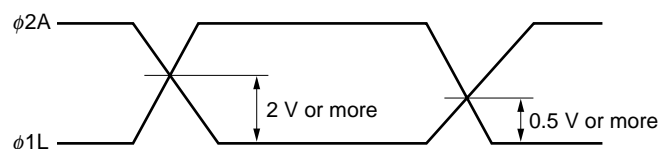
(Unit: ns)

Symbol	MIN.	TYP.	MAX.
t <sub>1</sub> , t <sub>11</sub>	0	10	—
t <sub>2</sub> , t <sub>12</sub>	0	50	—
t <sub>3</sub> , t <sub>5</sub> , t <sub>13</sub> , t <sub>15</sub>	0	5	—
t <sub>4</sub> , t <sub>14</sub>	20	50	—
t <sub>6</sub> , t <sub>16</sub>	20	50	—
t <sub>7</sub> , t <sub>17</sub>	20	50	—
t <sub>8</sub> , t <sub>18</sub>	0	50	—
t <sub>9</sub> , t <sub>19</sub>	1000	2000	—
t <sub>10</sub>	100	500	—

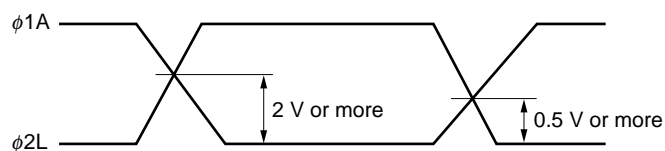
φ1A, φ2A cross points



φ1L, φ2A cross points

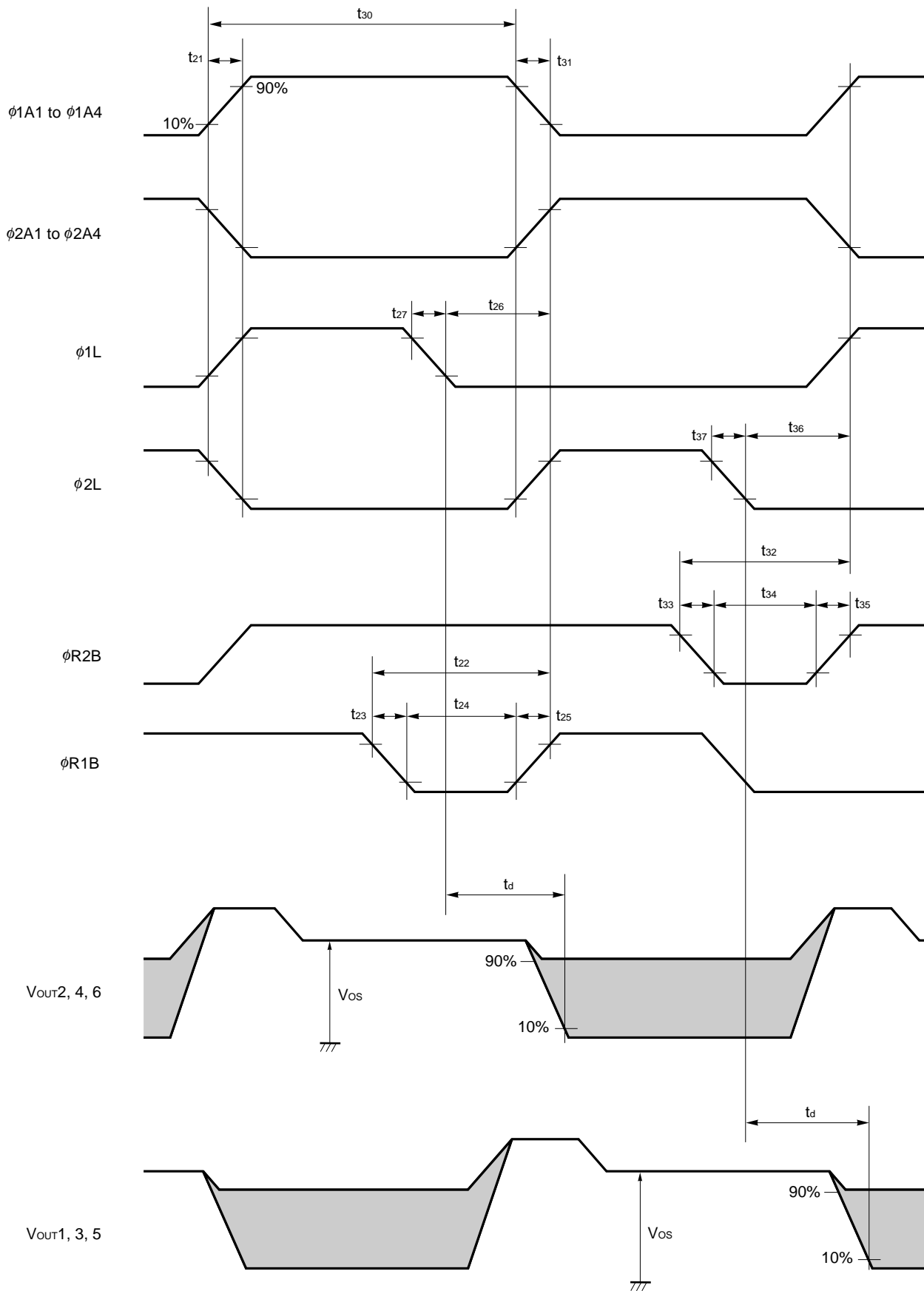


φ1A, φ2L cross points



- Remark 1.** Adjust input resistance of each pin for cross points (φ1A, φ2A), (φ1L, φ2A) and (φ1A, φ2L)
2. φ1A: φ1A1 to φ1A4
  - φ2A: φ2A1 to φ2A4

TIMING CHART5 (High speed drive  $f_{\phi R1B}, f_{\phi R2B} = 5 \text{ to } 8 \text{ MHz}$ )



Recommended Timing (High speed drive  $f_{\phi R1B}, f_{\phi R2B} = 5$  to  $8$  MHz)

(Unit: ns)

Symbol	MIN.	TYP.	MAX.
t <sub>21</sub> , t <sub>31</sub>	0	10	—
t <sub>22</sub> , t <sub>32</sub>	0	30	—
t <sub>23</sub> , t <sub>25</sub> , t <sub>33</sub> , t <sub>35</sub>	0	5	—
t <sub>24</sub> , t <sub>34</sub>	20	t <sub>30</sub> /2	—
t <sub>26</sub> , t <sub>36</sub>	10	20	—
t <sub>27</sub> , t <sub>37</sub>	0	10	—
t <sub>30</sub>	60	100	—

**Caution** When driving  $\mu$ PD3725A according to timing shown in TIMING CHART 3 at high speed, period of signal output is shorten, therefore data may not be sampled normally.

To sample data normally, drive  $\mu$ PD3725A according to timing shown in TIMING CHART 5. To extend the period of signal output, falling edge of last gate shift register clock  $\phi 1L$ ,  $\phi 2L$  should be earlier than that of shift register clock  $\phi 1A$ ,  $\phi 2A$ .

When making the falling edge of  $\phi 1L$ ,  $\phi 2L$  early, output signal is effected by noise from reset clock  $\phi R1B$ ,  $\phi R2B$ . To avoid the effect of this noise, the falling edge of  $\phi R1B$ ,  $\phi R2B$  should be set earlier.

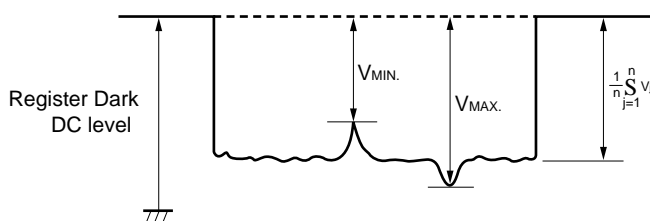
Driving at high speed, drive capability is necessary to be powered up. So design the peripheral circuit referring to peripheral circuit example 2.

**DEFINITIONS OF CHARACTERISTIC ITEMS**

1. Saturation voltage:  $V_{sat}$   
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE  
Product of intensity of illumination (lx) and storage time(s) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU  
The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU(\%) = \left( \frac{V_{MAX. \text{ or } V_{MIN.}}}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right) \times 100$$

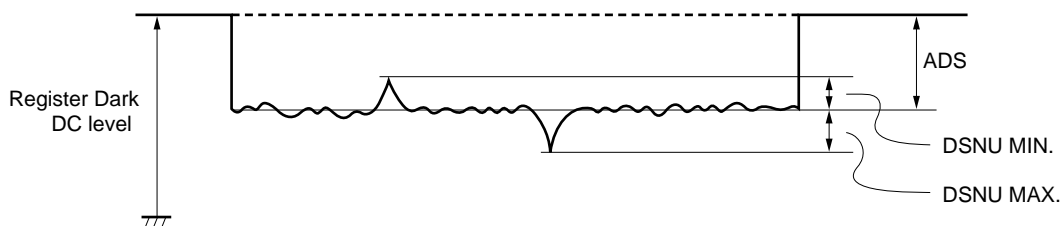
n: Number of valid bits  
V<sub>j</sub>: Output voltage of each bit



4. Average dark signal: ADS  
Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n} \sum_{j=1}^n V_j$$

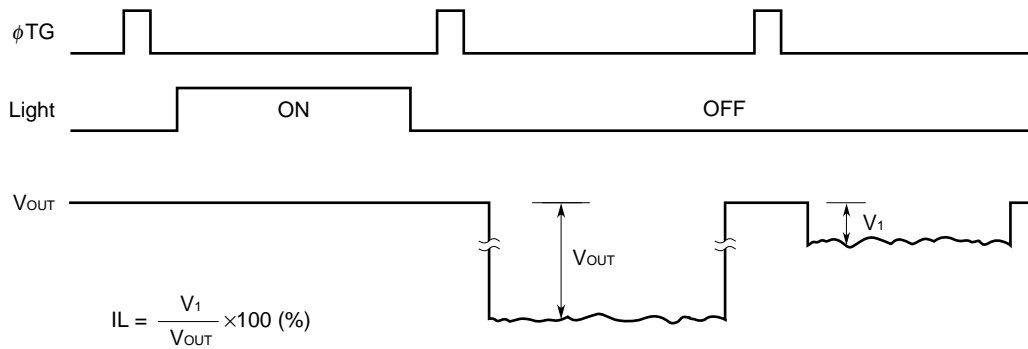
5. Dark signal non-uniformity: DSNU  
The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance:  $Z_o$   
Output pin impedance viewed from outside.
7. Response: R  
Output voltage divided by exposure (lx•s).  
Note that the response varies with a light source.

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.

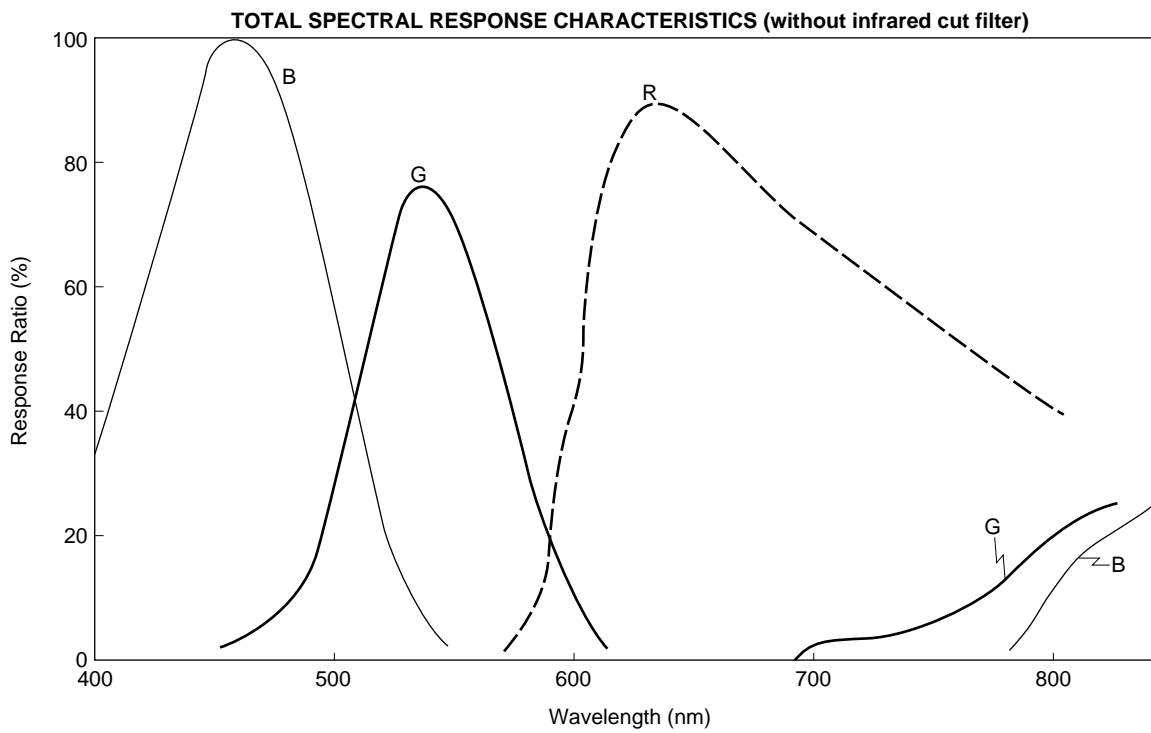
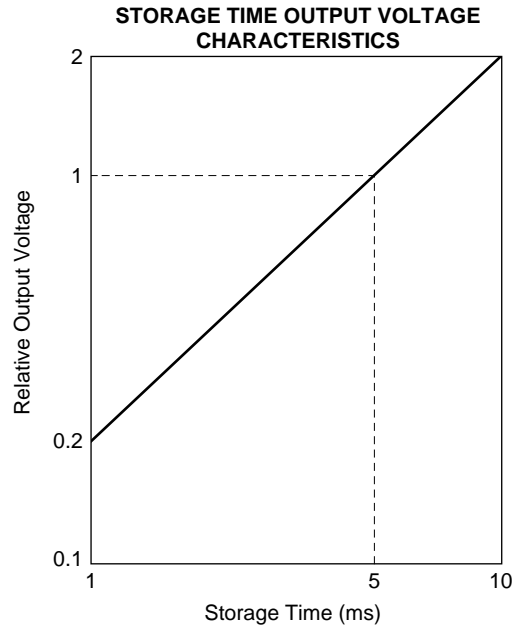
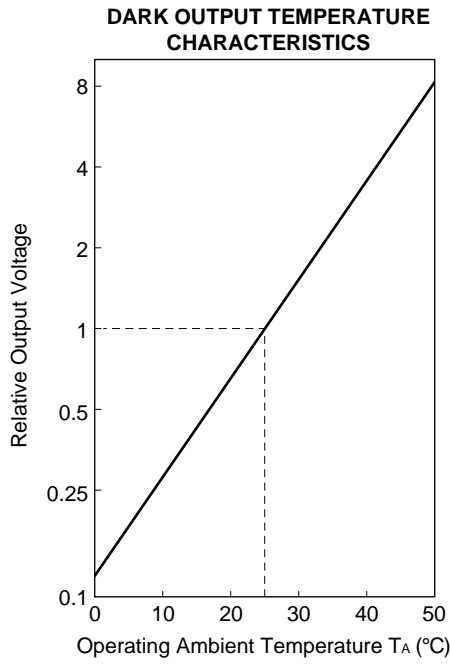


9. Register Imbalance: RI

The rate of the difference between the averages of the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

$$RI = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100 (\%)$$

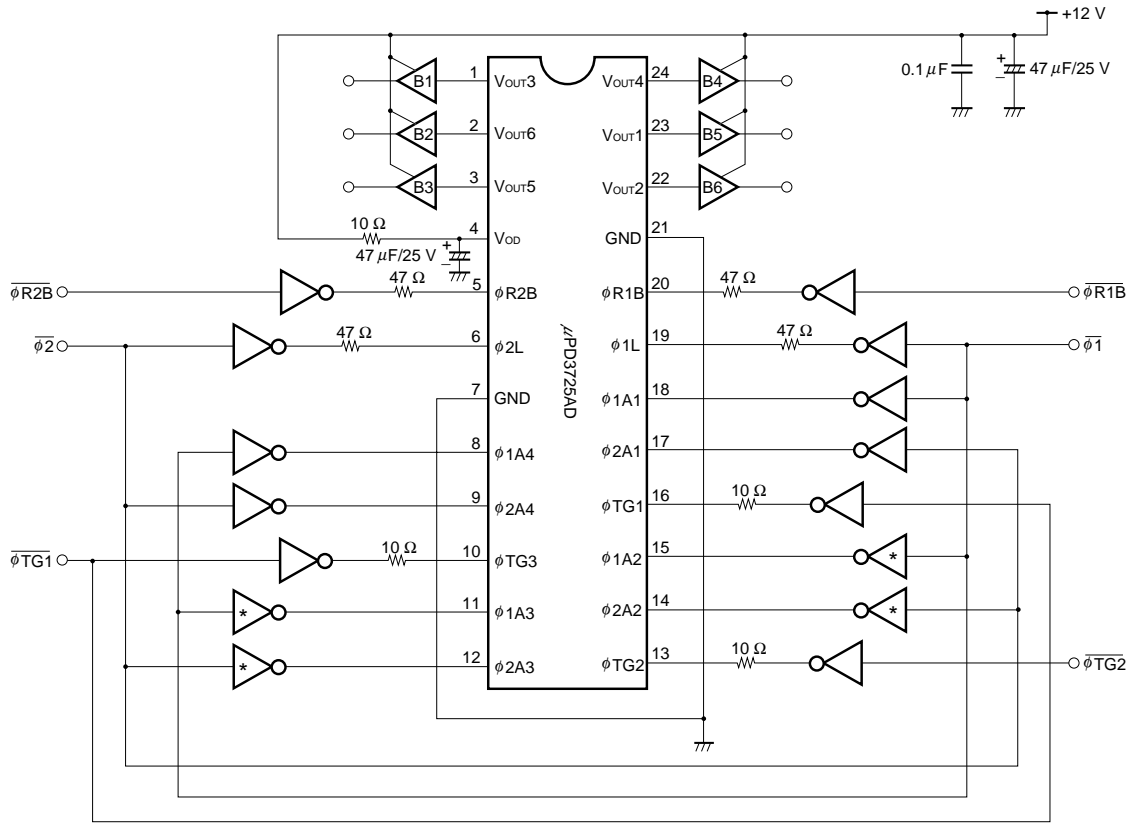
STANDARD CHARACTERISTIC CURVES (T<sub>A</sub> = +25 °C)







PERIPHERAL CIRCUIT EXAMPLE 2 (For high speed drive)

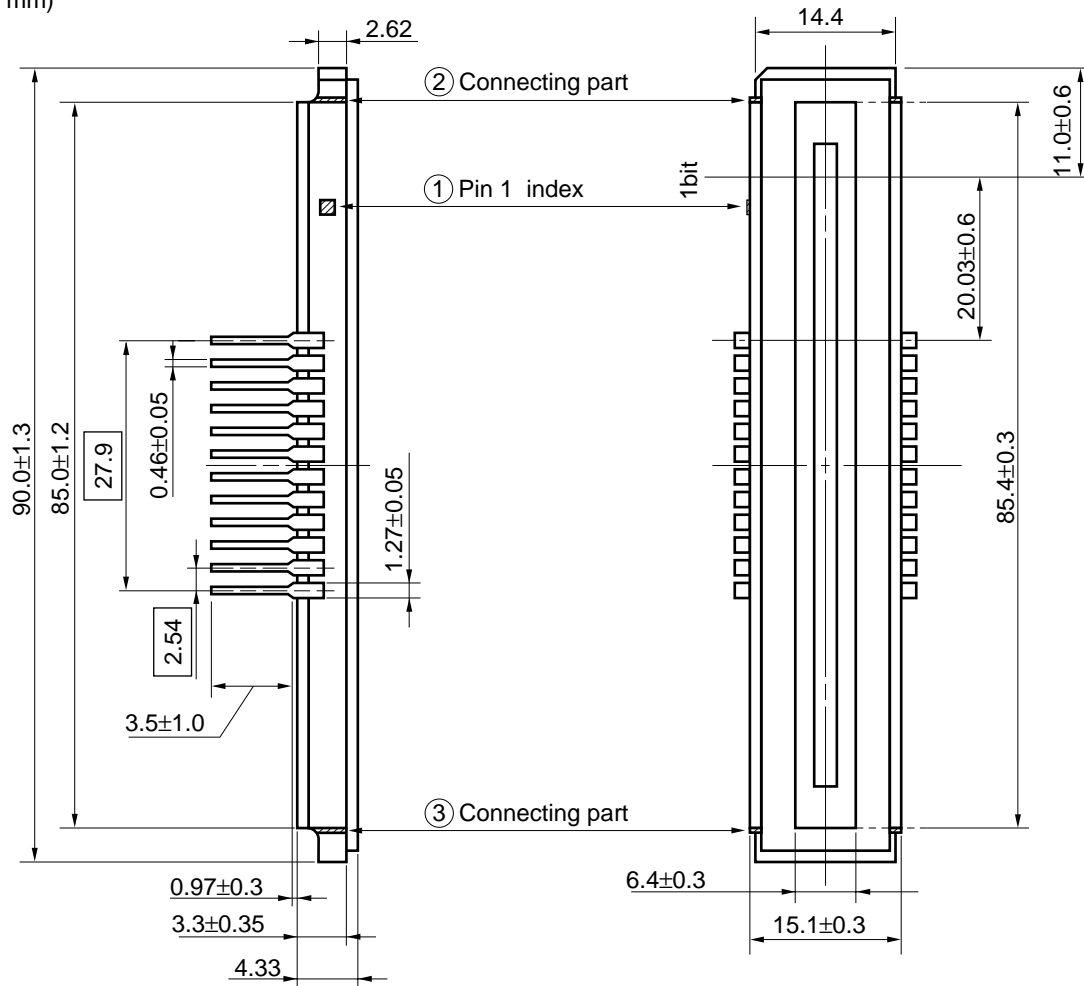


- Remarks**
1. Inverters: 74AC04
  2. For \* inverter, use high speed inverter which has double driving capability of 74AC04

PACKAGE DIMENSIONS (Unit: mm)

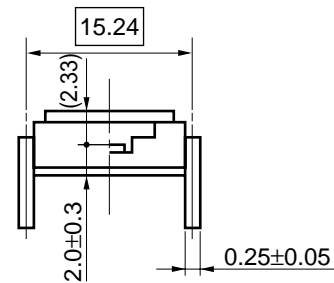
CCD LINEAR IMAGE SENSOR 24PIN CERAMIC DIP (600 mil)

(Unit : mm)



NOTE

① pin 1 index and ②, ③ connecting parts are made of silver wax and plated with gold. As they are electrically connected with GND, be sure not to touch with other wirings on the board.



Name	Dimensions	Refractive index
Glass cap	89.0 × 13.6 × 1.0	1.5

24D-1CCD-PKG-2

**RECOMMENDED SOLDERING CONDITIONS**

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document “**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL**” (C10535E).

**Type of Through Hole Device**

$\mu$ PD3725AD : CCD linear image sensor 24-pin ceramic DIP (600 mil)

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial heating method	Pin temperature: 260 °C or below, Heat time: 10 seconds or less (Per each lead).

**Caution** For through hole devices, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**[MEMO]**

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

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NEC devices are classified into the following three quality grades:

“Standard”, “Special”, and “Specific”. The Specific quality grade applies only to devices developed based on a customer designated “quality assurance program” for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices in “Standard” unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.

M4 94.11