

March 1997

Features

- Fully Static Operation
- Industry Standard 1024 x 4 Pinout (Same as Pinouts for 6514, 2114, 9114, and 4045 Types)
- Common Data Input and Output
- Memory Retention for Standby Battery Voltage as Low as 2V Min
- All Inputs and Outputs Directly TTL Compatible
- Three-State Outputs
- Low Standby and Operating Power

Description

The MWS5114 is a 1024 word by 4-bit static random access memory that uses the ion-implanted silicon gate complementary MOS (CMOS) technology. It is designed for use in memory systems where low power and simplicity in use are desirable. This type has common data input and data output and utilizes a single power supply of 4.5V to 6.5V.

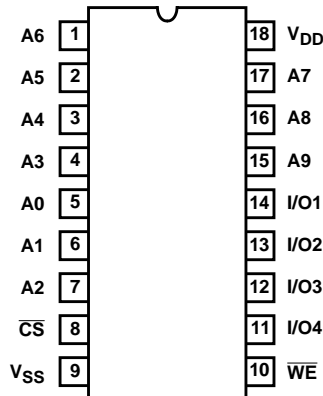
The MWS5114 is supplied in 18 lead, hermetic, dual-in-line sidebraced ceramic packages (D suffix) and in 18 lead dual-in-line plastic packages (E suffix).

Ordering Information

| 200ns | 250ns | 300ns | TEMPERATURE RANGE | PACKAGE | PKG. NO. |
|-------------------------|-------------------------|-----------|-------------------|------------------|----------------|
| MWS5114E3 | MWS5114E2 MWS5114E2X | MWS5114E1 | 0°C to +70°C | PDIP Burn-In | E18.3 E18.3 |
| MWS5114D3 MWS5114D3X | MWS5114D2 | MWS5114D1 | 0°C to +70°C | SBDIP Burn-In | D18.3 D18.3 |

Pinout

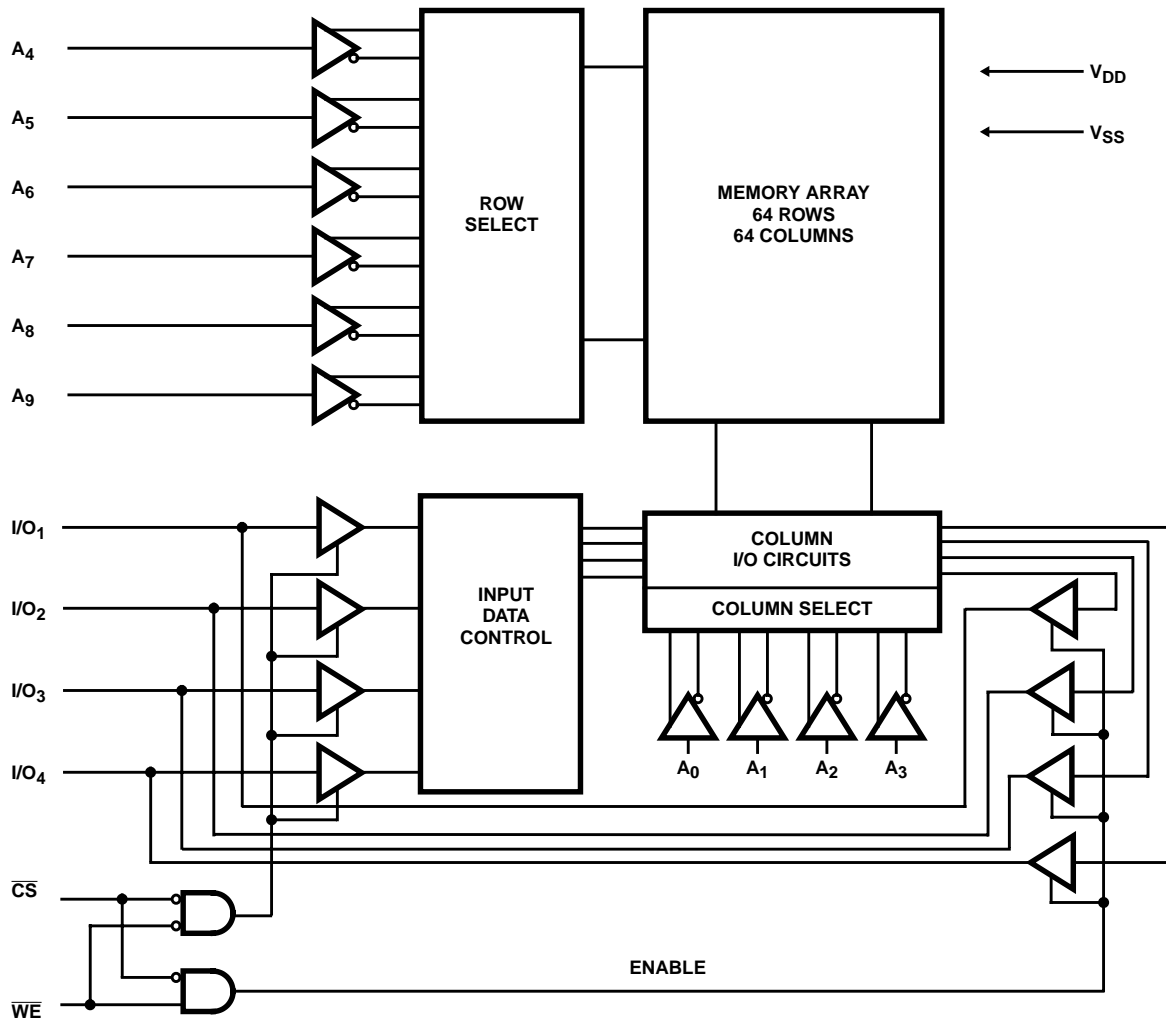
**MWS5114
(PDIP, SBDIP)
TOP VIEW**



OPERATIONAL MODES

| FUNCTION | CS | WE | DATA PINS |
|--------------|----|----|---------------------------|
| Read | 0 | 1 | Output: Dependent on data |
| Write | 0 | 0 | Input |
| Not Selected | 1 | X | High Impedance |

Functional Block Diagram



MWS5114

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
 (All Voltages Referenced to V_{SS} Terminal) -0.5V to +7V
 Input Voltage Range, All Inputs -0.5V to $V_{DD} + 0.5V$
 DC Input Current, Any One Input. $\pm 10mA$

Thermal Information

Thermal Resistance (Typical) θ_{JA} ($^{\circ}C/W$) θ_{JC} ($^{\circ}C/W$)
 Plastic DIP Package 75 N/A
 SBDIP Package 75 20
 Operating Temperature Range (T_A)
 Package Type D $-55^{\circ}C$ to $+125^{\circ}C$
 Package Type E $-40^{\circ}C$ to $+85^{\circ}C$
 Maximum Storage Temperature Range (T_{STG}) $-65^{\circ}C$ to $+150^{\circ}C$
 Maximum Junction Temperature
 Ceramic Package $+175^{\circ}C$
 Plastic Package $+150^{\circ}C$
 Maximum Lead Temperature. $+265^{\circ}C$

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

| PARAMETER | LIMITS | | UNITS |
|----------------------------|-----------|----------|-------|
| | ALL TYPES | | |
| | MIN | MAX | |
| DC Operating Voltage Range | 4.5 | 6.5 | V |
| Input Voltage Range | V_{SS} | V_{DD} | V |

Static Electrical Specifications

At $T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{DD} = \pm 5\%$, Except as Noted

| PARAMETER | SYMBOL | CONDITIONS | | | LIMITS | | | | | | | | | UNITS |
|--------------------------------|----------|--------------|-----------------|-----------------|-----------|-----------------|---------|-----------|-----------------|---------|-----------|-----------------|---------|---------|
| | | V_O (V) | V_{IN} (V) | V_{DD} (V) | MWS5114-3 | | | MWS5114-2 | | | MWS5114-1 | | | |
| | | | | | MIN | (NOTE 1) TYP | MAX | MIN | (NOTE 1) TYP | MAX | MIN | (NOTE 1) TYP | MAX | |
| Quiescent Device Current | IDD | - | 0, 5 | 5 | - | 75 | 100 | - | 75 | 100 | - | 75 | 250 | μA |
| Output Low (Sink) Current | I_{OL} | 0.4 | 0, 5 | 5 | 2 | 4 | - | 2 | 4 | - | 2 | 4 | - | mA |
| Output High (Source) Current | I_{OH} | 4.6 | 0, 5 | 5 | -0.4 | -1 | - | -0.4 | -1 | - | -0.4 | -1 | - | mA |
| Output Voltage Low-Level | VOL | - | 0, 5 | 5 | - | 0 | 0.1 | - | 0 | 0.1 | - | 0 | 0.1 | V |
| Output Voltage High-Level | VOH | - | 0, 5 | 5 | 4.9 | 5 | - | 4.9 | 5 | - | 4.9 | 5 | - | V |
| Input Low Voltage | V_{IL} | 0.5, 4.5 | - | 5 | - | 1.2 | 0.8 | - | 1.2 | 0.8 | - | 1.2 | 0.8 | V |
| Input High Voltage | V_{IH} | 0.5, 4.5 | - | 5 | 2.4 | - | - | 2.4 | - | - | 2.4 | - | - | V |
| Input Leakage Current (Note 2) | IIN | - | 0, 5 | 5 | - | ± 0.1 | ± 5 | - | ± 0.1 | ± 5 | - | ± 0.1 | ± 5 | μA |
| Operating Current (Note 3) | IDD1 | - | 0, 5 | 5 | - | 4 | 8 | - | 4 | 8 | - | 4 | 8 | mA |

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Static Electrical Specifications At $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{DD} = \pm 5\%$, Except as Noted (Continued)

| PARAMETER | SYMBOL | CONDITIONS | | | LIMITS | | | | | | | | | UNITS |
|---|-----------|--------------|-----------------|-----------------|-----------|-----------------|---------|-----------|-----------------|---------|-----------|-----------------|---------|---------------|
| | | V_O (V) | V_{IN} (V) | V_{DD} (V) | MWS5114-3 | | | MWS5114-2 | | | MWS5114-1 | | | |
| | | | | | MIN | (NOTE 1) TYP | MAX | MIN | (NOTE 1) TYP | MAX | MIN | (NOTE 1) TYP | MAX | |
| Three-State Output Leakage Current (Note 4) | I_{OUT} | 0, 5 | 0, 5 | 5 | - | ± 0.5 | ± 5 | - | ± 0.5 | ± 5 | - | ± 0.5 | ± 5 | μA |
| Input Capacitance | C_{IN} | - | - | - | - | 5 | 7.5 | - | 5 | 7.5 | - | 5 | 7.5 | pF |
| Output Capacitance | C_{OUT} | - | - | - | - | 10 | 15 | - | 10 | 15 | - | 10 | 15 | pF |

NOTES:

1. Typical values are for $T_A = 25^{\circ}\text{C}$ and nominal V_{DD} .
2. All inputs in parallel.
3. Outputs open circuited; cycle time = $1\mu\text{s}$.
4. All outputs in parallel.

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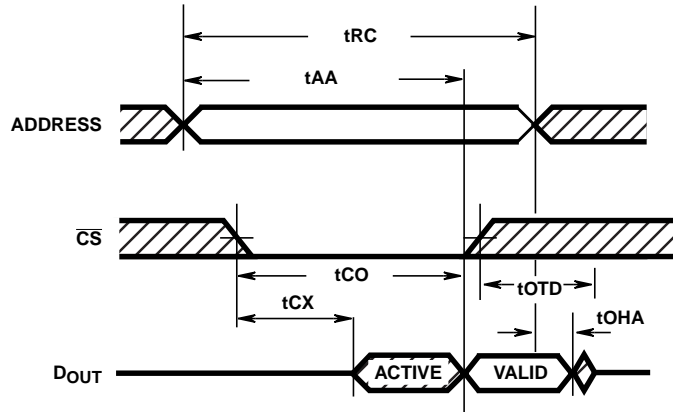
Dynamic Electrical Specifications at $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$, Input $t_R, t_F = 10\text{ns}$; $C_L = 50\text{pF}$ and 1 TTL Load

| PARAMETER | SYMBOL | LIMITS | | | | | | | | | UNITS |
|-------------------------------------|------------------|-----------------|-----------------|-----|-----------------|-----------------|-----|-----------------|-----------------|-----|-------|
| | | MWS5114-3 | | | MWS5114-2 | | | MWS5114-1 | | | |
| | | (NOTE 1) MIN | (NOTE 2) TYP | MAX | (NOTE 1) MIN | (NOTE 2) TYP | MAX | (NOTE 1) MIN | (NOTE 2) TYP | MAX | |
| READ CYCLE TIMES (FIGURE 1) | | | | | | | | | | | |
| Read Cycle | t _{RC} | 200 | 160 | - | 250 | 200 | - | 300 | 250 | - | ns |
| Access from Address | t _{AA} | - | 160 | 200 | - | 200 | 250 | - | 250 | 300 | ns |
| Chip Selection to Output Valid | t _{CO} | - | 110 | 150 | - | 150 | 200 | - | 200 | 250 | ns |
| Chip Selection to Output Active | t _{CX} | 20 | 100 | - | 20 | 100 | - | 20 | 100 | - | ns |
| Output Three-State from Deselection | t _{OTD} | - | 75 | 125 | - | 75 | 125 | - | 75 | 125 | ns |
| Output Hold from Address Change | t _{OHA} | 50 | 100 | - | 50 | 100 | - | 50 | 100 | - | ns |
| WRITE CYCLE TIMES (FIGURE 2) | | | | | | | | | | | |
| Write Cycle | t _{WC} | 200 | 160 | - | 250 | 200 | - | 300 | 220 | - | ns |
| Write | t _W | 125 | 100 | - | 150 | 120 | - | 200 | 140 | - | ns |
| Write Release | t _{WR} | 50 | 40 | - | 50 | 40 | - | 50 | 40 | - | ns |
| Address to Chip Select Setup Time | t _{ACS} | 0 | 0 | - | 0 | 0 | - | 0 | 0 | - | ns |
| Address to Write Setup Time | t _{AW} | 25 | 20 | - | 50 | 40 | - | 50 | 40 | - | ns |
| Data to Write Setup Time | t _{DSU} | 75 | 50 | - | 75 | 50 | - | 75 | 50 | - | ns |
| Data Hold from Write | t _{DH} | 30 | 10 | - | 30 | 10 | - | 30 | 10 | - | ns |

NOTES:

1. Time required by a limit device to allow for the indicated function.
2. Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

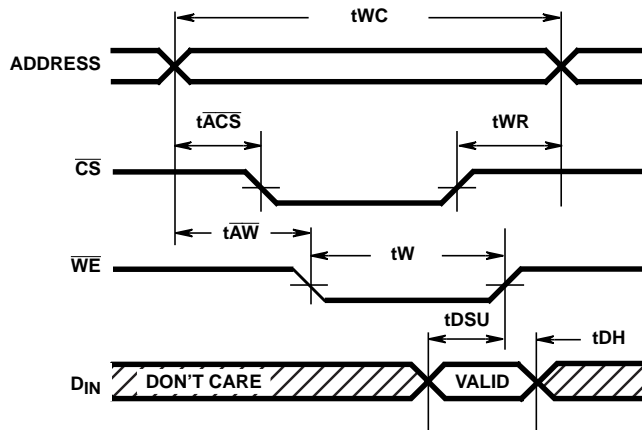
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NOTE:

1. \overline{WE} is high during the Read Cycle. Timing measurement reference level is 1.5V.

FIGURE 1. READ CYCLE TIMING WAVEFORMS



NOTE:

1. \overline{WE} is low during the Write Cycle. Timing measurement reference level is 1.5V.

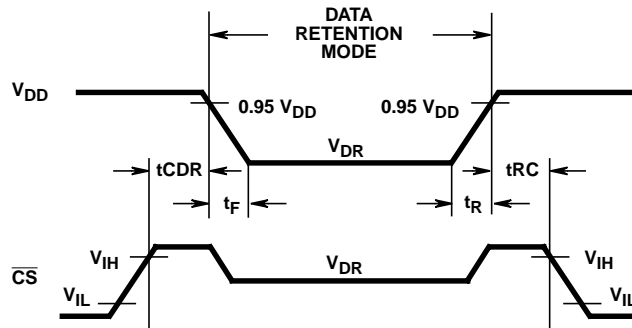
FIGURE 2. WRITE CYCLE TIMING WAVEFORMS

Data Retention Specifications at $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; See Figure 3

| PARAMETER | SYMBOL | TEST CONDITIONS | | LIMITS | | | UNITS | |
|---|------------|-----------------|--------------|-----------|--------------|-----|---------------|---------------|
| | | V_{DR} (V) | V_{DD} (V) | ALL TYPES | | | | |
| | | | | MIN | (NOTE 1) TYP | MAX | | |
| Minimum Data Retention Voltage | VDR | - | - | 2 | - | - | V | |
| Data Retention Quiescent Current | MWS5114-3 | IDD | 2 | - | - | 25 | 50 | μA |
| | MWS5114-2 | | 2 | - | - | 25 | 50 | μA |
| | MWS5114-1 | | 2 | - | - | 60 | 125 | μA |
| Chip Deselect to Data Retention Time | tCDR | - | 5 | 300 | - | - | ns | |
| Recovery to Normal Operation Time | tRC | - | 5 | 300 | - | - | ns | |
| V_{DD} to V_{DR} Rise and Fall Time | t_R, t_F | 2 | 5 | 1 | - | - | μs | |

NOTE:

1. Typical Values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

FIGURE 3. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

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