SONY

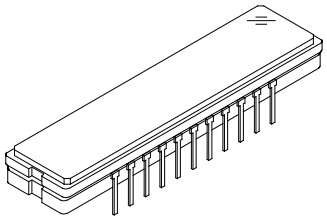
ILX511

2048-pixel CCD Linear Image Sensor (B/W)

Description

The ILX511 is a rectangular reduction type CCD linear image sensor designed for bar code POS hand scanner and optical measuring equipment use. A built-in timing generator and clock-drivers ensure single 5 V power supply for easy use.

22 pin DIP (Plastic)



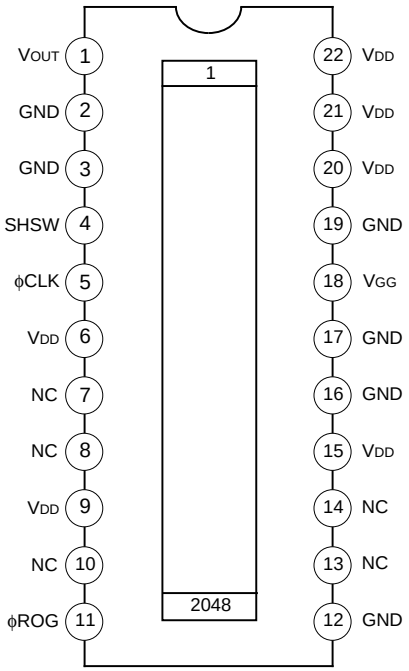
Features

- Number of effective pixels: 2048 pixels
- Pixel size: 14 µm × 200 µm (14 µm pitch)
- Single 5 V power supply
- Ultra-high sensitivity
- Built-in timing generator and clock-drivers
- Built-in sample-and-hold circuit
- Maximum clock frequency: 2MHz

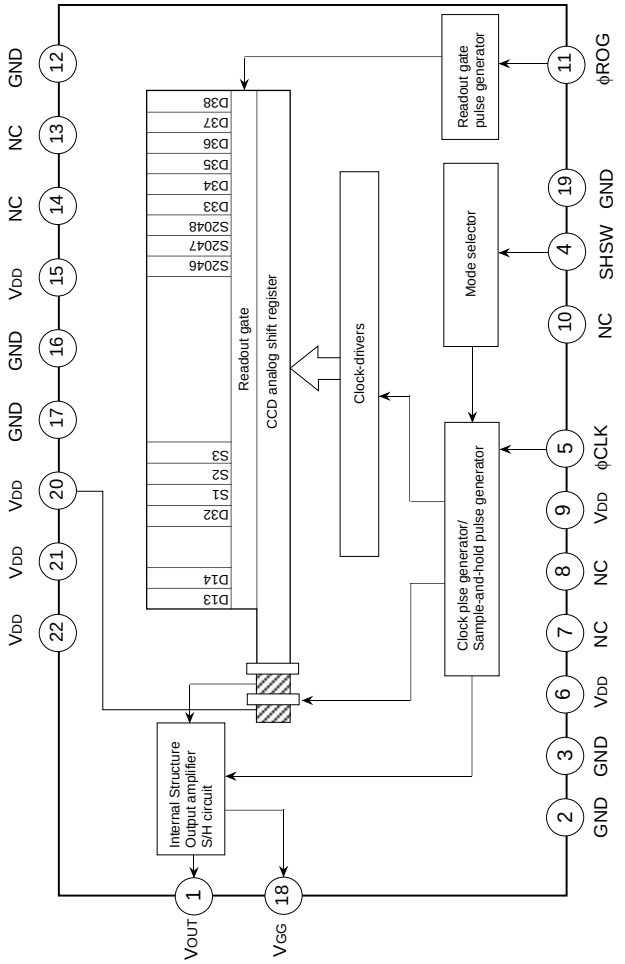
Absolute Maximum Ratings

• Supply voltage	V_{DD}	6	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



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E94108-TE

Pin Description

Pin No.	Symbol	Description
1	V_{OUT}	Signal output
2	GND	GND
3	GND	GND
4	SHSW	Switch (with S/H or without S/H)
5	ϕCLK	Clock pulse input
6	V_{DD}	5V power supply
7	NC	NC
8	NC	NC
9	V_{DD}	5V power supply
10	NC	NC
11	ϕROG	Readout gate pulse input
12	GND	GND
13	NC	NC
14	NC	NC
15	V_{DD}	5V power supply
16	GND	GND
17	GND	GND
18	V_{GG}	Output circuit gate bias
19	GND	GND
20	V_{DD}	5V power supply
21	V_{DD}	5V power supply
22	V_{DD}	5V power supply

Mode Description

Mode in Use	Pin 4 (SHSW)
With S/H	GND
Without S/H	V_{DD}

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	4.5	5.0	5.5	V

Input Clock Voltage Condition (Note)

Item	Min.	Typ.	Max.	Unit
V_{IH}	4.5	5.0	5.5	V
V_{IL}	0	—	0.5	V

Note) This is applied to the all pulses applied externally. (ϕCLK, ϕROG)

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕCLK pin	$C_{\phi CLK}$	—	10	—	pF

Electro-optical Characteristics

(Ta = 25 °C, V_{DD} = 5 V, Clock frequency: 1 MHz, Light source = 3200 K, IR cut filter: CM-500S (t = 1.0 mm), Without S/H mode)

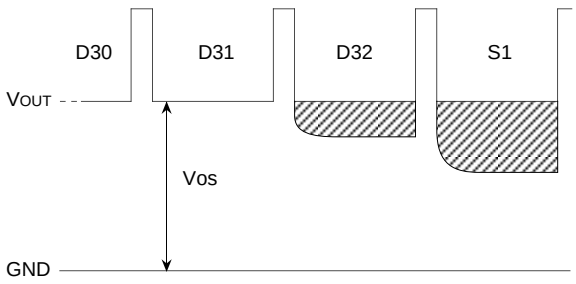
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	150	200	250	V/(lx • s)	Note 1
Sensitivity 2	R2	—	1800	—	V/(lx • s)	Note 2
Sensitivity nonuniformity	PRNU	—	5.0	10.0	%	Note 3
Saturation output voltage	V_{SAT}	0.6	0.8	—	V	—
Dark voltage average	V_{DRK}	—	3.0	6.0	mV	Note 4
Dark signal nonuniformity	DSNU	—	6.0	12.0	mV	Note 4
Image lag	IL	—	1	—	%	Note 5
Dynamic range	DR	—	267	—	—	Note 6
Saturation exposure	SE	—	0.004	—	lx • s	Note 7
5 V current consumption	I_{VDD}	—	5.0	10.0	mA	—
Total transfer efficiency	TTE	92.0	98.0	—	%	—
Output impedance	Z_O	—	250	—	Ω	—
Offset level	V_{OS}	—	2.8	—	V	Note 8

Note)

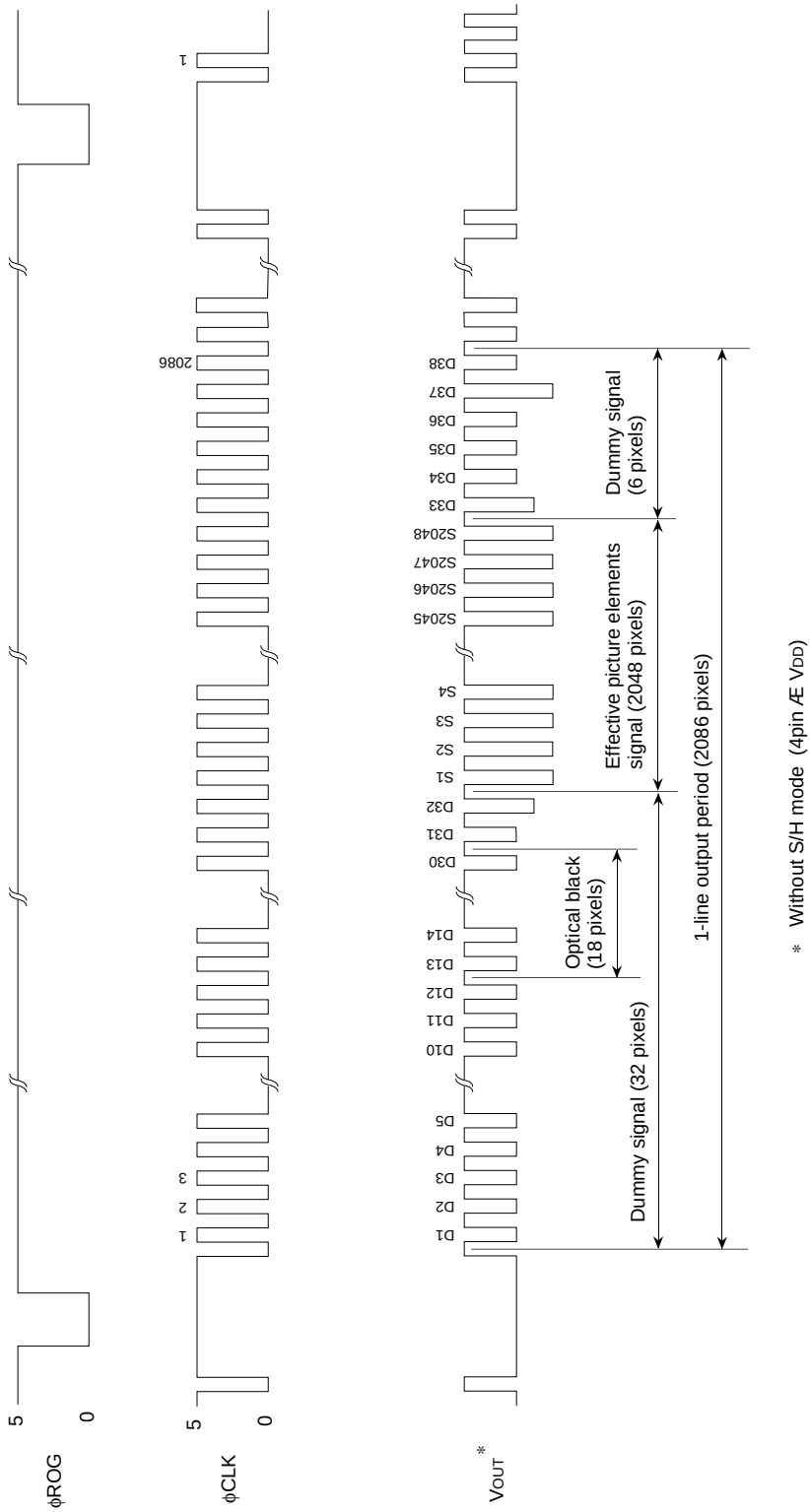
1. For the sensitivity test light is applied with a uniform intensity of illumination.
2. Light source: LED λ = 660nm
3. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

$$PRNU = \frac{(V_{MAX}-V_{MIN})/2}{V_{AVE}} \times 100\ (\%)$$

   The maximum output of all the valid pixels is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
4. Integration time is 10ms.
5. Typical value is used for clock pulse and readout pulse. V_{OUT} = 500 mV.
6. DR = V_{SAT}/V_{DRK}. When optical integration time is shorter, the dynamic range sets wider because dark voltage is in proportion to optical integration time.
7. SE = $V_{SAT}/R1$
8. Vos is defined as indicated below.



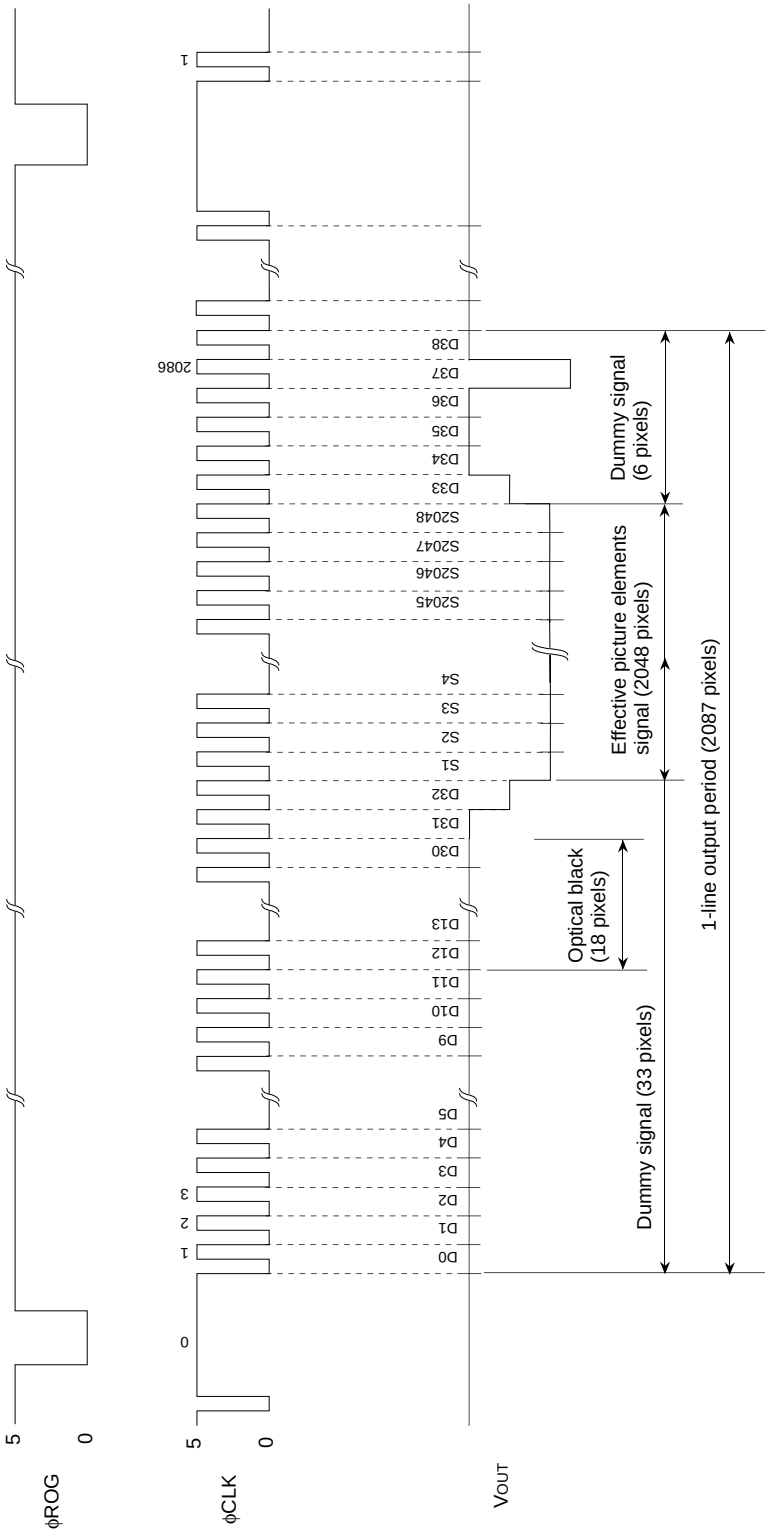
Clock Timing Diagram (Without S/H mode)



* Without S/H mode (4pin Æ VDD)

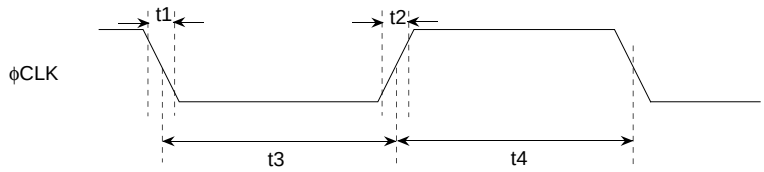
2088 or more clock pulses are required.

Clock Timing Diagram (With S/H mode)



2088 or more clock pulses are required.

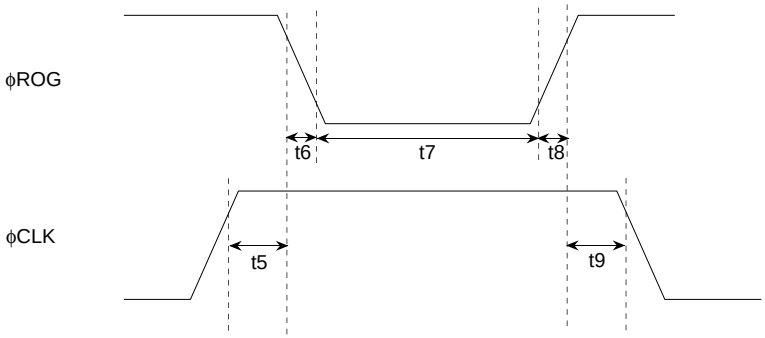
ϕ CLK Timing (For all modes)



Item	Symbol	Min.	Typ.	Max.	Unit
ϕ CLK pulse rise/fall time	t1, t2	0	10	100	ns
ϕ CLK pulse duty (Note 1)	—	40	50	60	%

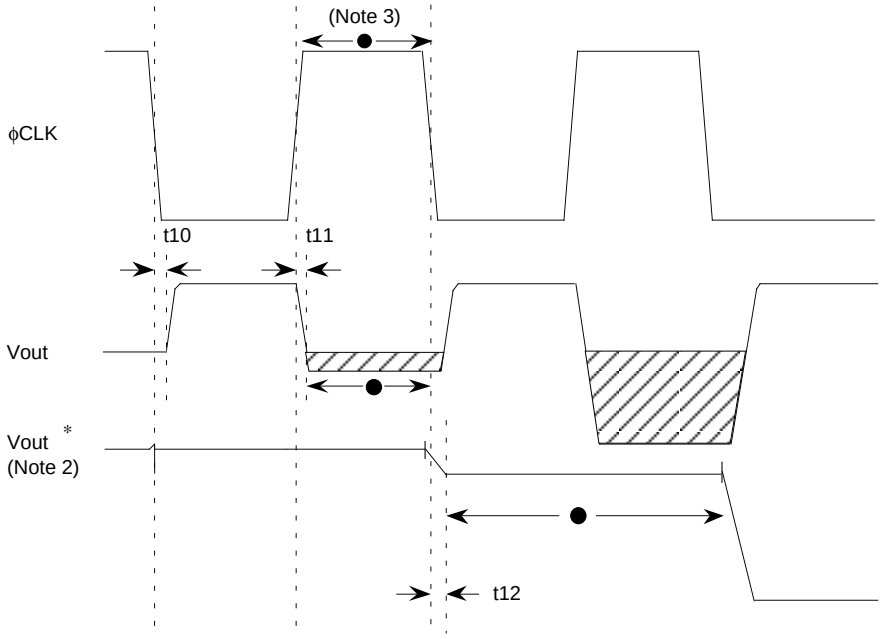
Note 1) $100 \times t4 / (t3 + t4)$

ϕ ROG, ϕ CLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
ϕ ROG, ϕ CLK pulse timing 1	t5	0	3000	—	ns
ϕ ROG, ϕ CLK pulse timing 2	t9	1000	3000	—	
ϕ ROG pulse rise/fall time	t6, t8	0	10	—	
ϕ ROG pulse period	t7	3000	5000	—	

ϕCLK, VOUT Timing (Note 1)



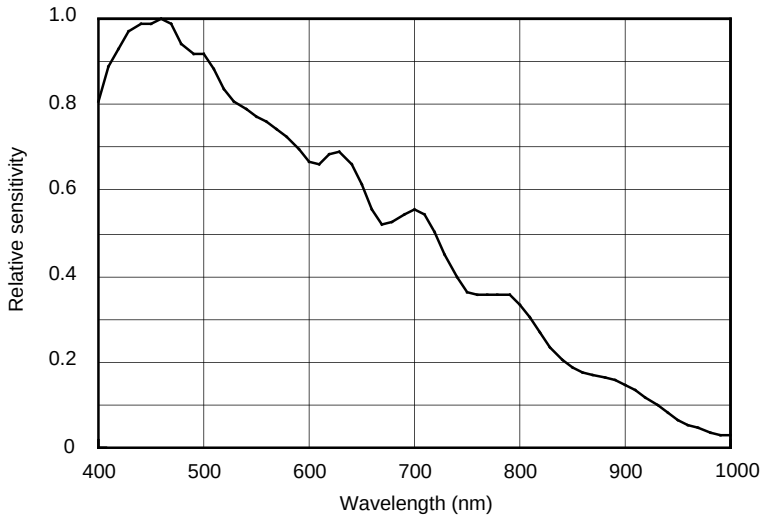
Item	Symbol	Min.	Typ.	Max.	Unit
ϕCLK-VOUT 1	t10	40	115	280	ns
ϕCLK-VOUT 2	t11	55	120	205	
ϕCLK-VOUT* (with S/H)	t12	10	165	240	

Note 1) fck = 1MHz, ϕCLK pulse duty = 50 %, ϕCLK pulse rise/fall time = 10 ns

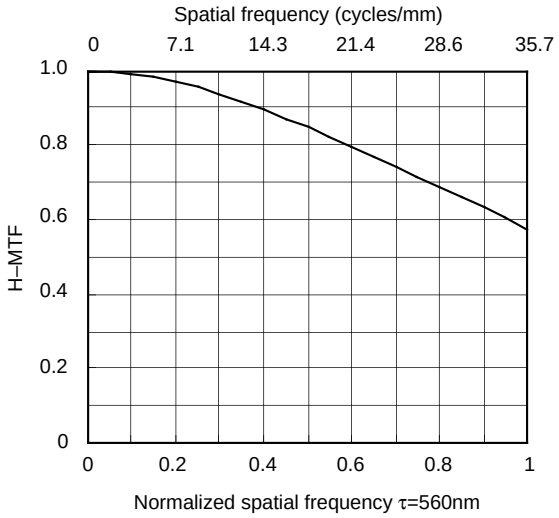
Note 2) Output waveform when internal S/H is in use.

Note 3) ● indicates the correspondence of clock pulse and data period.

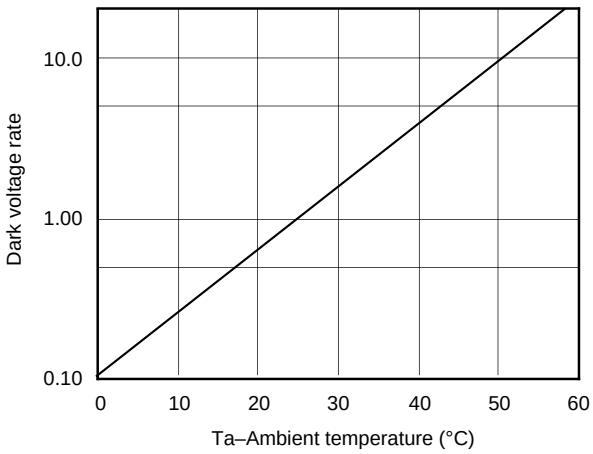
Spectral sensitivity (Typ.) (Ta = 25°C)



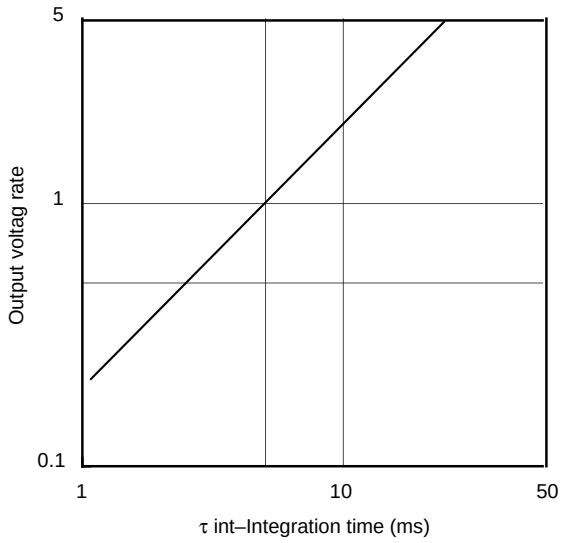
MTF of main scanning direction (Typ.)



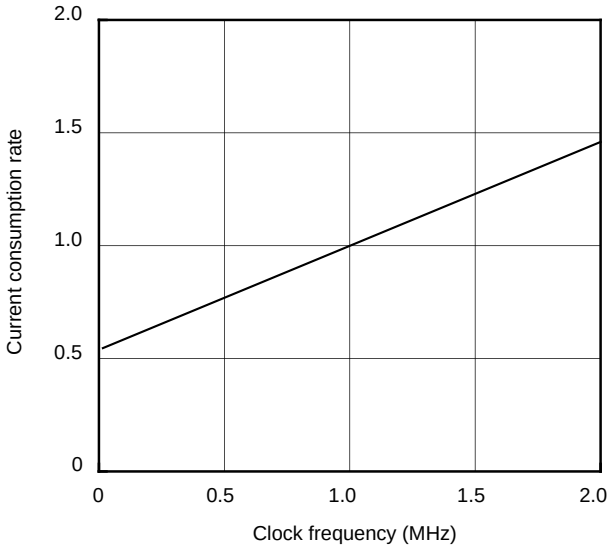
Dark voltage rate vs. Ambient temperature (Typ.)



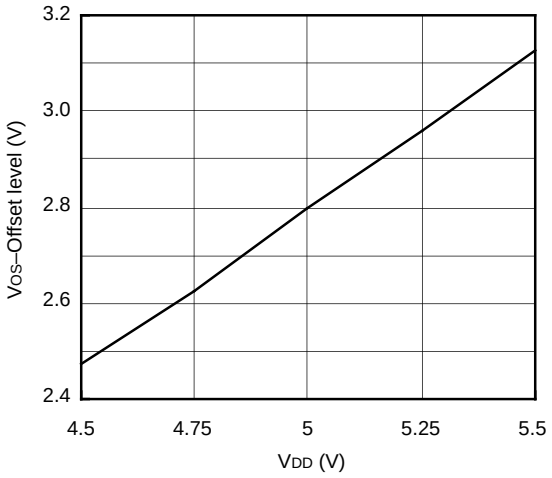
Output voltage rate vs. Integration time (Typ.)



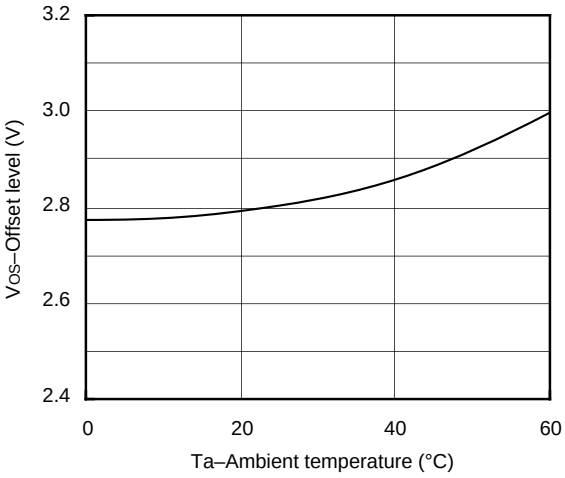
Current consumption rate vs. Clock frequency (Typ.)



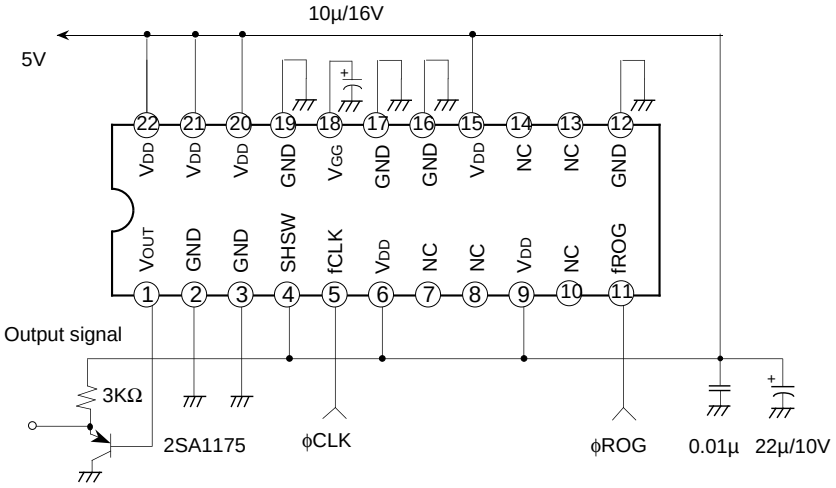
Offset level vs. V_{DD} (Typ.)



Offset level vs. Ambient temperature (Typ.)



Application Circuit (Without S/H mode (Note))



Note) This circuit diagram is the case when internal S/H is not used.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling, be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensors.

e) For the shipment of mounted substrates use cartons treated for the prevention of static charges.

2) Notes on handling CCD Cer-DIP package

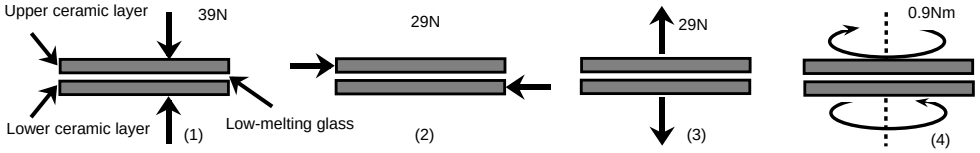
The following points should be observed when handling and installing this package.

a) (1) Compressive strength: 39N/surface
(Do not apply any load more than 0.7 mm inside the outer perimeter of the glass portion.)

(2) Shearing strength: 29N/surface

(3) Tensile strength: 29N/surface

(4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the glass to crack because the upper and lower ceramic layers are shielded by low-melting glass.

(1) Applying repetitive bending stress to the external leads.

(2) Applying heat to the external leads for an extended period of time with a soldering iron.

(3) Rapid cooling or heating.

(4) Applying a load or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.

(5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80 °C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount image sensors, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blower. (For dirt stuck through static electricity, ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

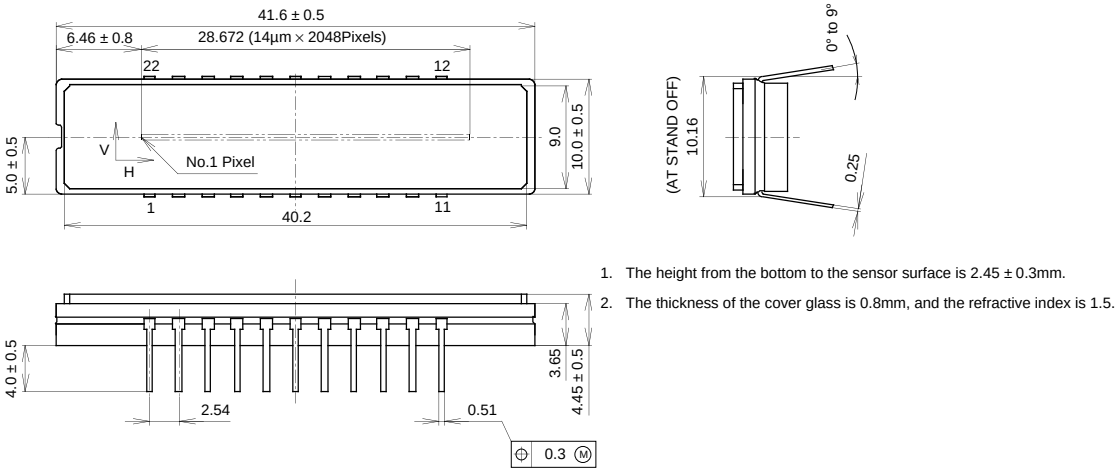
6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

7) Make sure the input pulse should not be -1 V or below.

8) Normal output signal is not obtained immediately after device switch on. Use the output signal added 22500 pulses or above to ϕ CLK clock pulse.

Package Outline Unit : mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is 2.45 ± 0.3mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.2g