PS21963/-A/-C

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21963-A

INTEGRATED POWER FUNCTIONS

600V/10A low-loss 5th generation IGBT inverter bridge for three phase DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

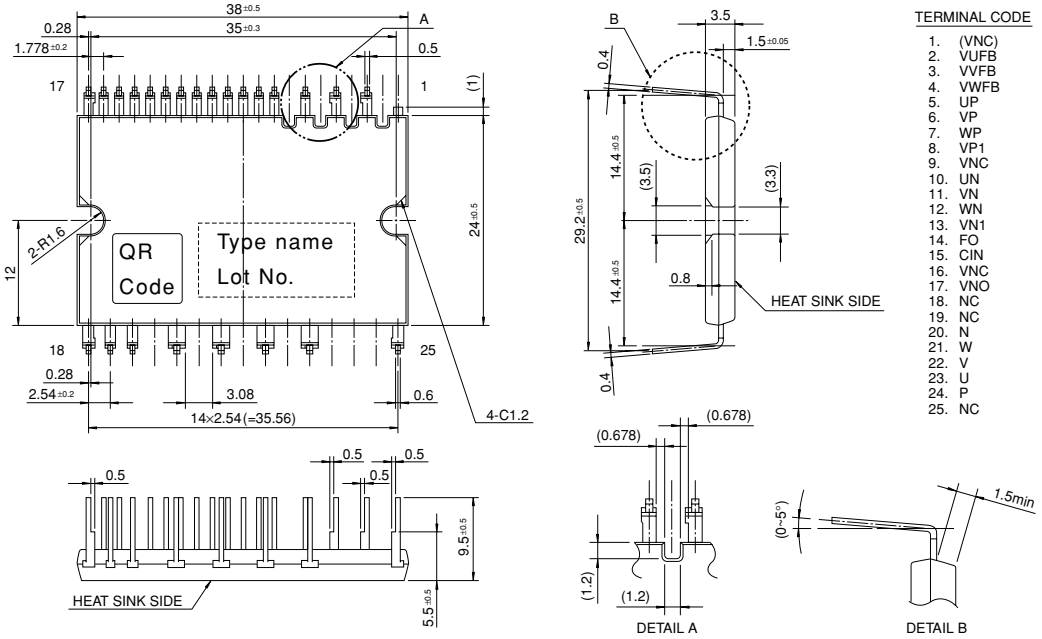
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT) or a UV fault (Lower-side supply).
- Input interface : 3V, 5V line (High Active).

APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES (PS21963)

Dimensions in mm



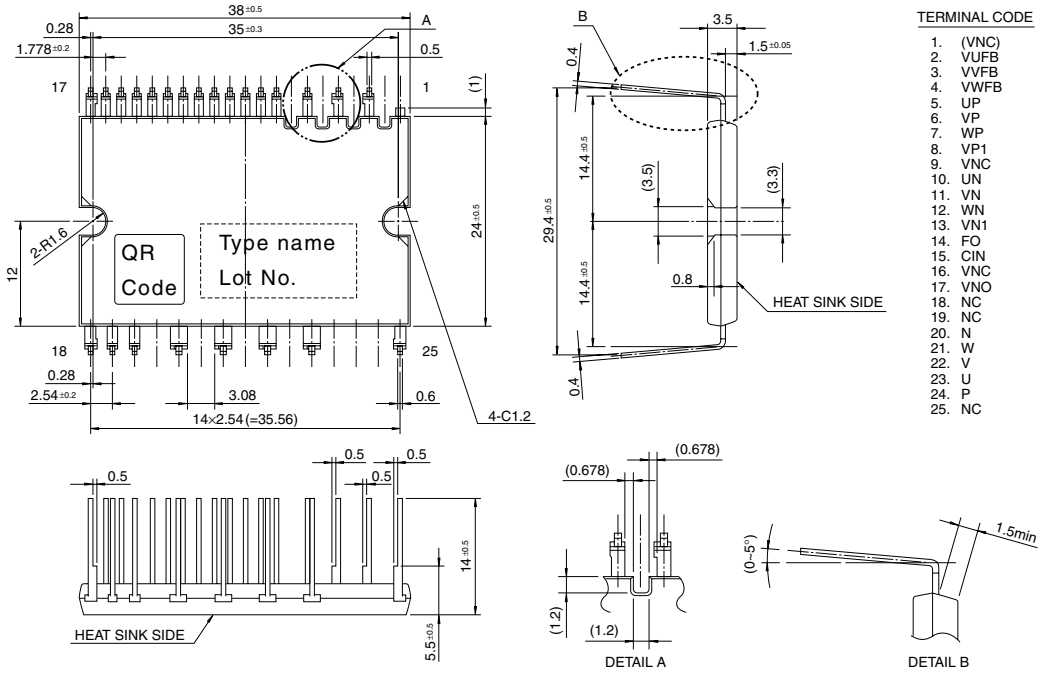
TERMINAL CODE

1.	(VNC)
2.	VUFB
3.	VVFB
4.	VWFB
5.	UP
6.	VP
7.	WP
8.	VP1
9.	VNC
10.	UN
11.	VN
12.	WN
13.	VN1
14.	FO
15.	CIN
16.	VNC
17.	VNO
18.	NC
19.	NC
20.	N
21.	W
22.	V
23.	U
24.	P
25.	NC

MITSUBISHI ELECTRIC

Fig. 2 LONG TERMINAL TYPE PACKAGE OUTLINES (PS21963-A)

Dimensions in mm

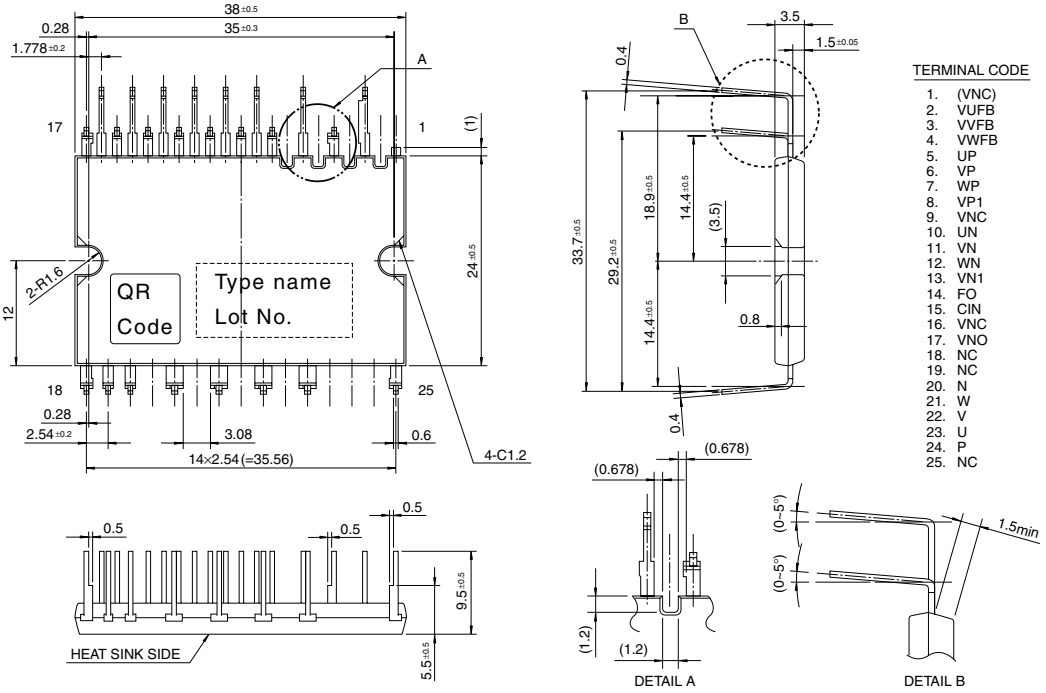


TERMINAL CODE

1. (VNC)
2. VUFB
3. VVFB
4. VWFB
5. UP
6. VP
7. WP
8. VP1
9. VNC
10. UN
11. VN
12. WN
13. VN1
14. FO
15. CIN
16. VNC
17. VNO
18. NC
19. NC
20. N
21. W
22. V
23. U
24. P
25. NC

Fig. 3 ZIGZAG TERMINAL TYPE PACKAGE OUTLINES (PS21963-C)

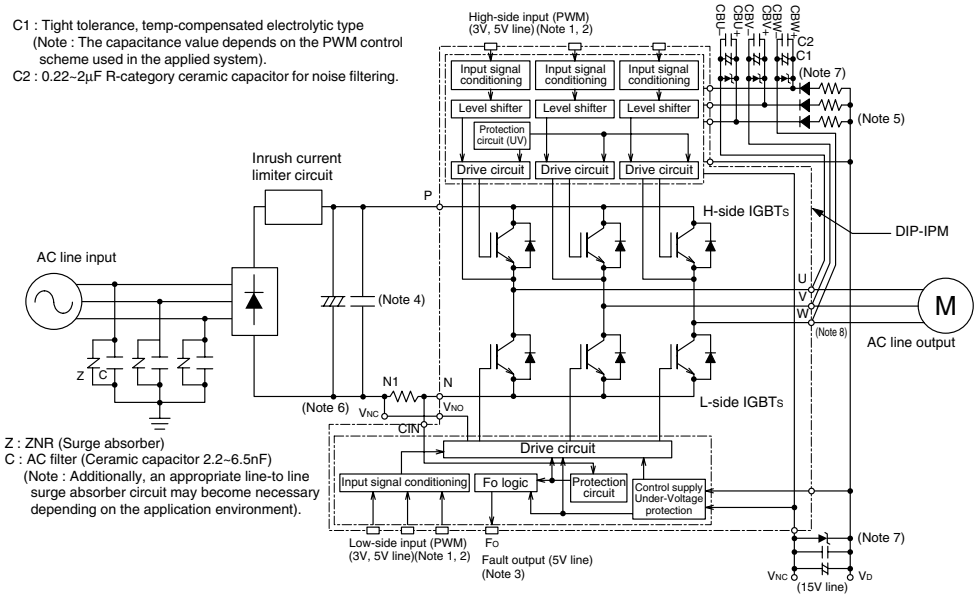
Dimensions in mm



TERMINAL CODE

1. (VNC)
2. VUFB
3. VVFB
4. VWFB
5. UP
6. VP
7. WP
8. VP1
9. VNC
10. UN
11. VN
12. WN
13. VN1
14. FO
15. CIN
16. VNC
17. VNO
18. NC
19. NC
20. N
21. W
22. V
23. U
24. P
25. NC

Fig. 4 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)



Note1: Input logic is high-active. There is a 3.3kΩ (min) pull-down resistor built-in each input circuit. When using an external CR filter, please make it satisfy the input threshold voltage.

2: By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 10)

3: This output is open drain type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor. (see also Fig. 10)

4: The wiring between the power DC link capacitor and the P & N1 terminals should be as short as possible to protect the DIP-IPM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1~0.22µF, high voltage type) is recommended to be mounted close to these P & N1 DC power input pins.

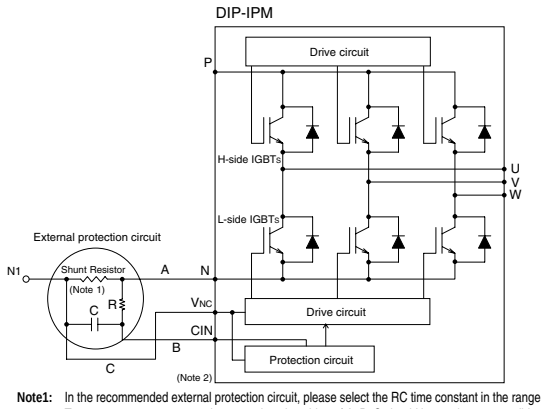
5: High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.

6: The terminal V_{NO} should be connected with the terminal V_{NC} outside.

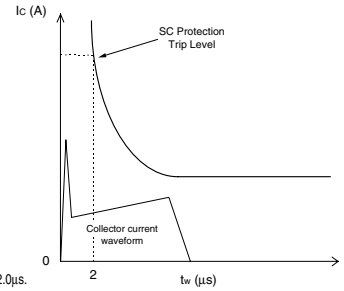
7: It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

8: Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.

Fig. 5 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) after allowing a suitable filtering time (defined by the RC circuit). When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output. Since the SC fault may be repetitive, it is recommended to stop the system when the Fo signal is received and check the fault.



Note1: In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0µs.

2: To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-N	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-N	500	V
V_{CES}	Collector-emitter voltage		600	V
±I_C	Each IGBT collector current	T_C = 25°C	10	A
±I_{CP}	Each IGBT collector current (peak)	T_C = 25°C, less than 1ms	20	A
P_C	Collector dissipation	T_C = 25°C, per 1 chip	27.0	W
T_j	Junction temperature	(Note 1)	–20~+125	°C

Note 1: The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_C \leq$ 100°C). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq$ 125°C (@ $T_C \leq$ 100°C).

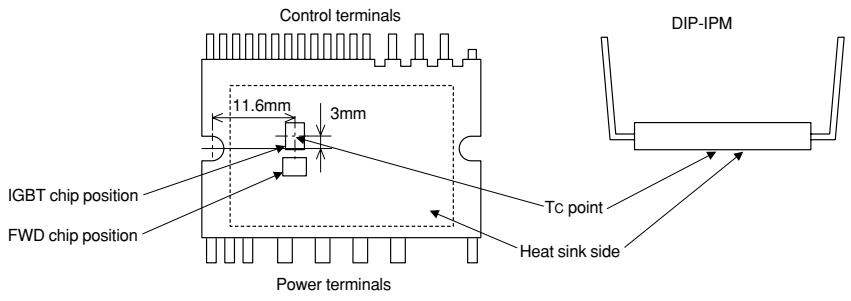
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}	–0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	–0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	–0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (short circuit protection capability)	V_D = 13.5~16.5V, Inverter part T_j = 125°C, non-repetitive, less than 2µs	400	V
T_C	Module case operation temperature	(Note 2)	–20~+100	°C
T_{stg}	Storage temperature		–40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minutes, All connected pins to heat-sink plate	1500	V_{rms}

Note 2: T_C measurement point



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	3.7	°C/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	—	—	4.5	°C/W

Note 3 : Grease with good thermal conductivity should be applied evenly with about +100µm~+200µm on the contacting surface of DIP-IPM and heat-sink.
The contacting thermal resistance between DIP-IPM case and heat sink ($R_{th(c-f)}$) is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ (per 1/6 module) is about 0.3°C/W when the grease thickness is 20µm and the thermal conductivity is 1.0W/m·k.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D = V_{DB} = 15V, V_{IN} = 5V	I_C = 10A, T_j = 25°C	—	1.70	2.20	V
			I_C = 10A, T_j = 125°C	—	1.80	2.30	
V_{EC}	FWD forward voltage	T_j = 25°C, –I_C = 10A, V_{IN} = 0V		—	1.70	2.20	V
t_{on}	Switching times	V_{CC} = 300V, V_D = V_{DB} = 15V, I_C = 10A, T_j = 125°C, V_{IN} = 0 ↔ 5V, Inductive load (upper-lower arm)		0.60	1.10	1.70	µs
t_{rr}				—	0.30	—	µs
$t_{c(on)}$				—	0.40	0.60	µs
t_{off}				—	1.50	2.10	µs
$t_{c(off)}$				—	0.50	0.80	µs
I_{CES}	Collector-emitter cut-off current	V_{CE} = V_{CES}	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	V_D = V_{DB} = 15V, V_{IN} = 5V	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	—	—	2.80	mA
			V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	—	—	0.55	mA
		V_D = V_{DB} = 15V, V_{IN} = 0V	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	—	—	2.80	mA
			V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	—	—	0.55	mA
V_{FOH}	F_O output voltage	V_{SC} = 0V, F_O terminal pull-up to 5V by 10kΩ		4.9	—	—	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		—	—	0.95	V
$V_{SC(ref)}$	Short circuit trip level	T_j = 25°C, V_D = 15V (Note 4)		0.43	0.48	0.53	V
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
UV_{DBt}	Control supply under-voltage protection	T_j ≤ 125°C	Trip level	10.0	—	12.0	V
UV_{DBr}			Reset level	10.5	—	12.5	V
UV_{Dt}			Trip level	10.3	—	12.5	V
UV_{Dr}			Reset level	10.8	—	13.0	V
t_{FO}	Fault output pulse width	(Note 5)		20	—	—	µs
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		—	2.1	2.6	V
$V_{th(off)}$	OFF threshold voltage			0.8	1.3	—	V
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.35	0.65	—	V

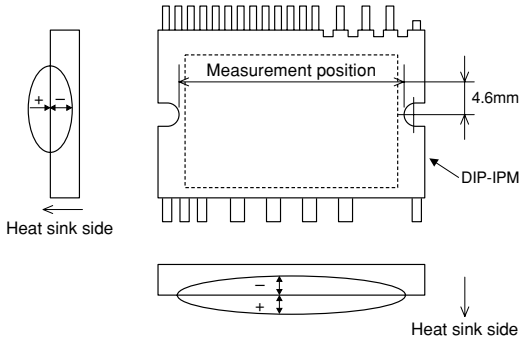
Note 4 : Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.
5 : Fault signal is asserted corresponding to a short circuit or lower side control supply under-voltage failure.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 6)	Recommended : 0.69 N·m	0.59	—	0.78	N·m
Weight			—	10	—	g
Heat-sink flatness	(Note 7)		–50	—	100	μm

Note 6 : Plain washers (ISO 7089~7094) are recommended.

Note 7 : Flatness measurement position



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-N		0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			–1	—	1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal, $T_C \leq 100°C$		1.5	—	—	μs
I_O	Output r.m.s. current	V_{CC} = 300V, V_D = V_{DB} = 15V, P.F = 0.8, sinusoidal PWM, $T_j \leq 125°C$, $T_C \leq 100°C$ (Note 8)	f_{PWM} = 5kHz	—	—	5.0	Arms
			f_{PWM} = 15kHz	—	—	3.0	
PWIN(on)	Allowable minimum input pulse width	(Note 9)		0.5	—	—	μs
PWIN(off)				0.5	—	—	
V_{NC}	V_{NC} voltage variation	Between V_{NC}-N (including surge)		–5.0	—	5.0	V

Note 8 : The allowable r.m.s. current value depends on the actual application conditions.
9 : IPM might not make response if the input signal pulse width is less than the recommended minimum value.

Fig. 6 THE DIP-IPM INTERNAL CIRCUIT

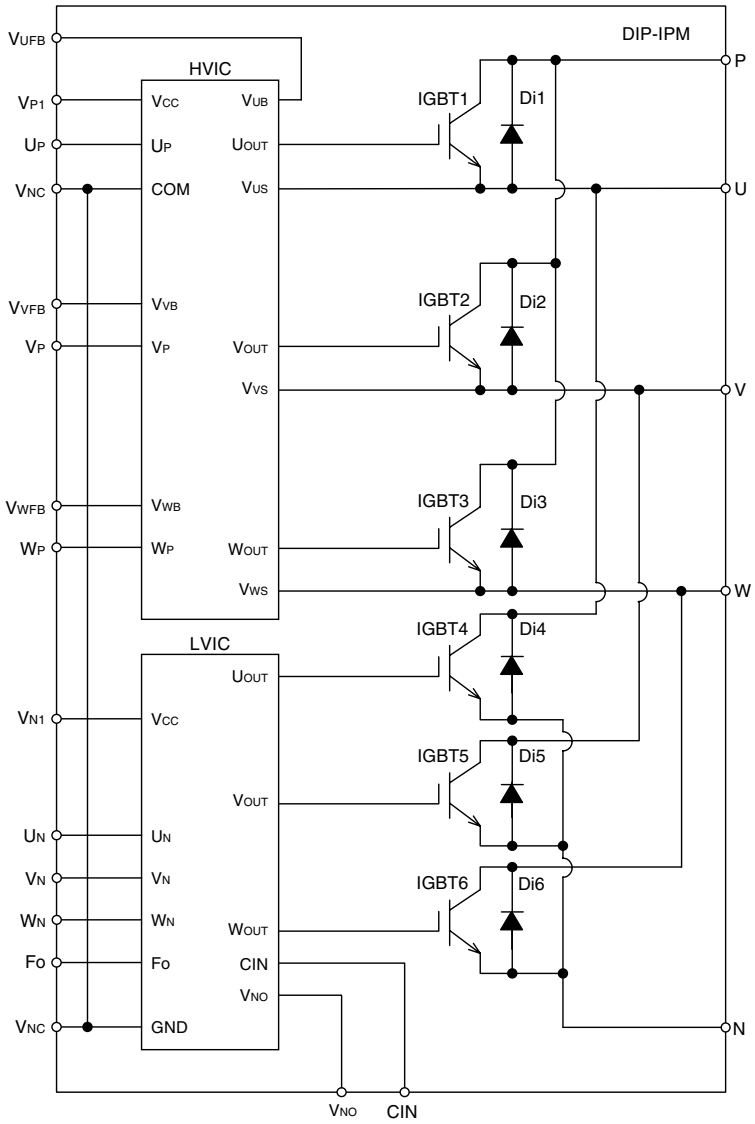
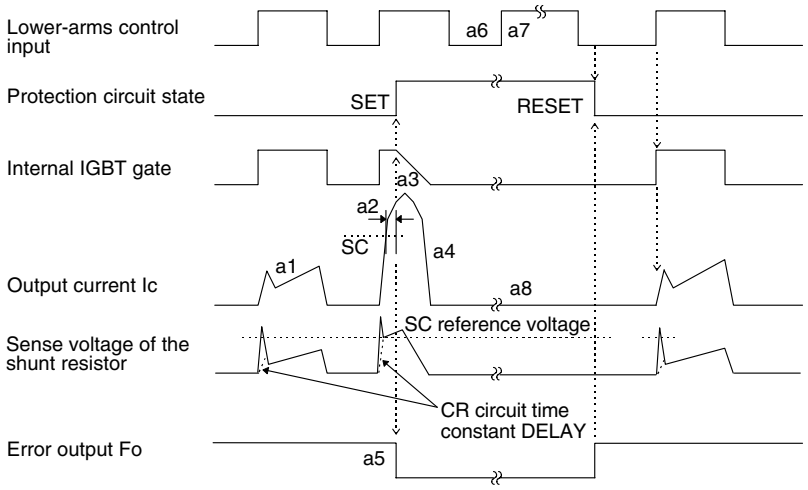


Fig. 7 TIMING CHART OF THE DIP-IPM PROTECTIVE FUNCTIONS

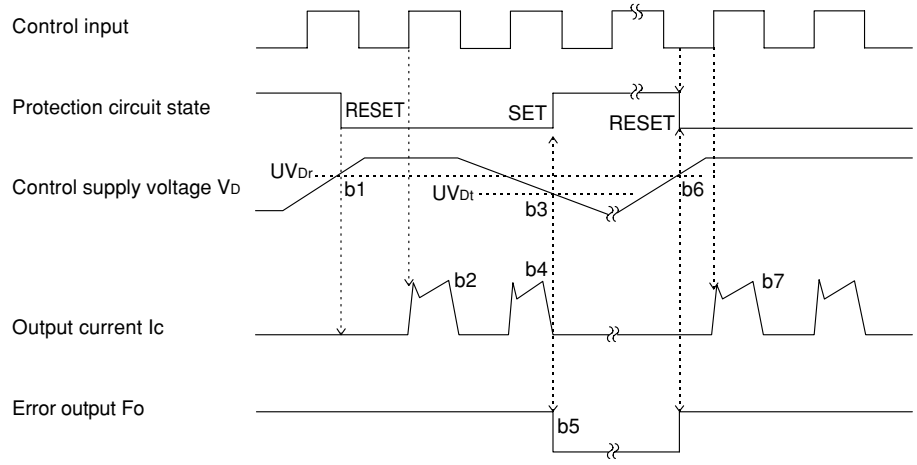
[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)

a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit detection (SC trigger).
a3. IGBT gate hard interruption.
a4. IGBT turns OFF.
a5. FO timer starts ($t_{FO(min)}$ = 20µs).
a6. Input "L" : IGBT OFF.
a7. Input "H".
a8. IGBT OFF in spite of input "H".



[B] Under-Voltage Protection (Lower-side, UV_D)

b1. Control supply voltage rising : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
b2. Normal operation : IGBT ON and carrying current.
b3. Under voltage trip (UV_{Dt}).
b4. IGBT OFF in spite of control input condition.
b5. FO output ($t_{FO} \geq 20\mu s$ and FO output continuously during UV period).
b6. Under voltage reset (UV_{Dr}).
b7. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (Upper-side, UV_{DB})

c1. Control supply voltage rises : After the voltage reaches UV_{DBr}, the circuits start to operate when next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. Under voltage trip (UV_{DBt}).
c4. IGBT OFF in spite of control input signal level, but there is no F_O signal output.
c5. Under voltage reset (UV_{DBr}).
c6. Normal operation : IGBT ON and carrying current.

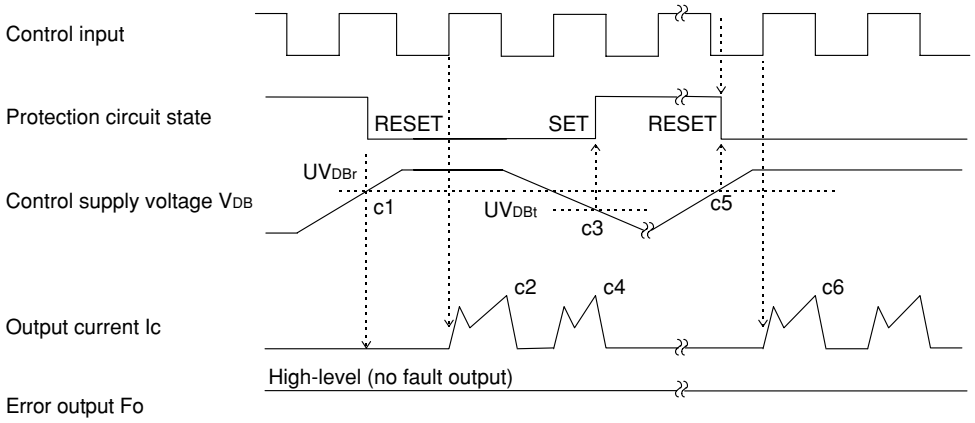
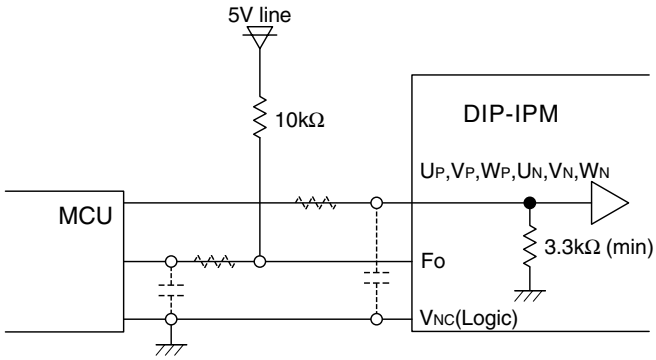


Fig. 8 RECOMMENDED MCU I/O INTERFACE CIRCUIT



Note : The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
The DIP-IPM input section integrates a 3.3kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

Fig. 9 WIRING CONNECTION OF SHUNT RESISTOR

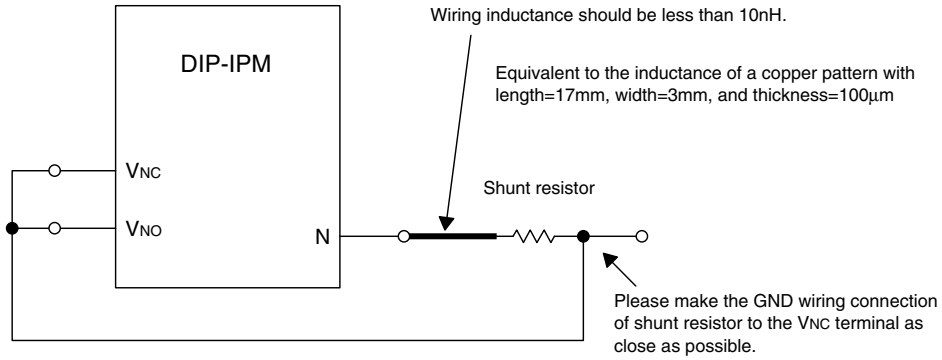
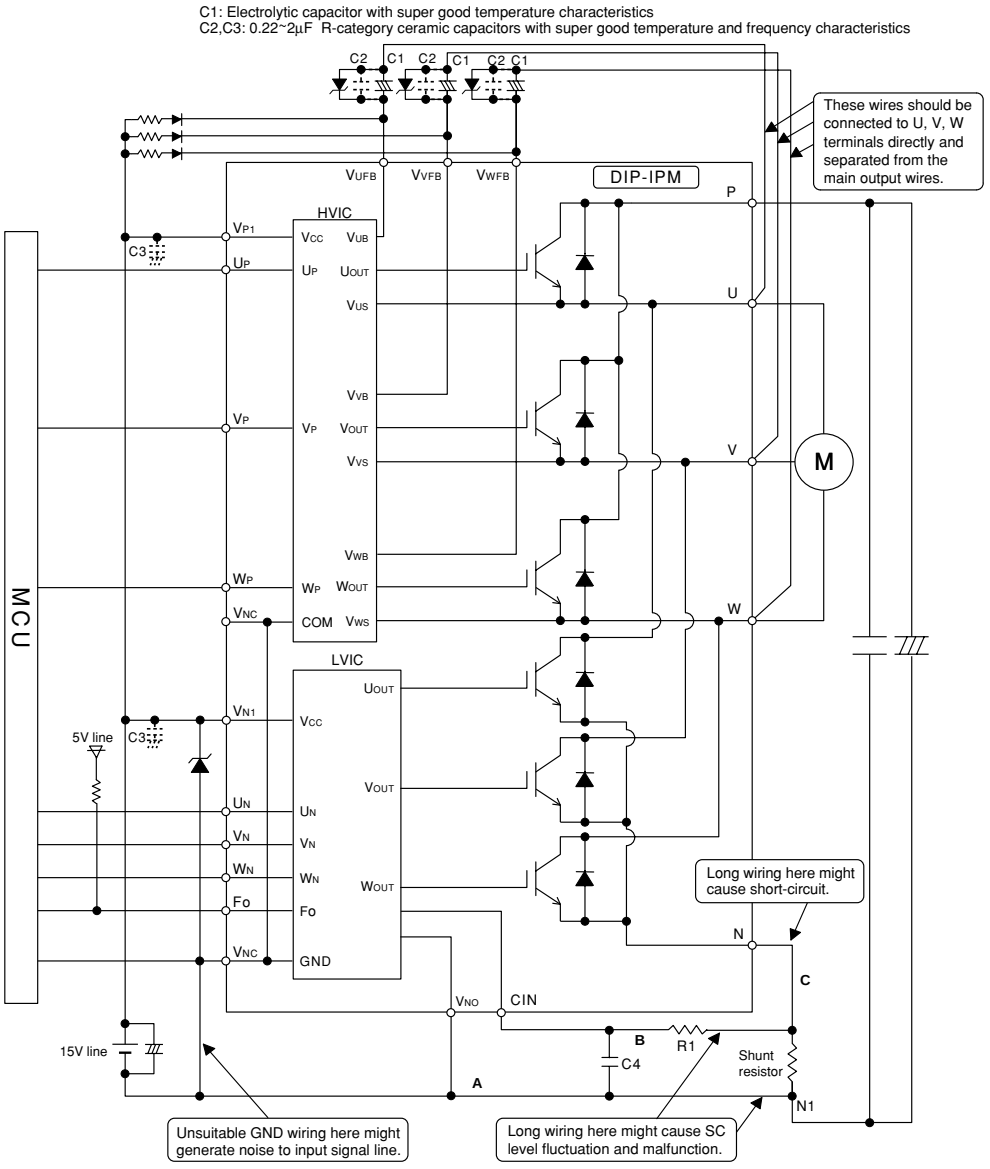


Fig. 10 AN EXAMPLE OF TYPICAL DIP-IPM APPLICATION CIRCUIT



Note 1 : To prevent malfunction, the wiring of each input should be as short as possible (2~3cm).
2 : By virtue of integrating HVIC inside, direct coupling to MCU without opto-coupler or transformer isolation is possible.
3 : FO output is open drain type, it should be pulled up to a 5V supply with an approximately 10kΩ resistor.
4 : The logic of input signal is high-active. The DIP-IPM input signal section integrates a 3.3kΩ (min) pull-down resistor. If using external filtering resistor, ensure the voltage drop of ON signal not below the threshold value.
5 : To prevent malfunction of protection, the wiring of A, B, C should be as short as possible.
6 : Please set the filter R1C4 time constant such that the IGBT can be interrupted within 2μs.
7 : Each capacitor should be located as nearby the pins of the DIP-IPM as possible.
8 : To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P&N1 pins is recommended.
9 : Make external wiring connection between VNO and VNC terminals as shown in Fig.9.
10 : Two VNC terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.
11 : It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.