## DESCRIPTION

The DAC08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 70 ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20-to-1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC08 series models guarantee full 8-bit monotonicity and linearities as tight as $0.1 \%$ over the entire operating temperature range. Device performance is essentially unchanged over the $\pm 4.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$ power supply range, with 37 mW power consumption attainable at $\pm 5 \mathrm{~V}$ supplies.
The compact size and low power consumption make the DAC08 attractive for portable and military aerospace applications.

## FEATURES

- Fast settling output current-70ns
- Full-scale current prematched to $\pm 1$ LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Relative accuracy to $0.1 \%$ maximum over temperature range
- High output compliance -10 V to +18 V
- True and complemented outputs
- Wide range multiplying capability
- Low FS current drift — $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$
- Wide power supply range- $\pm 4.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$
- Low power consumption- 37 mW at $\pm 5 \mathrm{~V}$


## APPLICATIONS

- 8-bit, 1 н A-to-D converters
- Servo-motor and pen drivers


## PIN CONFIGURATIONS

F, N Packages


D1 Package


NOTE:

1. SO and non-standard pinouts.

- Waveform generators
- Audio encoders and attenuators
- Analog meter drivers
- Programmable power supplies
- CRT display drivers
- High-speed modems
- Other applications where low cost, high speed and complete input/output versatility are required
- Programmable gain and attenuation
- Analog-Digital multiplication


## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG \# |
| :--- | :---: | :---: | :---: |
| 16-Pin Hermetic Ceramic Dual In-Line Package (Cerdip) | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | DAC08F | 0582 B |
| 16-Pin Hermetic Ceramic Dual In-Line Package (Cerdip) | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | DAC08AF | 0582 B |
| 16-Pin Plastic Dual In-Line Package (DIP) | 0 to $+70^{\circ} \mathrm{C}$ | DAC08CN | 0406 C |
| 16-Pin Hermetic Ceramic Dual In-Line Package (Cerdip) | 0 to $+70^{\circ} \mathrm{C}$ | DAC08CF | 0582 B |
| 16-Pin Plastic Dual In-Line Package (DIP) | 0 to $+70^{\circ} \mathrm{C}$ | DAC08EN | 0406 C |
| 16-Pin Hermetic Ceramic Dual In-Line Package (Cerdip) | 0 to $+70^{\circ} \mathrm{C}$ | DAC08EF | 0582 B |
| 16 -Pin Plastic Small Outline (SO) Package | 0 to $+70^{\circ} \mathrm{C}$ | DAC08ED | 0005 D |
| 16 -Pin Plastic Dual In-Line Package (DIP) | 0 to $+70^{\circ} \mathrm{C}$ | DAC08HN | 0406 C |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| V+ to V- | Power supply voltage | 36 | V |
| $\mathrm{V}_{5}-\mathrm{V}_{12}$ | Digital input voltage | V- to V-plus 36V |  |
| $\mathrm{V}_{\mathrm{LC}}$ | Logic threshold control | V - to V+ |  |
| $\mathrm{V}_{0}$ | Applied output voltage | V - to +18 | V |
| $\mathrm{I}_{14}$ | Reference current | 5.0 | mA |
| $\mathrm{V}_{14}, \mathrm{~V}_{15}$ | Reference amplifier inputs | $\mathrm{V}_{\mathrm{EE}}$ to $\mathrm{V}_{\mathrm{CC}}$ |  |
| $\mathrm{P}_{\mathrm{D}}$ | Maximum power dissipation $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (still-air) ${ }^{1}$ <br> F package <br> N package <br> D package | $\begin{aligned} & 1190 \\ & 1450 \\ & 1090 \end{aligned}$ | $\begin{aligned} & \mathrm{mW} \\ & \mathrm{~mW} \\ & \mathrm{~mW} \end{aligned}$ |
| TSOLD | Lead soldering temperature (10sec max) | 300 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{A}}$ | Operating temperature range <br> DAC08, DAC08A <br> DAC08C, E, H | $\begin{gathered} -55 \text { to }+125 \\ 0 \text { to }+70 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |
| $\mathrm{T}_{\text {STG }}$ | Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## NOTES

1. Derate above $25^{\circ} \mathrm{C}$, at the following rates:

F package at $9.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$
N package at $11.6 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$
D package at $8.7 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$

## DC ELECTRICAL CHARACTERISTICS

Pin 3 must be at least 3 V more negative than the potential to which $R_{15}$ is returned. $\mathrm{V}_{\mathrm{C}}= \pm 15 \mathrm{~V}$, $\mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA}$. Output characteristics refer to both $\mathrm{l}_{\text {OUT }}$ and $\overline{\mathrm{OUT}}$ unless otherwise noted. DAC08C, $\mathrm{E}, \mathrm{H}: \mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ DAC08/08A: $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS | DAC08C |  |  | $\begin{gathered} \text { DAC08E } \\ \text { DAC08 } \end{gathered}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
|  | Resolution |  | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
|  | Monotonicity |  | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
|  | Relative accuracy | Over temperature range |  |  |  |  |  |  |  |
|  | Differential non-linearity |  |  |  | $\pm 0.78$ |  |  | $\pm 0.39$ | \%FS |
| TCI ${ }_{\text {FS }}$ | Full-scale tempco |  |  | $\pm 10$ |  |  | $\pm 10$ |  | ppm/ ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{OC}}$ | Output voltage compliance | Full-scale current change<1/2LSB | -10 |  | +18 | -10 |  | +18 | V |
| $\mathrm{I}_{\text {FS4 }}$ | Full-scale current | $\mathrm{V}_{\mathrm{REF}}=10.000 \mathrm{~V}, \mathrm{R}_{14}, \mathrm{R}_{15}=5.000 \mathrm{k} \Omega$ | 1.94 | 1.99 | 2.04 | 1.94 | 1.99 | 2.04 | mA |
| $\mathrm{I}_{\text {FSS }}$ | Full-scale symmetry | $\mathrm{I}_{\text {FS4 }}{ }^{-\mathrm{I}_{\text {FS }}}$ |  | $\pm 2.0$ | $\pm 16$ |  | $\pm 1.0$ | $\pm 8.0$ | $\mu \mathrm{A}$ |
| Izs | Zero-scale current |  |  | 0.2 | 4.0 |  | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {FSR }}$ | Full-scale output current range | $\begin{gathered} R_{14,}, R_{15}=5.000 \mathrm{k} \Omega \\ \mathrm{~V}_{\text {REF }}=+15.0 \mathrm{~V}, \mathrm{~V}-=-10 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{REF}}=+25.0 \mathrm{~V}, \mathrm{~V}-=-12 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{aligned} & 2.1 \\ & 4.2 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 2.1 \\ & 4.2 \\ & \hline \end{aligned}$ |  |  | mA |
| $\begin{aligned} & \mathrm{V}_{\mathrm{IL}} \\ & \mathrm{~V}_{\mathrm{IH}} \end{aligned}$ | Logic input levels Low High | $\mathrm{V}_{\mathrm{LC}}=0 \mathrm{~V}$ | 2.0 |  | 0.8 | 2.0 |  | 0.8 | V |
| $\begin{aligned} & \mathrm{I}_{\mathrm{IL}} \\ & \mathrm{I}_{\mathrm{IH}} \\ & \hline \end{aligned}$ | Logic input current Low High | $\begin{gathered} \mathrm{V}_{\mathrm{LC}}=0 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=-10 \mathrm{~V} \text { to }+0.8 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=2.0 \mathrm{~V} \text { to } 18 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} -2.0 \\ 0.002 \\ \hline \end{gathered}$ | $\begin{array}{r} -10 \\ 10 \\ \hline \end{array}$ |  | $\begin{gathered} -2.0 \\ 0.002 \end{gathered}$ | $\begin{array}{r} -10 \\ 10 \\ \hline \end{array}$ | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {IS }}$ | Logic input swing | V -=-15V | -10 |  | +18 | -10 |  | +18 | V |
| $\mathrm{V}_{\text {THR }}$ | Logic threshold range | $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ | -10 |  | +13.5 | -10 |  | +13.5 | V |
| $\mathrm{I}_{15}$ | Reference bias current |  |  | -1.0 | -3.0 |  | -1.0 | -3.0 | $\mu \mathrm{A}$ |
| dl/dt | Reference input slew rate |  | 4.0 | 8.0 |  | 4.0 | 8.0 |  | $\mathrm{mA} / \mu \mathrm{s}$ |
| $\mathrm{PSSI}_{\mathrm{FS}+}$ $\mathrm{PSI}_{\mathrm{FS}}$ | Power supply sensitivity Positive <br> Negative | $\begin{gathered} \hline \mathrm{I}_{\mathrm{REFF}}=1 \mathrm{~mA} \\ \mathrm{~V}+=4.5 \text { to } 5.5 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V} ; \\ \mathrm{V}+=13.5 \text { to } 16.5 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V} \\ \mathrm{~V}=-4.5 \text { to }-5.5 \mathrm{~V}, \mathrm{~V}+=+15 \mathrm{~V} ; \\ \mathrm{V}-=-13.5 \text { to }-16.5, \mathrm{~V}+=+15 \mathrm{~V} \end{gathered}$ |  | $\begin{aligned} & 0.0003 \\ & 0.002 \end{aligned}$ | $\begin{aligned} & 0.01 \\ & 0.01 \end{aligned}$ |  | $\begin{aligned} & 0.0003 \\ & 0.002 \end{aligned}$ | $\begin{aligned} & 0.01 \\ & 0.01 \end{aligned}$ | \%FS/\%VS |
| $\begin{aligned} & \mathrm{I}+ \\ & \mathrm{I}- \\ & \hline \end{aligned}$ | Power supply current Positive Negative | $\mathrm{V}_{\mathrm{S}}= \pm 5 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=1.0 \mathrm{~mA}$ |  | $\begin{array}{r} 3.1 \\ -4.3 \\ \hline \end{array}$ | $\begin{gathered} 3.8 \\ -5.8 \\ \hline \end{gathered}$ |  | $\begin{array}{r} 3.1 \\ -4.3 \\ \hline \end{array}$ | $\begin{gathered} 3.8 \\ -5.8 \end{gathered}$ |  |
| $\begin{aligned} & 1+ \\ & 1+ \\ & 1- \end{aligned}$ | Positive Negative | $\mathrm{V}_{\mathrm{S}}=+5 \mathrm{~V},-15 \mathrm{~V}, \mathrm{I}_{\text {ReF }}=2.0 \mathrm{~mA}$ |  | $\begin{gathered} \hline 3.1 \\ -7.1 \end{gathered}$ | $\begin{gathered} 3.8 \\ -7.8 \end{gathered}$ |  | $\begin{gathered} \hline 3.1 \\ -7.1 \end{gathered}$ | $\begin{gathered} 3.8 \\ -7.8 \end{gathered}$ | mA |
| $\begin{array}{\|l\|} \hline 1+ \\ 1- \end{array}$ | Positive Negative | $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{I}_{\text {REF }}=2.0 \mathrm{~mA}$ |  | $\begin{gathered} 3.2 \\ -7.2 \end{gathered}$ | $\begin{gathered} 3.8 \\ -7.8 \end{gathered}$ |  | $\begin{gathered} 3.2 \\ -7.2 \end{gathered}$ | $\begin{gathered} 3.8 \\ -7.8 \end{gathered}$ |  |
| $\mathrm{P}_{\mathrm{D}}$ | Power dissipation | $\begin{gathered} \pm 5 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=1.0 \mathrm{~mA} \\ +5 \mathrm{~V},-15 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA} \\ \pm 15 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 37 \\ 122 \\ 156 \end{gathered}$ | $\begin{gathered} 48 \\ 136 \\ 174 \\ \hline \end{gathered}$ |  | $\begin{gathered} 37 \\ 122 \\ 156 \end{gathered}$ | $\begin{gathered} 48 \\ 136 \\ 174 \\ \hline \end{gathered}$ | mW |

DC ELECTRICAL CHARACTERISTICS (Continued)
Pin 3 must be at least 3 V more negative than the potential to which R 15 is returned. $\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA}$, Output characteristics refer to both I IOUT and IOUT, unless otherwise noted. DAC08C, E, H: $T_{A}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$. DAC08/08A: $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$.

| SYMBOL | PARAMETER | TEST CONDITIONS | DAC08H DAC08A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
|  | Resolution |  | 8 | 8 | 8 | Bits |
|  | Monotonicity |  | 8 | 8 | 8 | Bits |
|  | Relative accuracy Differential non-linearity | Over temperature range |  |  | $\begin{gathered} \pm 0.1 \\ \pm 0.19 \end{gathered}$ | $\begin{aligned} & \hline \text { \%FS } \\ & \text { \%FS } \end{aligned}$ |
| $\mathrm{TCl}_{\text {FS }}$ | Full-scale tempco |  |  | $\pm 10$ | $\pm 50$ | ppm/ ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {OC }}$ | Output voltage compliance | Full-scale current change 1/2LSB | -10 |  | +18 | V |
| $\mathrm{I}_{\text {FS4 }}$ | Full-scale current | $\mathrm{V}_{\mathrm{REF}}=10.000 \mathrm{~V}, \mathrm{R}_{14}, \mathrm{R}_{15}=5.000 \mathrm{k} \Omega$ | 1.984 | 1.992 | 2.000 | mA |
| $\mathrm{I}_{\text {FSS }}$ | Full-scale symmetry | $\mathrm{I}_{\text {FS4 }}{ }^{-1} \mathrm{FS} 2$ |  | $\pm 1.0$ | $\pm 4.0$ | $\mu \mathrm{A}$ |
| Izs | Zero-scale current |  |  | 0.2 | 1.0 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {FSR }}$ | Full-scale output current range | $\begin{gathered} \mathrm{R}_{14,}, \mathrm{R}_{15}=5.000 \mathrm{k} \Omega \\ \mathrm{~V}_{\mathrm{REF}}=+15.0 \mathrm{~V}, \mathrm{~V}-=-10 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{REF}}=+25.0 \mathrm{~V}, \mathrm{~V}-=-12 \mathrm{~V} \end{gathered}$ | $\begin{array}{r} 2.1 \\ 4.2 \\ \hline \end{array}$ |  |  | mA |
| $\begin{aligned} & \mathrm{V}_{\mathrm{IL}} \\ & \mathrm{~V}_{\mathrm{IH}} \end{aligned}$ | Logic input levels Low High | $\mathrm{V}_{\mathrm{LC}}=0 \mathrm{~V}$ | 2.0 |  | 0.8 | V |
| $\begin{aligned} & I_{\mathrm{IL}} \\ & I_{\mathrm{HH}} \end{aligned}$ | Logic input current Low High | $\begin{gathered} \mathrm{V}_{\mathrm{LC}}=0 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=-10 \mathrm{~V} \text { to }+0.8 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=2.0 \mathrm{~V} \text { to } 18 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} -2.0 \\ 0.002 \end{gathered}$ | $\begin{array}{r} -10 \\ 10 \\ \hline \end{array}$ | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {IS }}$ | Logic input swing | V -=-15V | -10 |  | +18 | V |
| $\mathrm{V}_{\text {THR }}$ | Logic threshold range | $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ | -10 |  | +13.5 | V |
| $\mathrm{I}_{15}$ | Reference bias current |  |  | -1.0 | -3.0 | $\mu \mathrm{A}$ |
| d//dt | Reference input slew rate |  | 4.0 | 8.0 |  | $\mathrm{mA} / \mu \mathrm{s}$ |
| $\begin{aligned} & \mathrm{PSSI}_{\mathrm{FS}+} \\ & \mathrm{PSI}_{\mathrm{FS}-} \end{aligned}$ | Power supply sensitivity Positive <br> Negative | $\begin{gathered} \hline \mathrm{I}_{\mathrm{REF}}=1 \mathrm{~mA} \\ \mathrm{~V}+=4.5 \text { to } 5.5 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V} ; \\ \mathrm{V}+=13.5 \text { to } 16.5 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V} \\ \mathrm{~V}-=-4.5 \text { to }-5.5 \mathrm{~V}, \mathrm{~V}+=+15 \mathrm{~V} ; \\ \mathrm{V}-=-13.5 \text { to }-16.5, \mathrm{~V}+=+15 \mathrm{~V} \end{gathered}$ |  | $\begin{aligned} & 0.0003 \\ & 0.002 \end{aligned}$ | $\begin{aligned} & 0.01 \\ & 0.01 \end{aligned}$ | \%FS/\%VS |
| $\begin{aligned} & 1+ \\ & 1- \\ & \hline \end{aligned}$ | Power supply current Positive Negative | $\mathrm{V}_{\mathrm{S}}= \pm 5 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=1.0 \mathrm{~mA}$ |  | $\begin{gathered} 3.1 \\ -4.3 \end{gathered}$ | $\begin{gathered} 3.8 \\ -5.8 \end{gathered}$ |  |
| $\begin{array}{\|l\|} \hline 1+ \\ 1- \\ \hline \end{array}$ | Positive Negative | $\mathrm{V}_{\mathrm{S}}=+5 \mathrm{~V},-15 \mathrm{~V}, \mathrm{I}_{\text {REF }}=2.0 \mathrm{~mA}$ |  | $\begin{gathered} \hline 3.1 \\ -7.1 \end{gathered}$ | $\begin{gathered} \hline 3.8 \\ -7.8 \end{gathered}$ | mA |
| $\begin{array}{\|l\|} \hline 1+ \\ 1- \\ \hline \end{array}$ | Positive Negative | $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{I}_{\text {REF }}=2.0 \mathrm{~mA}$ |  | $\begin{gathered} \hline 3.2 \\ -7.2 \end{gathered}$ | $\begin{gathered} \hline 3.8 \\ -7.8 \end{gathered}$ |  |
| $\mathrm{P}_{\mathrm{D}}$ | Power dissipation | $\begin{gathered} \pm 5 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=1.0 \mathrm{~mA} \\ +5 \mathrm{~V},-15 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA} \\ \pm 15 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA} \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline 37 \\ 122 \\ 156 \\ \hline \end{gathered}$ | $\begin{gathered} 48 \\ 136 \\ 174 \end{gathered}$ | mW |

## AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | DAC08C |  |  | $\begin{gathered} \hline \text { DAC08E } \\ \text { DAC08 } \end{gathered}$ |  |  | DAC08H DAC08A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| ts | Settling time | To $\pm 1 / 2 \mathrm{LSB}$, all bits switched on or off, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 70 | 135 |  | 70 | 135 |  | 70 | 135 | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLL}} \\ & \mathrm{t}_{\mathrm{PH}} \end{aligned}$ | Propagation delay <br> Low-to-High <br> High-to-Low | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, each bit. <br> All bits switched |  | 35 | 60 |  | 35 | 60 |  | 35 | 60 | ns |

## TEST CIRCUITS



Figure 1. Relative Accuracy Test Circuit


Figure 2. Transient Response and Settling Time

## 8-Bit high-speed multiplying D/A converter

## TEST CIRCUITS (Continued)



Figure 3. Reference Current Slew Rate Measurement

NOTES
(See text for values of C .)
Typical values of $R_{14}=R_{15}=1 \mathrm{k}$


$$
\begin{aligned}
& V_{\text {REF }}=+2 \\
& C=15 \mathrm{pF}
\end{aligned}
$$

$V_{1}$ and $I_{I}$ apply to inputs $A_{1}$ through $A_{8}$
The resistor tied to Pin 15 is to temperature compensate the bias current and may not be necessary for all applications
$I_{O}=K\left|\frac{A_{1}}{2}+\frac{A_{2}}{4}+\frac{A_{3}}{8}+\frac{A_{4}}{16}+\frac{A_{5}}{32}+\frac{A_{6}}{64}+\frac{A_{7}}{128}+\frac{A_{8}}{256}\right|$
where $K \approx \frac{V_{R E F}}{R_{14}}$
and $A_{N}=$ ' 1 ' if $A_{N}$ is at High Level
$A_{N}=$ ' 0 ' if $A_{N}$ is at Low Level
Figure 4. Notation Definitions

## TYPICAL PERFORMANCE CHARACTERISTICS



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

## Reference AMP Common-Mode Range All Bits On


$\mathrm{V}_{15}$ - REFERENCE COMMON MODE VOLTAGE (V) POSITIVE COMMON-MODE RANGE IS ALWAYS $(\mathrm{V}+)-1.5 \mathrm{~V}$.


Bit Transfer Characteristics


NOTES:
$\mathrm{B}_{1}$ through $\mathrm{B}_{8}$ have identical transfer characteristics. Bits are fully switched, with less than 1/2LSB error, at less than $\pm 100 \mathrm{mV}$ from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0 V over the operating temperature range ( $\mathrm{V}_{\mathrm{LC}}=0.0 \mathrm{~V}$ ).
$\mathrm{V}_{\mathrm{TH}}-\mathrm{V}_{\mathrm{LC}}$ vs Temperature


Power Supply Current vs $\mathbf{V}_{+}$



Power Supply Current vs V-


Power Supply Current vs Temperature


Maximum Reference Input Frequency vs Compensation Capacitor Value


## TYPICAL APPLICATION



NOTES:
$R E Q=R_{I N} \| R_{P}$
Typical Values
$\mathrm{R}_{\mathrm{IN}}=5 \mathrm{k} \Omega$
$+\mathrm{V}_{\text {IN }}=10 \mathrm{~V}$
Pulsed Referenced Operation

## FUNCTIONAL DESCRIPTION

## Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.
Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, $\mathrm{R}_{15}$ can be tied to a negative voltage corresponding to the minimum input level. $R_{15}$ may be eliminated with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased as $\mathrm{R}_{14}$ value is increased. This is in order to maintain proper phase margin. For $R_{14}$ values of $1.0,2.5$, and $5.0 \mathrm{k} \Omega$, minimum capacitor values are 15 , 37 , and 75 pF , respectively. The capacitor may be tied to either $\mathrm{V}_{\mathrm{EE}}$ or ground, but using $\mathrm{V}_{\mathrm{EE}}$ increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if $R_{14}$ is grounded and the reference voltage is applied to $R_{15}$ as shown. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0 V above the $\mathrm{V}_{\text {EE }}$ supply. Bipolar input signals may be handled by connecting $\mathrm{R}_{14}$ to a positive reference voltage equal to the peak positive input level at Pin 15.
When using a DC reference voltage, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage, but if a well regulated 5.0 V supply which drives logic is to be used as the reference, $\mathrm{R}_{14}$ should be formed of two series resistors with the junction of the two resistors bypassed with $0.1 \mu \mathrm{~F}$ to ground. For reference voltages greater than 5.0 V , a clamp diode is recommended between Pin 14 and ground.
If $P$ in 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods applies and the amplifier must be heavily compensated, decreasing the overall bandwidth.

## Output Voltage Range

The voltage at Pin 4 must always be at least 4.5 V more positive than the voltage of the negative supply (Pin 3) when the reference current
is 2 mA or less, and at least 8 V more positive than the negative supply when the reference current is between 2 mA and 4 mA . This is necessary to avoid saturation of the output transistors, which would cause serious accuracy degradation.

## Output Current Range

Any time the full-scale current exceeds 2 mA , the negative supply must be at least 8 V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

## Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the DAC08 series is essentially constant over the operating temperature range due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC08 series has a very low full-scale current drift over the operating temperature range.

The DAC08 series is guaranteed accurate to within $\pm \mathrm{LSB}$ at $+25^{\circ} \mathrm{C}$ at a full-scale output current of 1.992 mA . The relative accuracy test circuit is shown in Figure 1. The 12-bit converter is calibrated to a full-scale output current of 1.99219 mA , then the DAC08 full-scale current is trimmed to the same value with $R_{14}$ so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.
Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of $\pm$ part in 65,536 , or $\pm 0.00076 \%$, which is much more accurate than the $\pm 0.19 \%$ specification of the DAC08 series.

## Monotonicity

A monotonic converter is one which always provides analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The DAC08 series is monotonic for all values of reference current above 0.5 mA . The recommended range for operation is a DC reference current between 0.5 mA and 4.0 mA .

## Settling Time

The worst-case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within LSB for 8-bit accuracy. This time applies when $\mathrm{R}_{\mathrm{L}}<500 \Omega$ and $\mathrm{C}_{\mathrm{O}}<25 \mathrm{pF}$. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the DAC functions in a positive-going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.
Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, $100 \mu \mathrm{~F}$ supply bypassing for low frequencies, minimum scope lead length, and avoidance of ground loops are all mandatory.

## SETTLING TIME AND PROPAGATION DELAY



NOTES:
$D_{1}, D_{2}=$ IN6263 or equivalent
$\mathrm{D}_{3}=$ IN914 or equivalent
$\mathrm{C}_{1}=0.01 \mu \mathrm{~F}$
$\mathrm{C}_{2}, \mathrm{C}_{3}=0.1 \mu \mathrm{~F}$
$\mathrm{Q}_{1}=2$ N3904
$\mathrm{C}_{4}, \mathrm{C}_{5}=15 \mathrm{pF}$ and includes all probe and fixturing capacitance.

## BASIC DAC08 CONFIGURATION



NOTES:
$I_{\text {FS }} \approx \frac{+V_{\text {REF }}}{R_{\text {REF }}} \times \frac{255}{256} ; 1_{O}+\bar{I}_{\mathrm{O}}=\mathrm{I}_{\text {FS }}$ for all logic states

## RECOMMENDED FULL-SCALE AND ZERO-SCALE ADJUST



NOTES:
$\mathrm{R}_{1}=$ low T.C.
$R_{3}=R_{1}+R_{2}$
$R_{2} \approx 0.1 R_{1}$ to minimize pot. contribution to full-scale drift

## UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT



## UNIPOLAR VOLTAGE OUTPUT FOR HIGH IMPEDANCE OUTPUT



BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)


|  | $\mathbf{B}_{\mathbf{1}}$ | $\mathbf{B}_{\mathbf{2}}$ | $\mathbf{B}_{\mathbf{3}}$ | $\mathbf{B}_{\mathbf{4}}$ | $\mathbf{B}_{\mathbf{5}}$ | $\mathbf{B}_{\mathbf{6}}$ | $\mathbf{B}_{\mathbf{7}}$ | $\mathbf{B}_{\mathbf{8}}$ | $\mathbf{V}_{\mathbf{O U T}}$ | $\mathbf{\nabla}_{\mathbf{O U T}}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Positive full-scale | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -9.920 V | +10.000 |
| Positive FS - 1LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -9.840 V | +9.920 |
| + Zero-scale + 1LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -0.080 V | +0.160 |
| Zero-scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | +0.080 |
| Zero-scale - 1LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.080 | 0.000 |
| Negative full scale - 1LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +9.920 | -9.840 |
| Negative full scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +10.000 | -9.920 |

