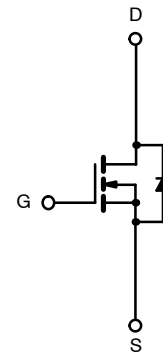
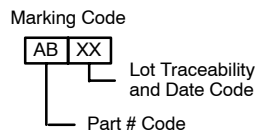
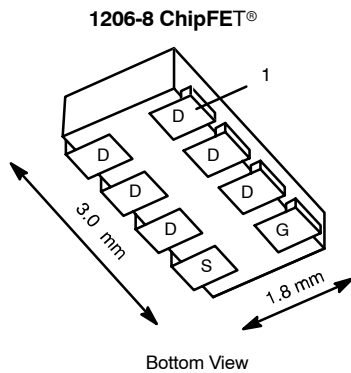


## N-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
20	0.030 @ $V_{GS} = 4.5$ V	7.2
	0.045 @ $V_{GS} = 2.5$ V	5.9

**TrenchFET<sup>®</sup>**  
Power MOSFETS  
2.5-V Rated



Ordering Information: Si5404DC-T1

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		$V_{DS}$	20		V
Gate-Source Voltage		$V_{GS}$	$\pm 12$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	7.2	5.2	A
	$T_A = 85^\circ\text{C}$		5.2	3.8	
Pulsed Drain Current		$I_{DM}$	20		
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	2.1	1.1	
Maximum Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2.5	1.3	W
	$T_A = 85^\circ\text{C}$		1.3	0.7	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 5$ sec	$R_{thJA}$	40	50	$^\circ\text{C}/\text{W}$
	Steady State		80	95	
Maximum Junction-to-Foot (Drain)		$R_{thJF}$	15	20	

Notes

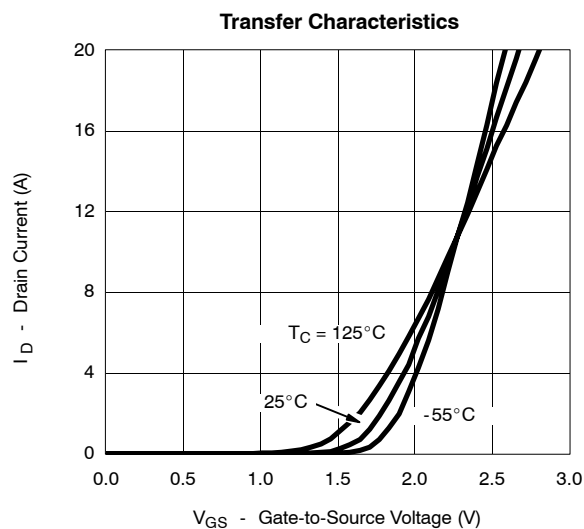
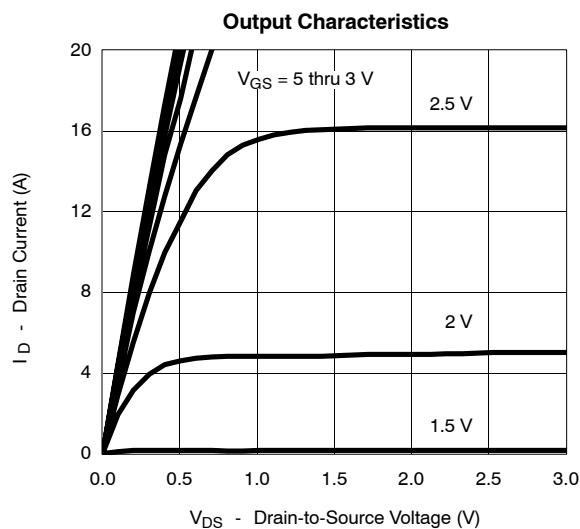
- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.6			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	20			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.2 A		0.025	0.030	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 4.3 A		0.038	0.045	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.2 A		20		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.1 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.2 A		12	18	nC
Gate-Source Charge	Q <sub>gs</sub>			2.4		
Gate-Drain Charge	Q <sub>gd</sub>			3.2		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 4.5 V, R <sub>G</sub> = 6 Ω		20	30	ns
Rise Time	t <sub>r</sub>			40	60	
Turn-Off Delay Time	t <sub>d(off)</sub>			40	60	
Fall Time	t <sub>f</sub>			15	23	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.1 A, di/dt = 100 A/μs		30	60	

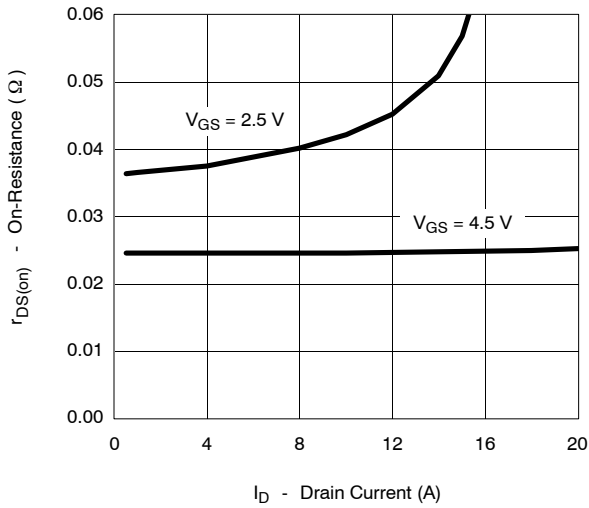
## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

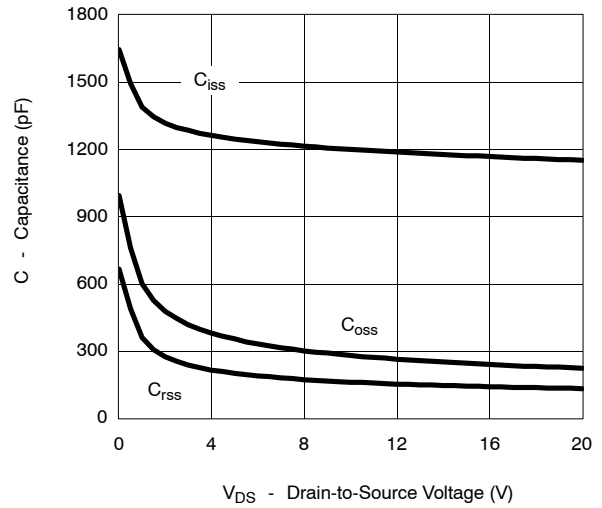
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

## TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

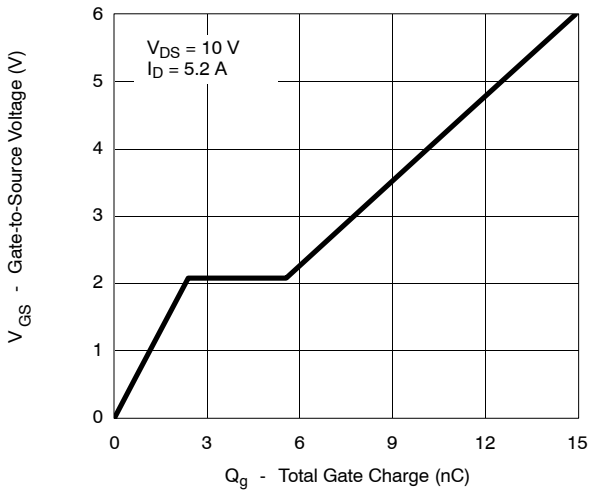
**On-Resistance vs. Drain Current**



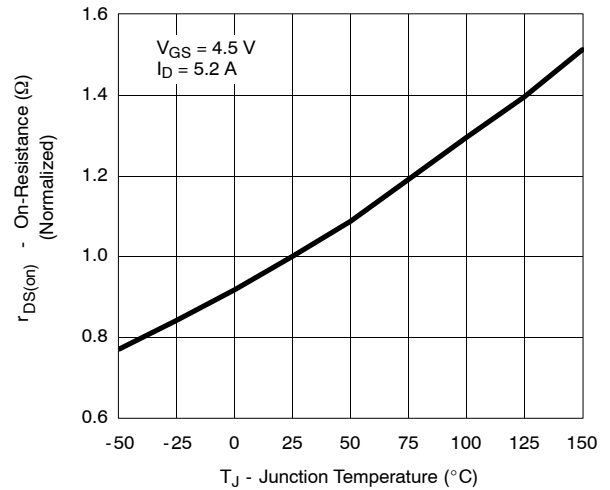
**Capacitance**



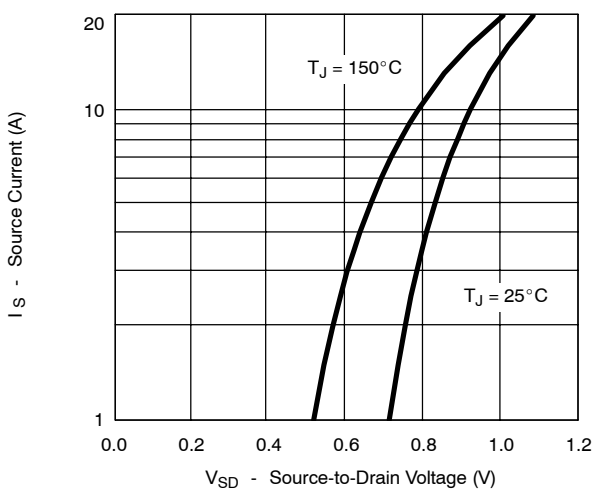
**Gate Charge**



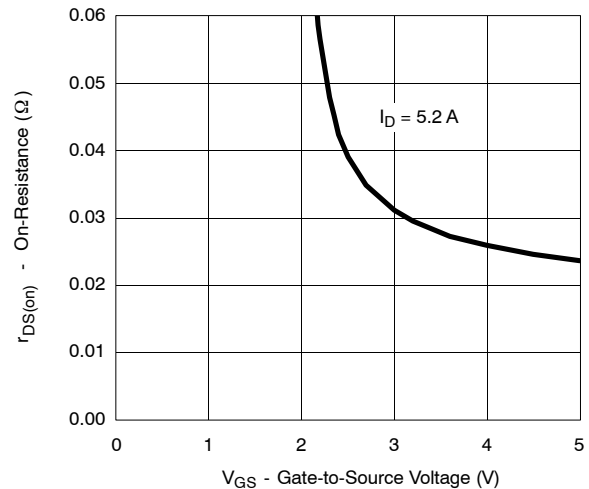
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

