

SMD Super Fast Recovery Rectifiers



CSFA101-G Thru. CSFA105-G

Reverse Voltage: 50 to 600 Volts

Forward Current: 1.0 Amp

RoHS Device

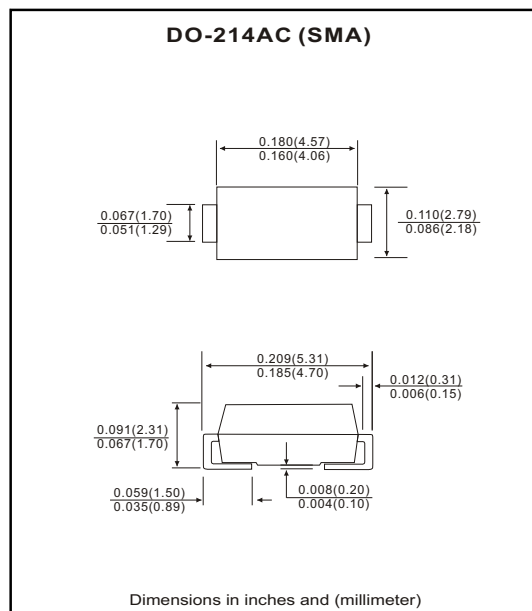


Features

- Ideal for surface mount applications.
- Easy pick and place.
- Plastic package has Underwriters Lab. flammability classification 94V-0.
- Super fast recovery time 35nS.
- Built-in strain relief.
- Low forward voltage drop.

Mechanical data

- Case: JEDEC DO-214AC, molded plastic.
- Terminals: solderable per MIL-STD-750, method 2026.
- Polarity: Color band denotes cathode end.
- Approx. weight: 0.063 grams



Maximum Ratings and Electrical Characteristics

| Parameter | Symbol | CSFA101-G | CSFA102-G | CSFA103-G | CSFA104-G | CSFA105-G | Units |
|--|-----------------|-------------|-----------|-----------|-----------|-----------|---------------|
| Max. repetitive peak reverse voltage | V_{RRM} | 50 | 100 | 200 | 400 | 600 | V |
| Max. DC blocking voltage | V_{DC} | 50 | 100 | 200 | 400 | 600 | V |
| Max. RMS voltage | V_{RMS} | 35 | 70 | 140 | 280 | 420 | V |
| Peak surge forward current, 8.3ms single half sine-wave superimposed on rate load (JEDEC method) | I_{FSM} | 30 | | | | | A |
| Max. average forward current | I_o | 1.0 | | | | | A |
| Max. instantaneous forward voltage at 1.0A | V_F | 0.95 | | 1.25 | | 1.5 | V |
| Reverse recovery time | T_{rr} | 35 | | | | | nS |
| Max. DC reverse current at $T_A=25^{\circ}C$ rated DC blocking voltage $T_A=100^{\circ}C$ | I_R | 5.0 | | | 100 | | μA |
| Max. thermal resistance (Note 1) | $R_{\theta JL}$ | 35 | | | | | $^{\circ}C/W$ |
| Max. operating junction temperature | T_J | 150 | | | | | $^{\circ}C$ |
| Storage temperature | T_{STG} | -55 to +150 | | | | | $^{\circ}C$ |

Notes: 1. Thermal resistance from junction to lead mounted on P.C.B. with 8.0x8.0 mm² copper pad area.

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RATING AND CHARACTERISTIC CURVES (CSFA101-G thru CSFA105-G)

Fig.1 Reverse Characteristics

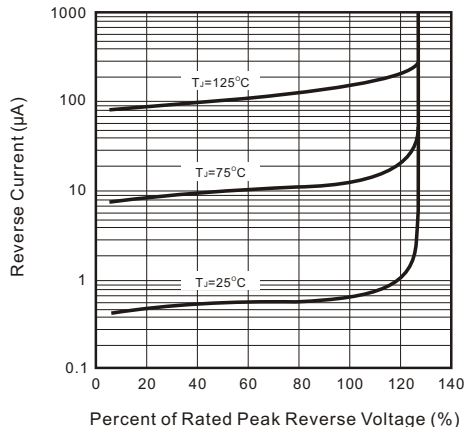


Fig.2 Forward Characteristics

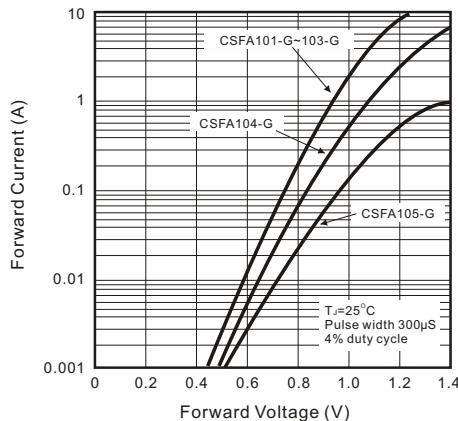


Fig.3 Junction Capacitance

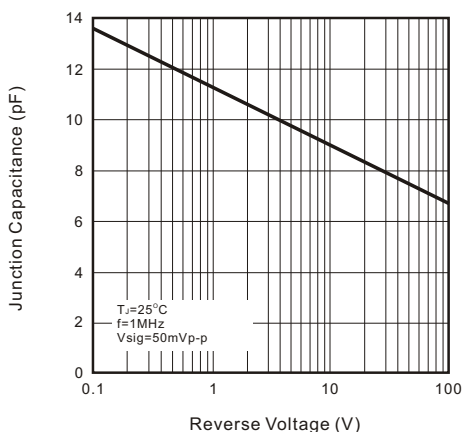


Fig.4 Non-repetitive Forward Surge Current

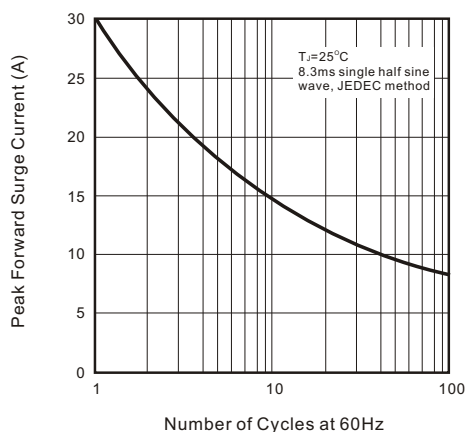


Fig.5 Test Circuit Diagram and Reverse Recovery Time Characteristics

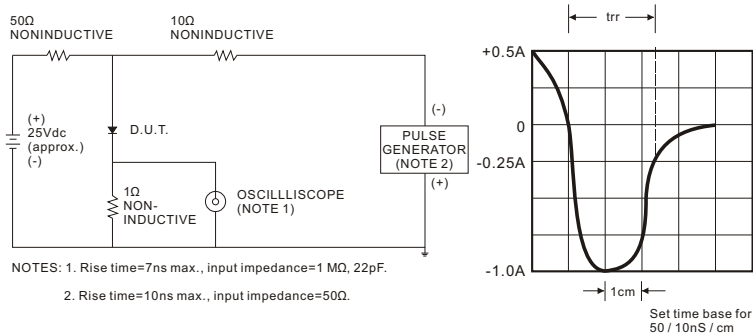


Fig.6 Current Derating Curve

