C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H074P/F

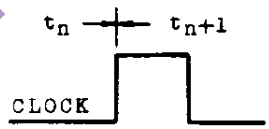
TC40H074 DUAL D-TYPE FLIP-FLOP WITH PRESET AND CLEAR

The TC40H074 is a D-type flip-flop containing two circuits which permits clear and preset operations.

*1 ... Set $\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ to "H" level.

D-MODE (*1)

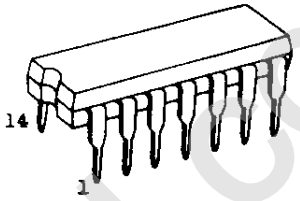
t_n	$t_n + 1$	
D	Q	$\overline{Q}$
L	L	H
H	H	L



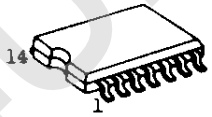
R-S MODE (*2)

INPUTS		OUTPUTS	
CLEAR	PRESENT	$\overline{Q}$	Q
H	L	L	H
L	H	H	L
L	L	H	H
H	H	D - MODE	

*2 ... Set D and CLOCK to "H" or "L" level.

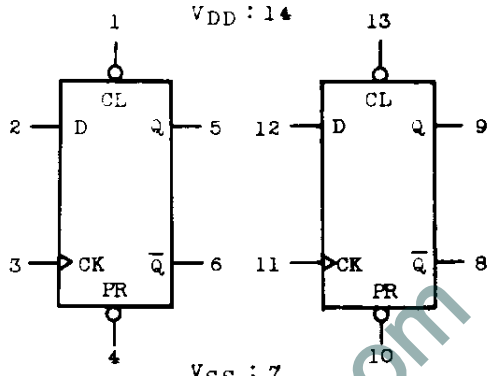


DIP14(3D14A-P)



MFP14(F14GB-P)

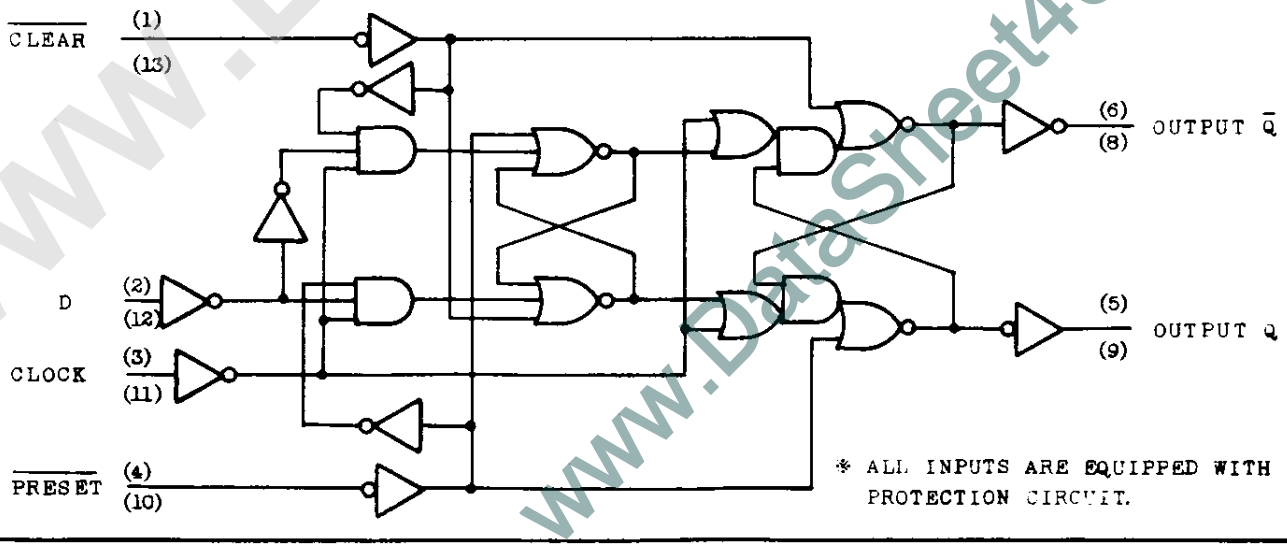
BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temp./Time	T_{sol}	260°C • 10 sec	

LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0.0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4,95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IH}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage "H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OH}=4.5V V_{OL}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Input Voltage "L" Level	V_{IL}		5	-	1.0	-		1.0	-	1.0	V
Input Current "H" Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	10^{-2}	5.0	-	25.0	μA

*All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		5	-	27	40	ns
Output Fall Time		t_{of}		5	-	27	40	ns
Propagation Delay Time	(Low-High)	t_{pLH}	CLOCK-Q, $\overline{Q}$	5	-	49	72	ns
	(High-Low)	t_{pHL}		5	-	43	65	ns
	(Low-High)	t_{pLH}	$\overline{CLEAR}$ / $\overline{PRESET}$ -Q, $\overline{Q}$	5	-	33	50	ns
	(High-Low)	t_{pHL}		5	-	59	88	ns
Min. Pluse Width		t_W	$\overline{CLEAR}$, $\overline{PRESET}$	5		20	32	ns
Max. Clock Rise Time		$t_{r\phi}$	CLOCK	5	1.0	-	-	μs
Max. Clock Fall Time		$t_{f\phi}$						
Min. Data Setup Time		t_{set-up}	D-CLOCK	5	-	16	25	ns
Min. Data Hold Time		t_{hold}	CLOCK-D	5	-	-	0	ns
Max. Clock Frequency		$f_{MAX\phi}$		5	10	20	-	MHz
Input Capacitance		C_{IN}			-	5		pF
Clear and Preset Removal Time		t_{rem}		5	-	19	35	ns

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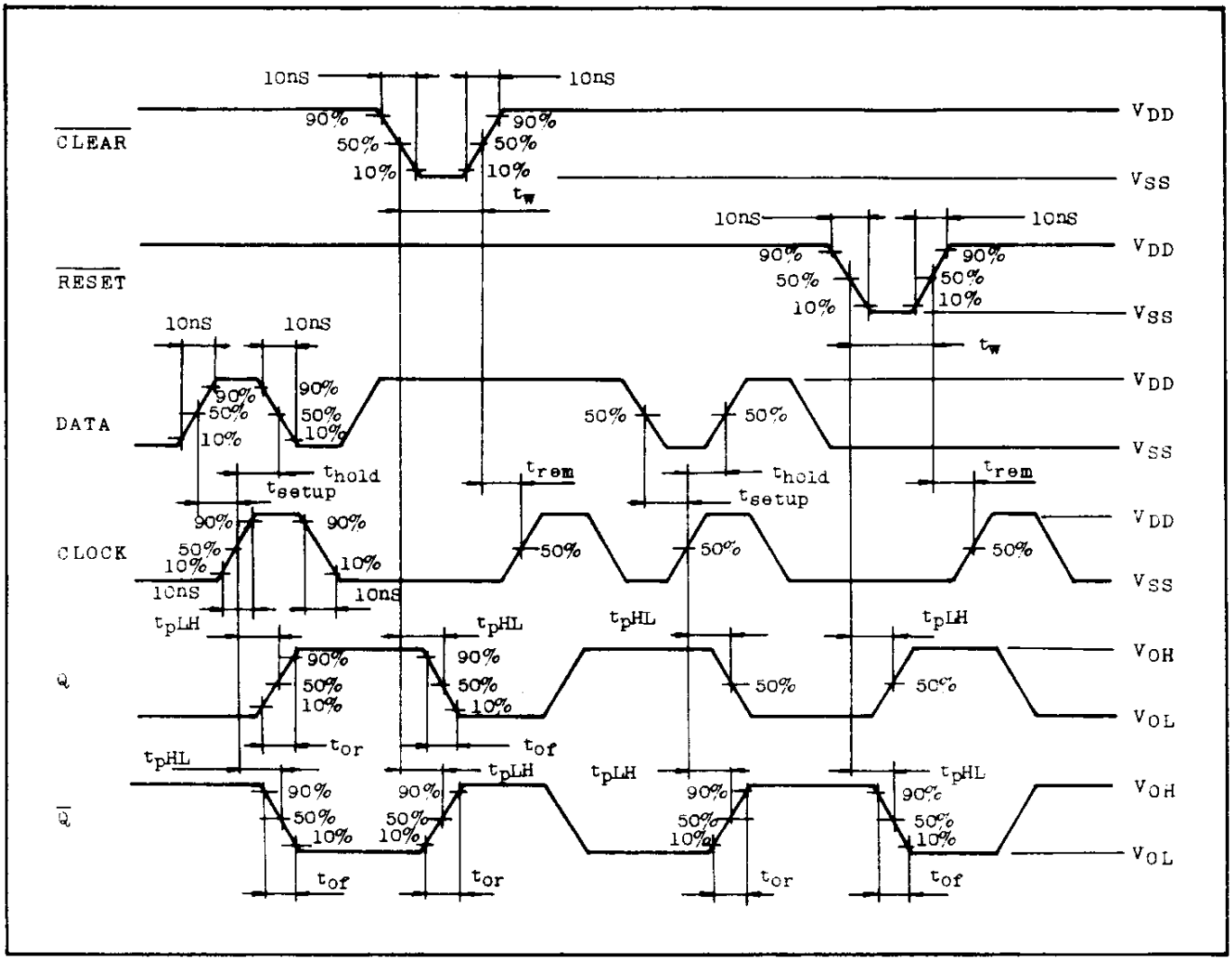
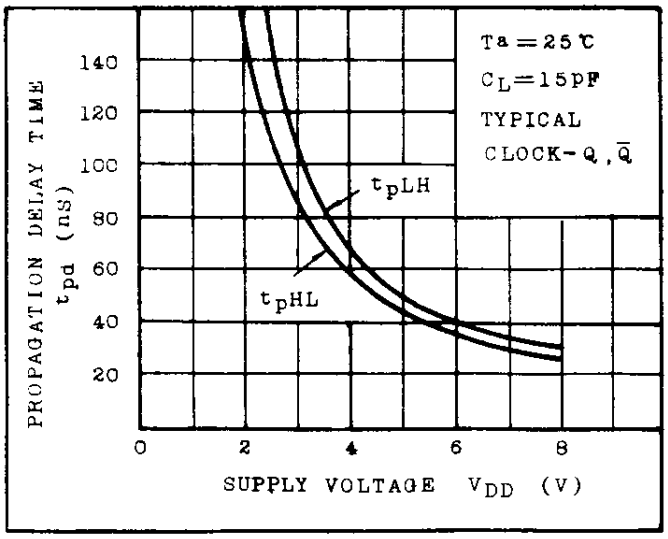
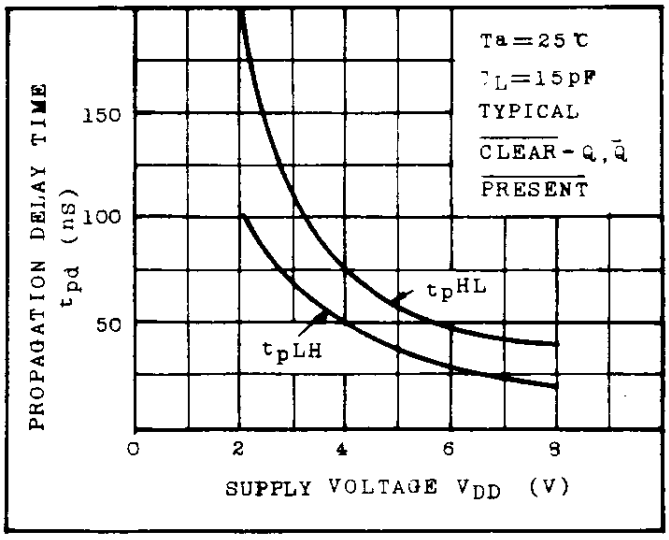
SWITCHING TIME TEST WAVEFORM



t_{pd} - V_{DD}



t_{pd} - V_{DD}



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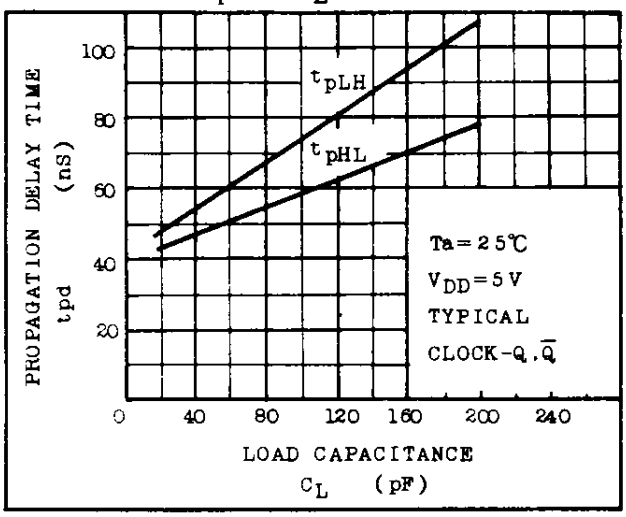
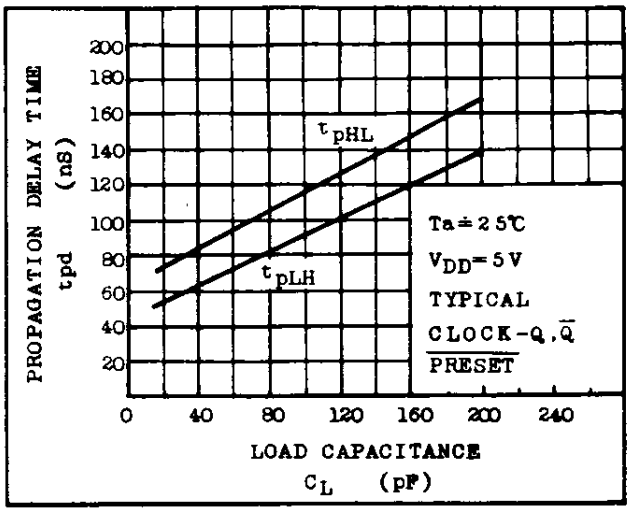
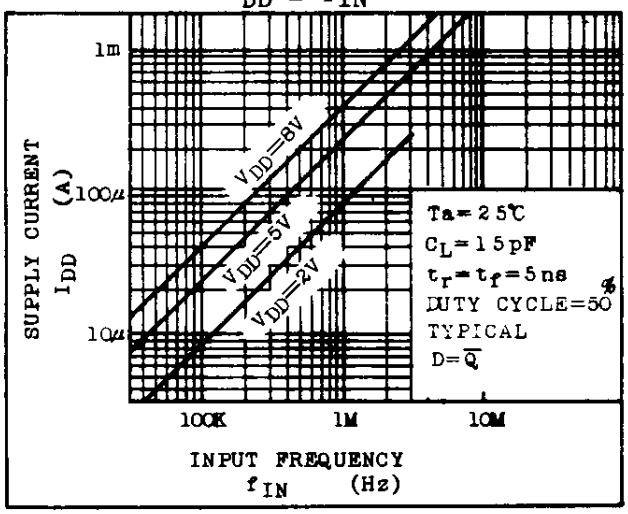
t_{pd} - C_L



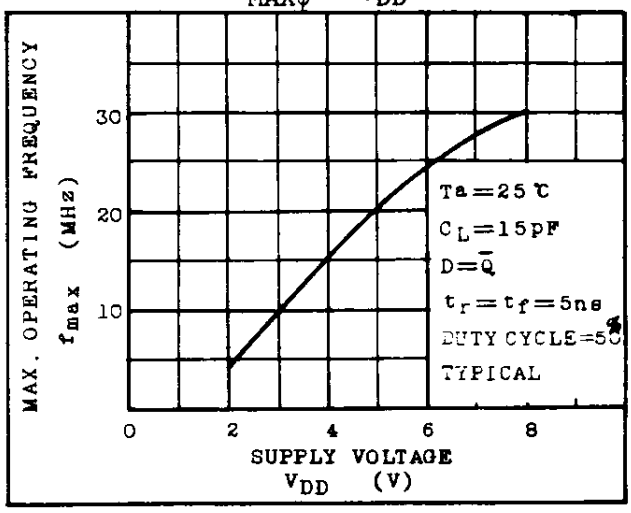
t_{pd} - C_L



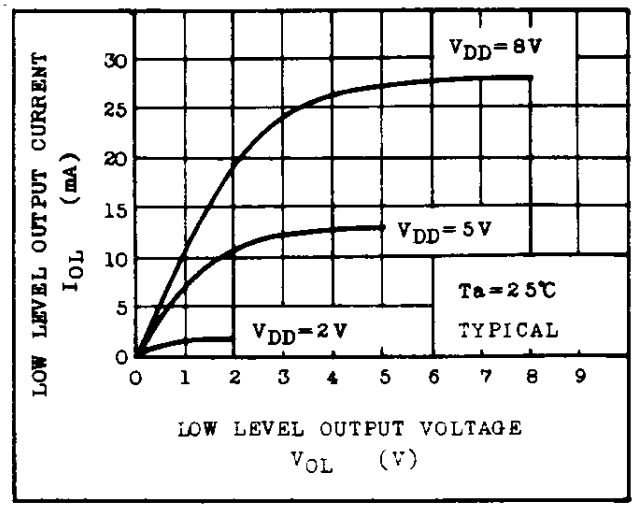
I_{DD} - f_{IN}



$f_{MAX\phi}$ - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})