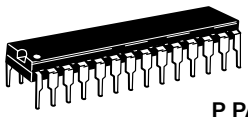
MCM6265C

8K x 9 Bit Fast Static RAM

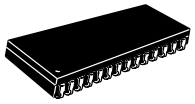
The MCM6265C is fabricated using Motorola's high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual–in–line and plastic small–outline J–leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 110 – 150 mA Maximum AC
- Fully TTL Compatible — Three State Output

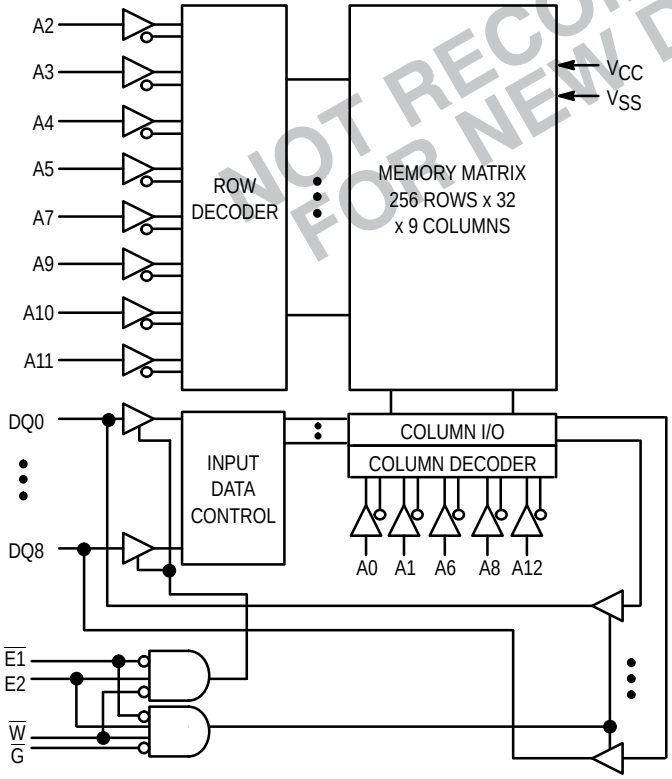


P PACKAGE
300 MIL PLASTIC
CASE 710B–01

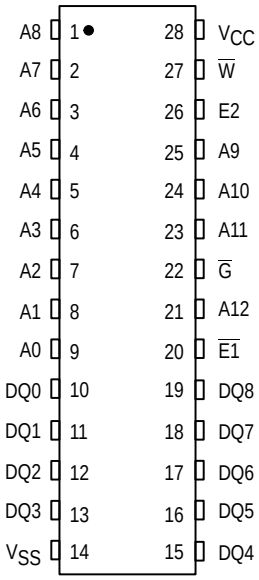


J PACKAGE
300 MIL SOJ
CASE 810B–03

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A12	Address Input
DQ0 – DQ8	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

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TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	H	Output Disabled	I_{CCA}	High–Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	– 12	– 15	– 20	– 25	– 35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	130	120	110	mA
AC Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{CC} = Max, f = f_{max})	I_{SB1}	45	40	35	30	30	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	– 12		– 15		– 20		– 25		– 35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	12	—	15	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	—	11	—	12	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Enable High to Output High–Z	t_{EHQZ}	0	6	0	8	0	9	0	10	0	11	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	5,6,7
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	0	9	0	10	ns	5,6,7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

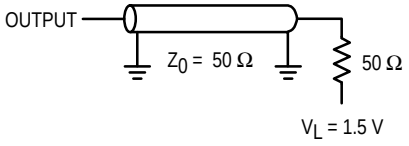


Figure 1A

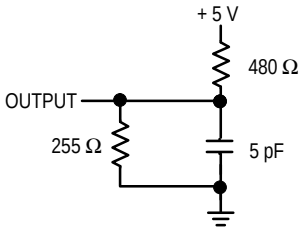
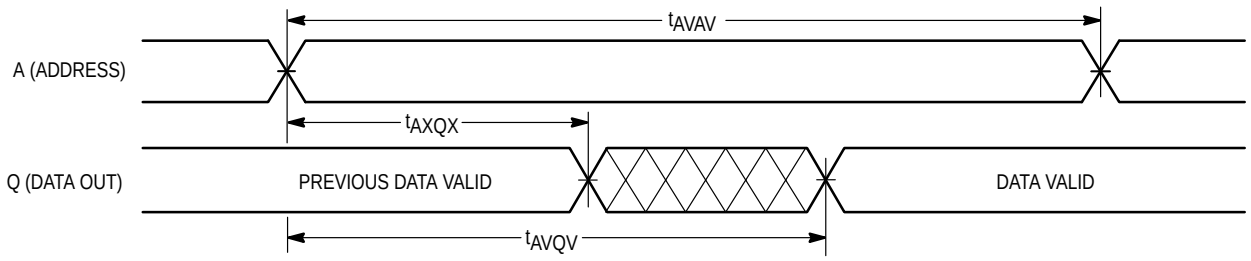


Figure 1B

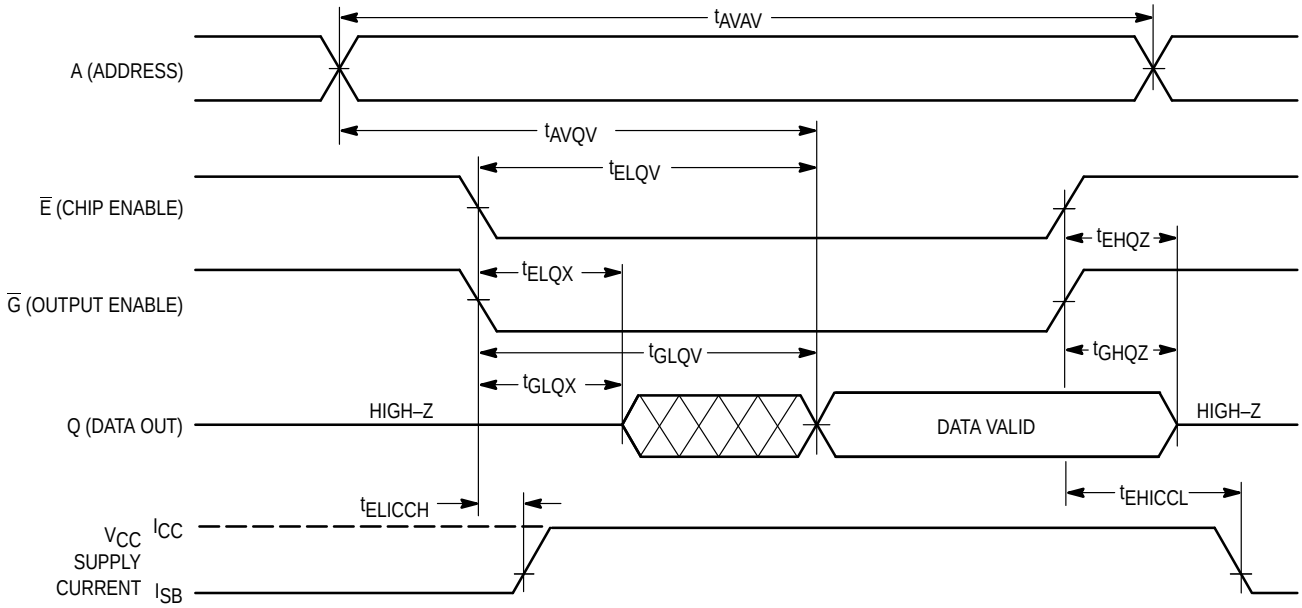
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

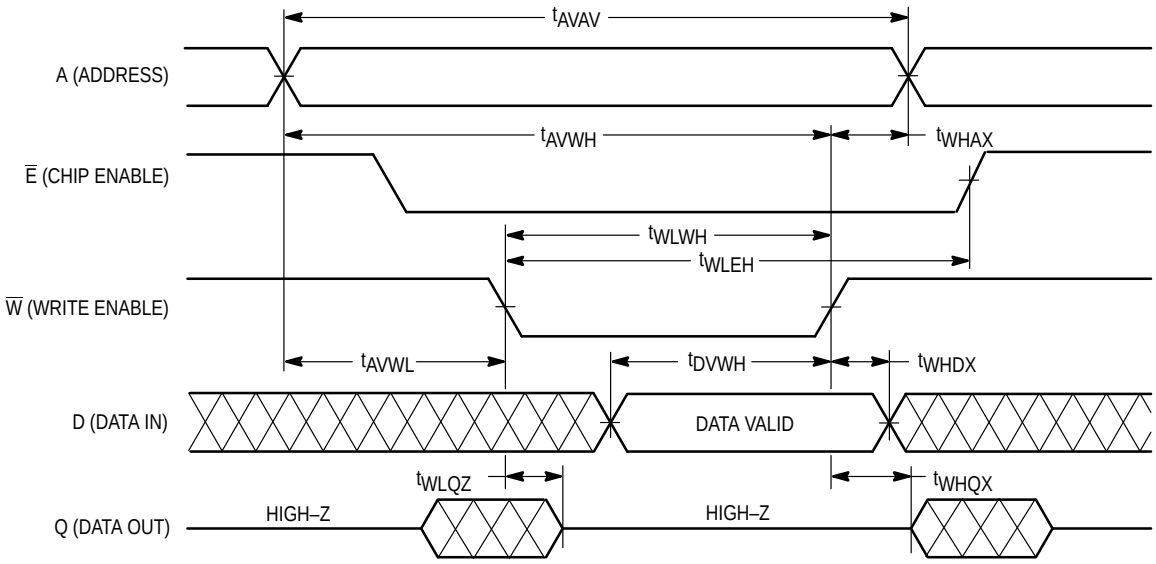


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	– 12		– 15		– 20		– 25		– 35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	8	—	10	—	12	—	15	—	17	—	ns	5
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	6	0	7	0	8	0	10	0	12	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

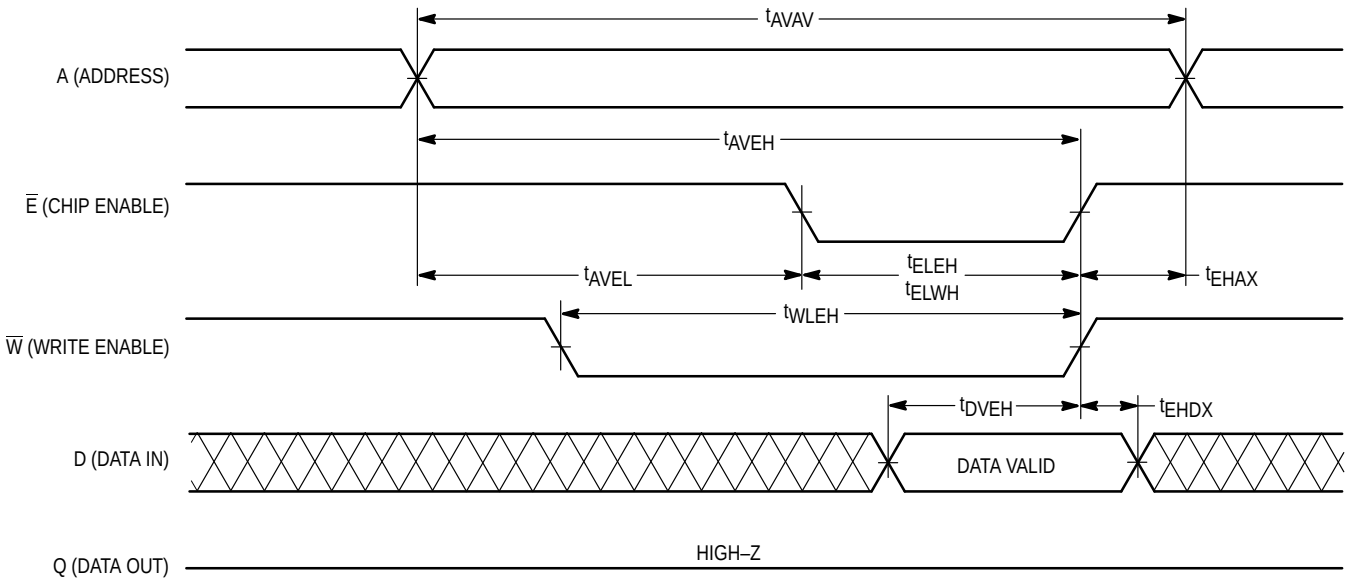


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	– 12		– 15		– 20		– 25		– 35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	12	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	10	—	12	—	15	—	25	—	ns	4, 5
Write Pulse Width	t_{WLEH}	10	—	12	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

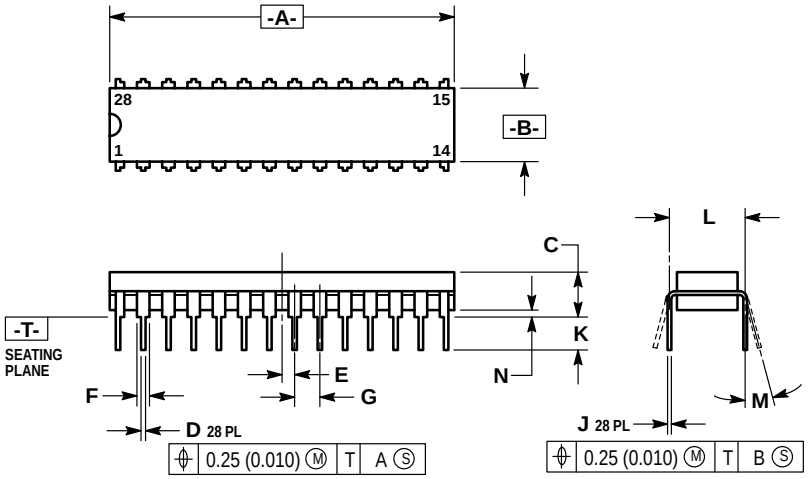
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



PACKAGE DIMENSIONS

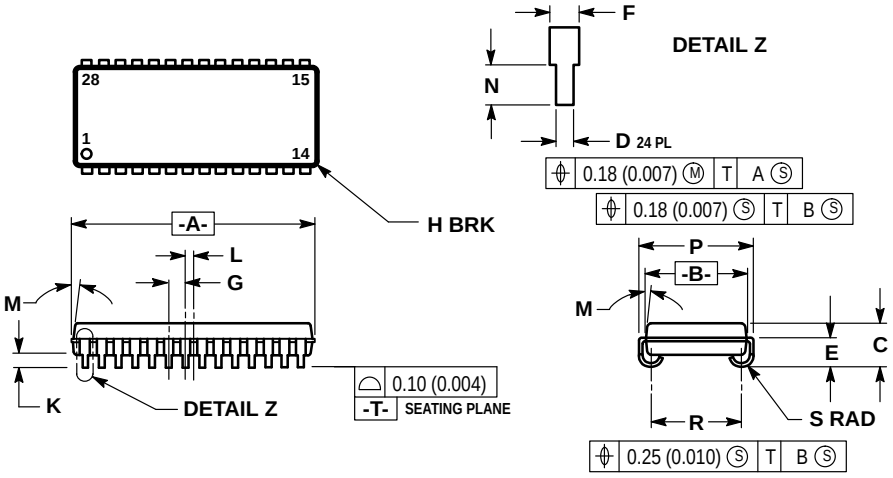
28 LEAD
300 MIL PDIP
CASE 710B–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	34.55	34.79	1.360	1.370
B	7.12	7.62	0.280	0.300
C	3.81	4.57	0.150	0.180
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	3.18	3.42	0.125	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

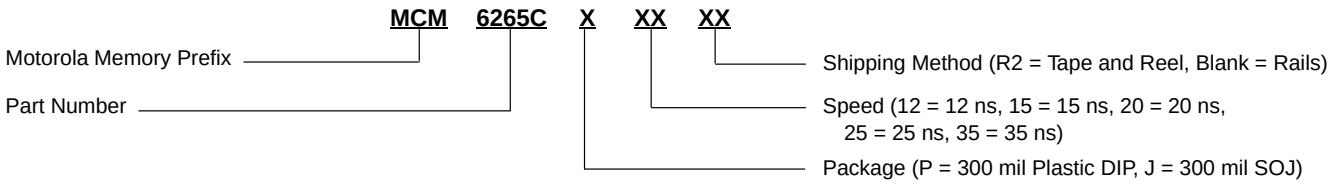
28 LEAD
300 MIL SOJ
CASE 810B–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. 810B-01 AND -02 OBSOLETE, NEW STANDARD 810B-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	10°	0°	10°
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —			
	MCM6265CP12	MCM6265CJ12	MCM6265CJ12R2
	MCM6265CP15	MCM6265CJ15	MCM6265CJ15R2
	MCM6265CP20	MCM6265CJ20	MCM6265CJ20R2
	MCM6265CP25	MCM6265CJ25	MCM6265CJ25R2
	MCM6265CP35	MCM6265CJ35	MCM6265CJ35R2

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