Ordering number: 2909A

Thick Film Hybrid IC

STK4048XI

AF Power Amplifier (Split Power Supply) (150W min, THD = 0.008%)

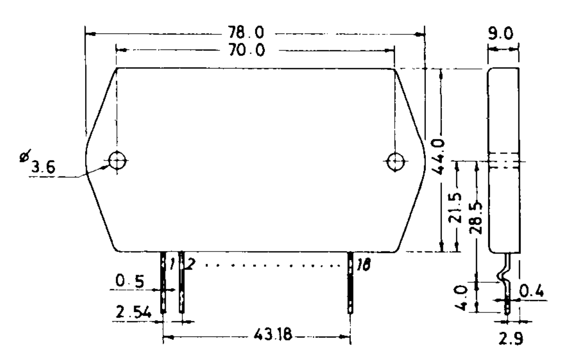
Features

- The use of a current mirror circuit, cascode circuit, pure complementary circuit provides low distortion (THD= 0.008%/100kHz LPF ON).
- Possible to design electronic supplementary circuits (pop noise muting at the time of power ON/OFF, load short protector, thermal shutdown)

Package Dimensions

unit: mm

4051A



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		±87	V
Thermal resistance	θj-c	Per power Transistor	1.2	°C/W
Junction temperature	Tj		150	°C
Operating substrate temperature	T_C		125	°C
Storage temperature	Tstg		–30 to +125	°C

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		±60	V
Load resistance	R_L		8	Ω

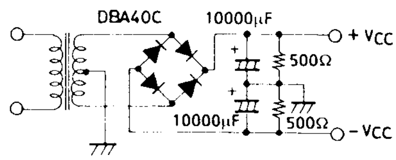
SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Operating Characteristics at Ta = 25°C, V_{CC} = ±60V, R_L = 8Ω, VG = 40dB, Rg = 600Ω, 100kHz LPF ON, R_L : noninductive load

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	Icco	V_{CC} = ±72V	15		120	mA
Output power	Po	THD = 0.008%, f = 20Hz to 20kHz	150			W
Total harmonic distortion	THD	Po = 1.0W, f = 1kHz			0.008	%
Frequency response	f_L, f_H	Po = 1.0W, $^{+0}_{-3}$ dB		20 to 50k		Hz
Input impedance	r_i	Po = 1.0W, f = 1kHz		55		kΩ
Output noise voltage	V_{NO}*	V_{CC} = ±72V, Rg = 10kΩ			1.2	mVrms
Neutral voltage	V_N	V_{CC} = ±72V	–70	0	+70	mV

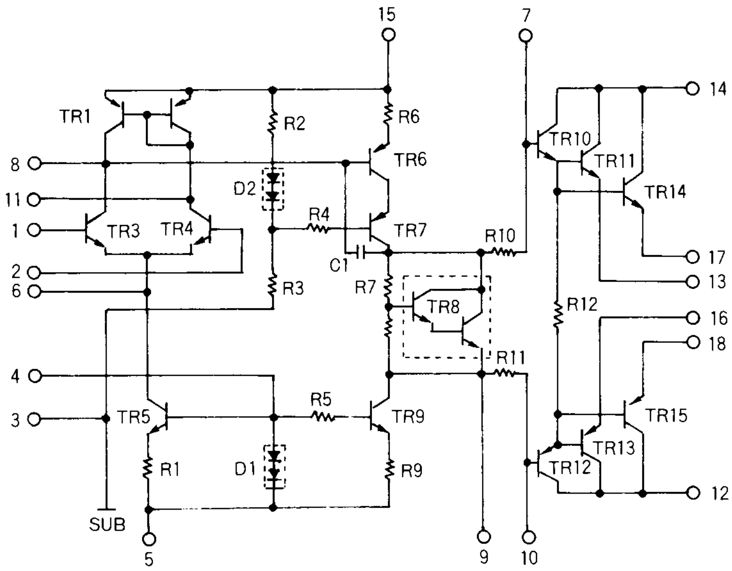
Notes. For power supply at the time of test, use a constant-voltage power supply unless otherwise specified.

*The output noise voltage is represented by the peak value on rms scale (VTVM) of average value indicating type. The noise voltage waveform includes no flicker noise. For measurement of the output noise voltage, use the specified transformer power supply shown right.

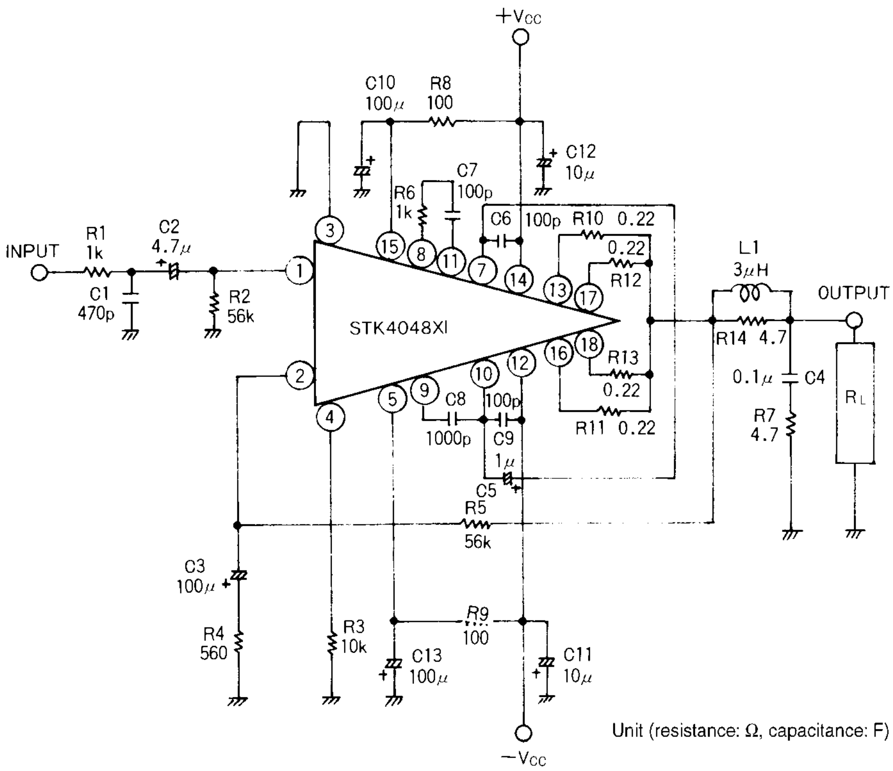


Specified Transformer Power Supply
(Equivalent to MG250)

Equivalent Circuit

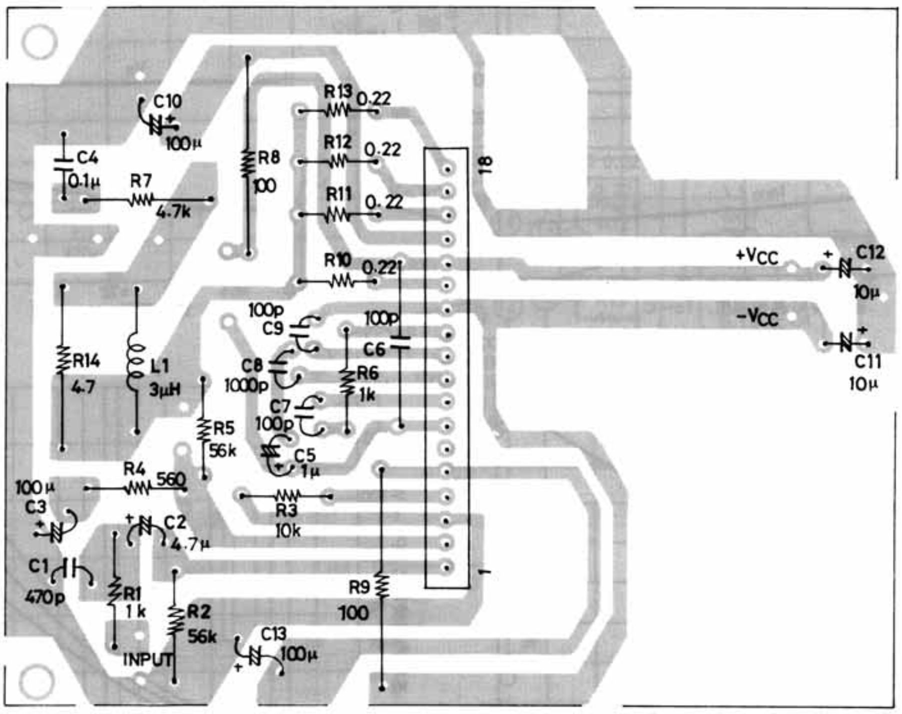


Sample Application Circuit: 150W min Single-Channel AF Power Amplifier

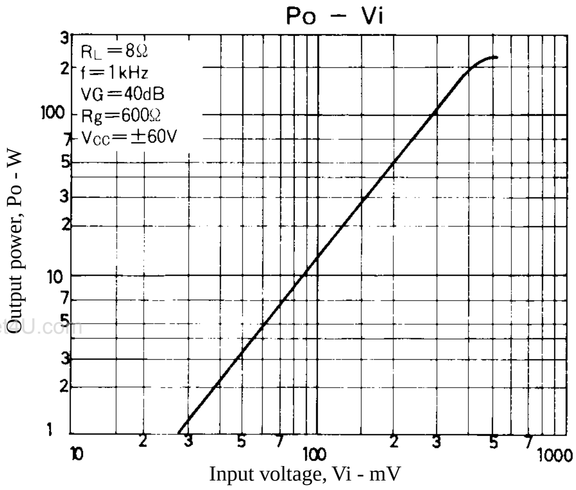


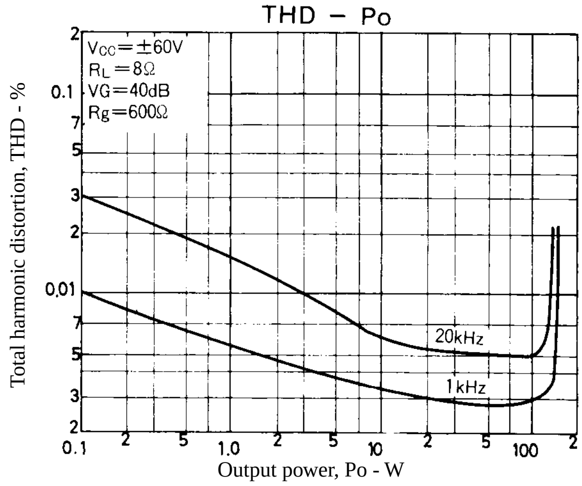
Unit (resistance: Ω, capacitance: F)

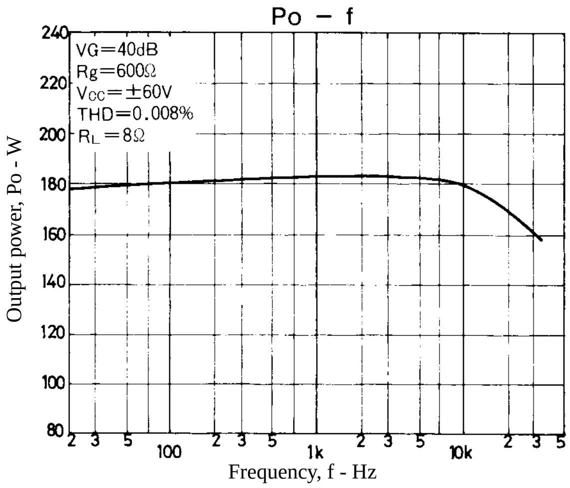
Sample Printed Circuit Pattern for Application Circuit (Cu-foiled side)

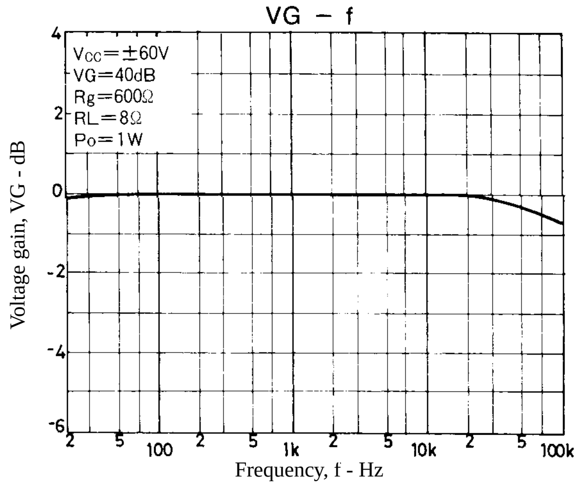


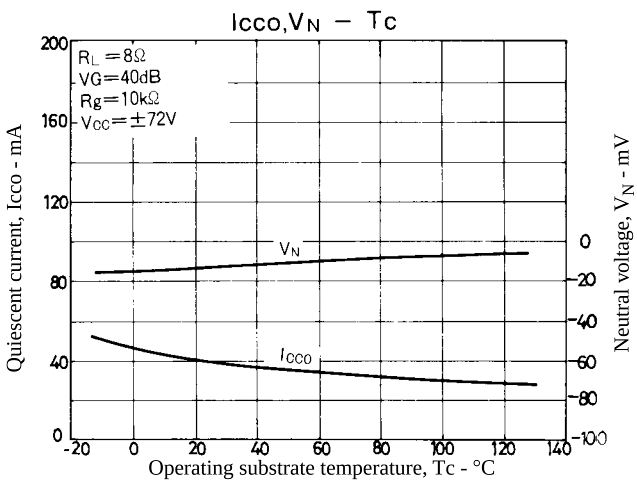
Unit (resistance: Ω, capacitance: F)

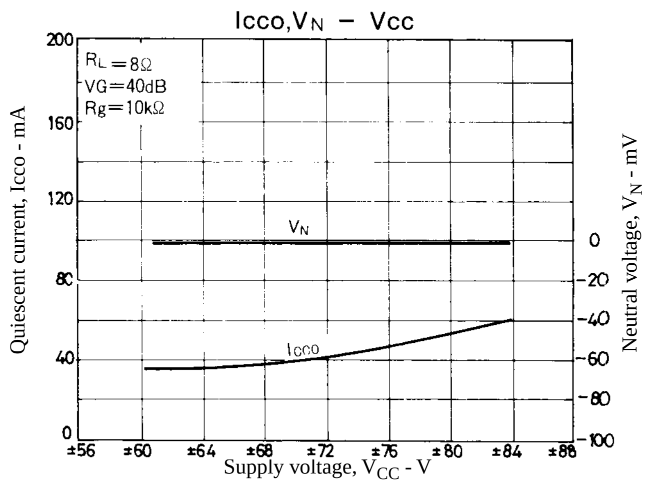

Po − Vi
RL = 8Ω
f = 1kHz
VG = 40dB
Rg = 600Ω
VCC = ±60V
Output power, Po - W
Input voltage, Vi - mV

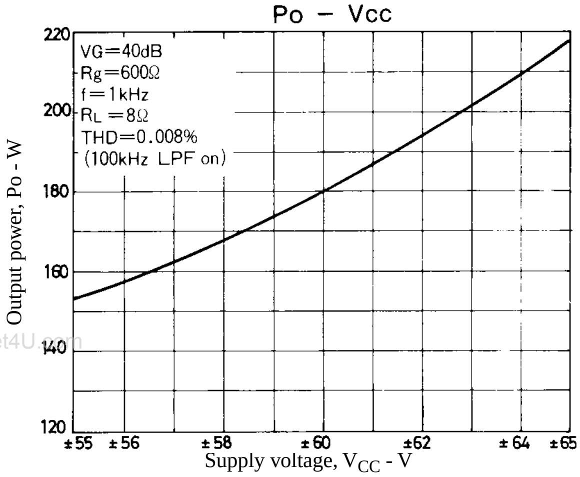

THD − Po
VCC = ±60V
RL = 8Ω
VG = 40dB
Rg = 600Ω
20kHz
1kHz
Total harmonic distortion, THD - %
Output power, Po - W

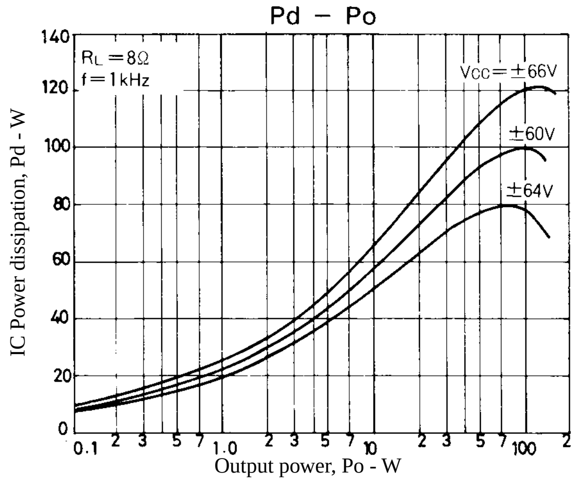

Po − f
VG = 40dB
Rg = 600Ω
VCC = ±60V
THD = 0.008%
RL = 8Ω
Output power, Po - W
Frequency, f - Hz

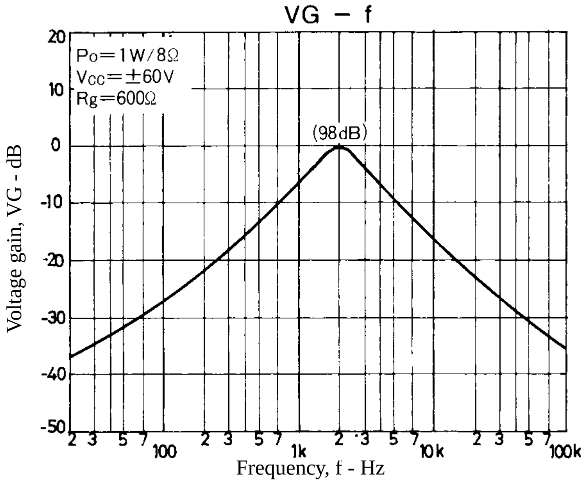

VG − f
VCC = ±60V
VG = 40dB
Rg = 600Ω
RL = 8Ω
Po = 1W
Voltage gain, VG - dB
Frequency, f - Hz


Icco, VN − Tc
RL = 8Ω
VG = 40dB
Rg = 10kΩ
VCC = ±72V
VN
Icco
Quiescent current, Icco - mA
Neutral voltage, VN - mV
Operating substrate temperature, Tc - °C

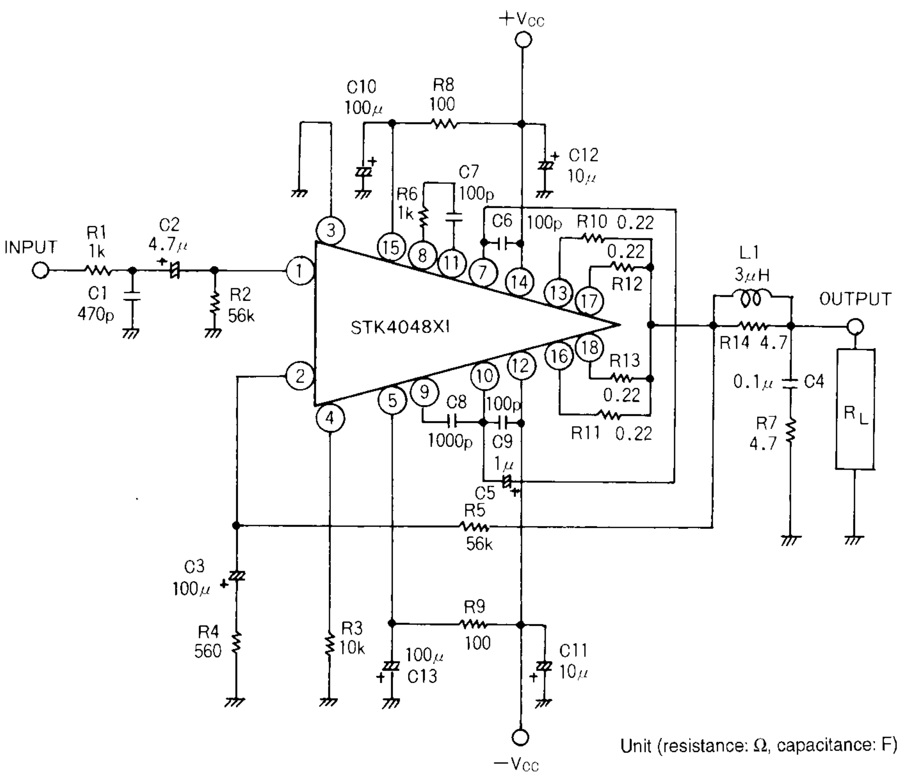

Icco, VN − Vcc
RL = 8Ω
VG = 40dB
Rg = 10kΩ
VN
Icco
Quiescent current, Icco - mA
Neutral voltage, VN - mV
Supply voltage, VCC - V





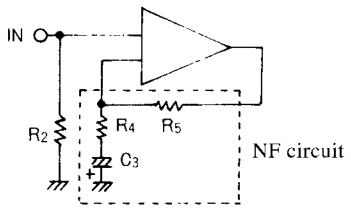


Description of External Parts



Unit (resistance: Ω, capacitance: F)

R1, C1	Input filter circuit • Used to reduce noise at high frequencies.
C2	Input coupling capacitor • Used to block DC current. When the reactance of the capacitor increases at low frequencies, the dependence of 1/f noise on signal source resistance causes the output noise to worsen. It is better to decrease the reactance.
R2	Input bias resistor • Used to bias the input pin to zero. • Affects V_N stability. (See NF circuit.) • Because of differential input, this resistor fixes the input resistance practically.

R4, R5
C3 (C2)
	NFB circuit (AC NF circuit). It is desirable that the error of the resistor value is 1% or less.
	
	
	C3 : Capacitor for AC NF
	R4, R5 : Used to set VG
	• VG setting obtained by using R4, R5 .... $VG = \log 20 \cdot \frac{R_5}{R_4}$ (40dB is recommended)
	• Low cutoff frequency setting obtained by using, R4, C3. .... $f_L = \frac{1}{2\pi \cdot R_4 \cdot C_3}$ (Hz)
	• Change of VG setting
	  • It is desirable to change R4. In this case, the low cutoff frequency setting needs to be rechecked.
	  • When VG setting is changed by changing R5, R5 must be made equal to R2 to ensure V_N balance. If the resistor value is increased more than the existing value, it may be hard to ensure V_N balance and the temperature characteristic of V_N may be also deteriorated.

R3	First-stage constant-current bias resistor
R6, C7	Used for oscillation blocking and phase compensation
R7, C4	Used for oscillation blocking and phase compensation (C4 : A polyester film capacitor is recommended.)
C6, C9	Used for oscillation blocking and phase compensation (Must be connected near the pin) C6 : Power amp on (+) side C9 : Power amp on (–) side
C4	Used for oscillation blocking and phase compensation (Used for oscillation blocking before clip)
C5	Used for oscillation blocking and distortion improvement
C8, C10	Ripple filter circuit on (+) side
R9, C13	Ripple filter circuit on (–) side
C11, C12	Used for oscillation blocking • Used to decrease the power supply impedance to operate the IC stably. Must be connected near the IC pin. It is desirable to use an electrolytic capacitor.
L1, R14	Used for oscillation blocking
R10, R11 R12, R13	Output limiting resistors

Thermal Design

The IC power dissipation of the STK4048XI at the IC-operated mode is 100W max. at load resistance 8Ω for continuous sine wave as shown in Figure 1.

In an actual application where a music signal is used, it is impractical to estimate the power dissipation based on the continuous signal as shown right, because too large a heat sink must be used. It is reasonable to estimate the power dissipation as 1/10 Po max. (EIAJ).
That is, Pd = 65W at 8Ω

Thermal resistance θc-a of a heat sink for this IC power dissipation (Pd) is fixed under conditions 1 and 2 shown below.

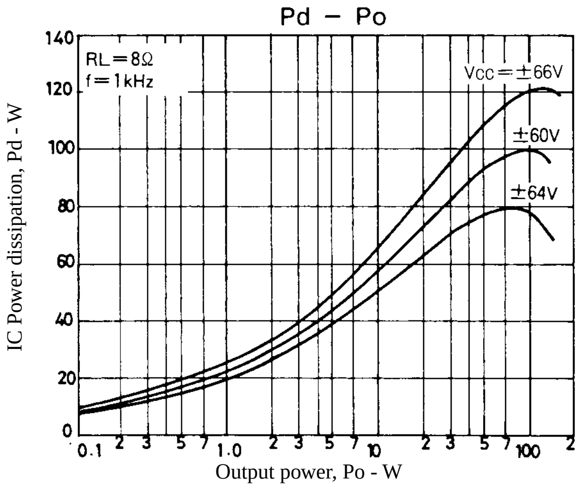


Figure 1. STK4048XI Pd – Po (R_L = 8Ω)

Condition 1: $Tc = Pd \times \theta c\text{-}a + Ta \leq 125°C$ .... (1)
where Ta : Specified ambient temperature
Tc : Operating substrate temperature

Condition 2: $T_j = Pd \times (\theta c\text{-}a) + Pd/4 \times (\theta j\text{-}c) + Ta \leq 150°C$ .... (2)
where Tj : Junction temperature of power transistor

Assuming that the power dissipation is shared equally among the four power transistors, thermal resistance θj-c is 1.2°C/W and

$$Pd \times (\theta c\text{-}a + 1.2/4) + Ta \leq 150°C \quad (3)$$

Thermal resistance θc-a of a heat sink must satisfy inequalities (1) and (3).
Figure 2 shows the relation between Pd and θc-a given from (1) and (3) with Ta as a parameter.

[Example] The thermal resistance of a heat sink is obtained when the ambient temperature specified for a stereo amplifier is 50°C.
Assuming V_{CC} = ±60V, R_L = 8Ω,
R_L = 8Ω : Pd = 65W at 1/10 Po max.
The thermal resistance of a heat sink is obtained from Figure 2.
R_L = 8Ω : θc-a1 = 1.15°C/W
Tj when a heat sink is used is obtained from (3).
R_L = 8Ω : Tj = 144.3°C

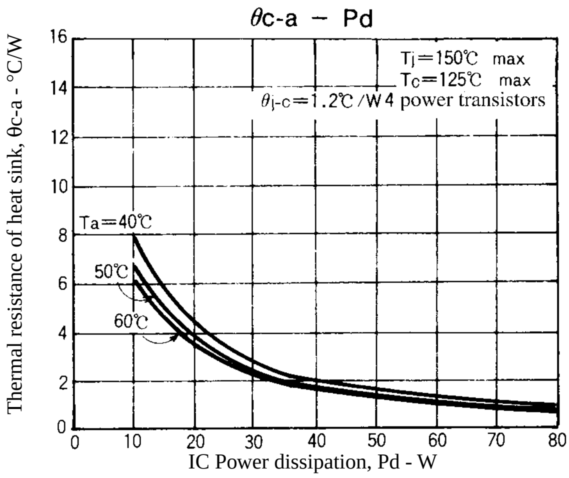


Figure 2. STK4048XI θc-a – Pd

This design is based on the use of a constant-voltage regulated power supply. Pd differs when a transformer power supply is used. Redesign must be made based on Pd that suits the regulation of each transformer.

This catalog provides information as of July, 1997. Specifications and information herein are subject to change without notice.