TOSHIBA SEMICONDUCTOR
TECHNICAL DATA

TOSHIBA GTR MODULE

MG50G2DM1

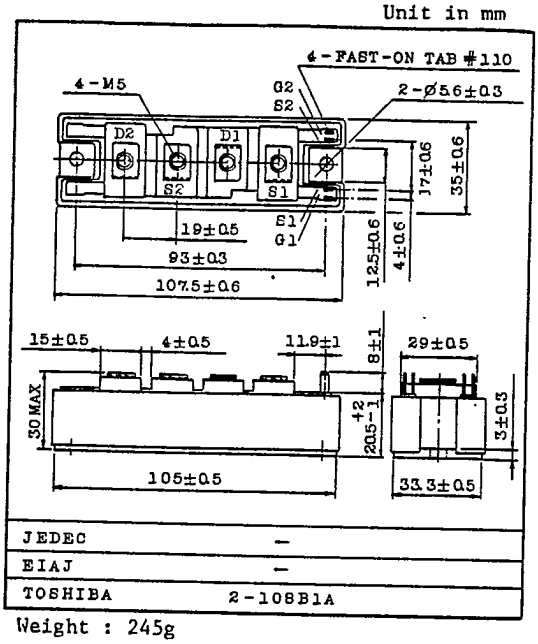
SILICON N CHANNEL MOS TYPE

HIGH POWER SWITCHING APPLICATIONS.
MOTOR CONTROL APPLICATIONS.

FEATURES:

- The Drain is Isolated from Case.
- 2 MOS FETs are Built-in to 1 Package.
- With Built-in Free Wheeling Diode.
- Low Drain-Source ON Resistance
  : $R_{DS(ON)}$=0.14Ω(Max.)(I_D=50A)
- Enhancement-Mode.

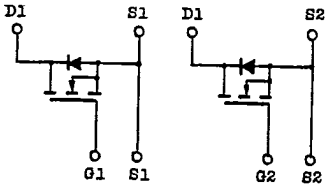
Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	2-108B1A

Weight : 245g

EQUIVALENT CIRCUIT



MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	450	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	DC	I_D	±50	A
	1ms		±100	
Drain Power Dissipation (Tc=25°C)		P_D	400	W
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-40~125	°C
Isolation Voltage		V_{Isol}	2500 (AC, 1 Minute)	V
Screw Torque (Terminal/Mounting)		-	30/30	kg·cm

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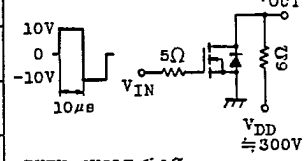
ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	±150	nA
Drain Cut-Off Current		I_{DSS}	V_{DS}=450V, V_{GS}=0	-	-	3.0	mA
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
Gate-Source Cut-off Voltage		$V_{GS(OFF)}$	V_{DS}=10V, I_D=50mA	1.8	2.8	4.0	V
Forward Transfer Admittance		$\|Y_{fs}\|$	V_{DS}=10V, I_D=50A	12.0	21.0	-	S
Drain-Source ON Resistance		$R_{DS(ON)}$	I_D=50A, V_{GS}=10V	-	0.09	0.14	Ω
Input Capacitance		C_{iss}	V_{DS}=10V, V_{GS}=0, f=1MHz	-	13000	-	pF
Switching Time	Rise Time	t_r	 DUTY CYCLE≦1%	-	350	700	ns
	Turn-on Time	t_{on}		-	400	800	
	Fall Time	t_f		-	100	200	
	Turn-off Time	t_{off}		-	650	1300	
Source Drain Forward Voltage		V_{DSF}	I_D=-50A, V_{GS}=0	-	1.15	1.95	V
Reverse Recovery Time		t_{rr}	I_D=-50A, R_G=5Ω V_{GS}=-10V, di/dt=150A/μs	-	250	500	ns
Thermal Resistance		$R_{th(ch-c)}$		-	-	0.31	°C/W

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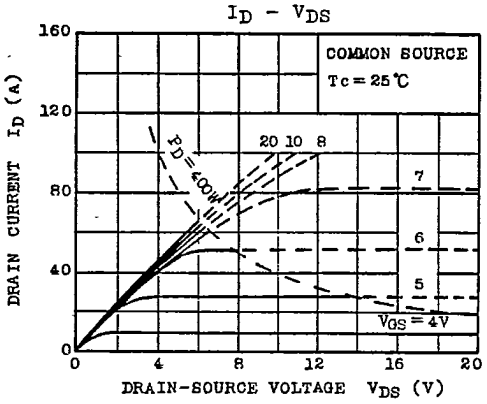
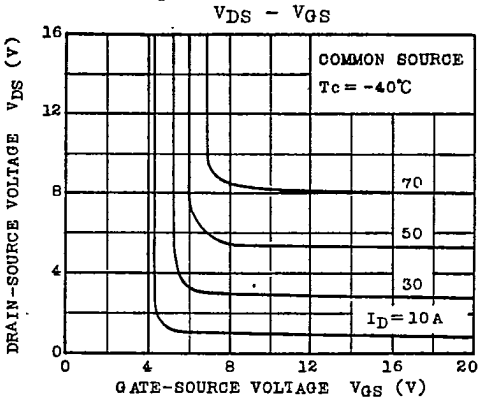
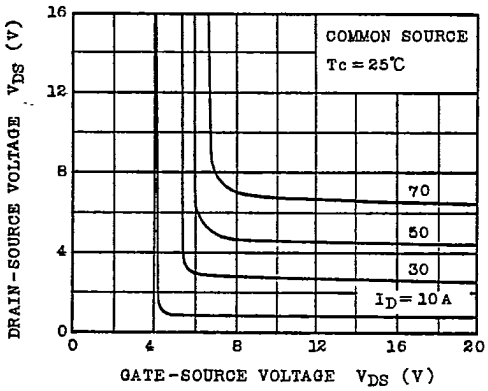
I_D – V_{DS}



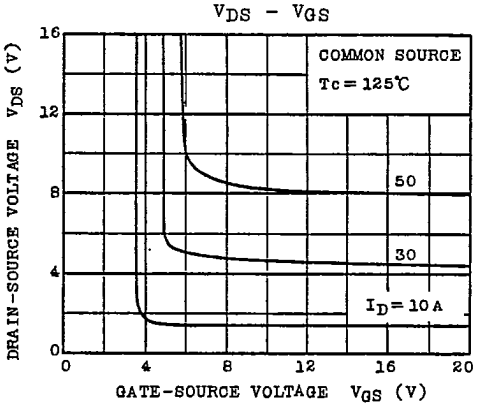
V_{DS} – V_{GS}



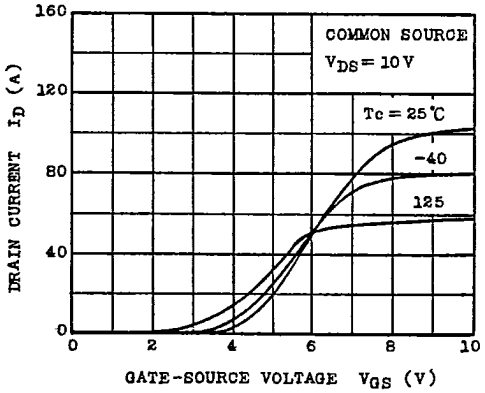
V_{DS} – V_{GS}



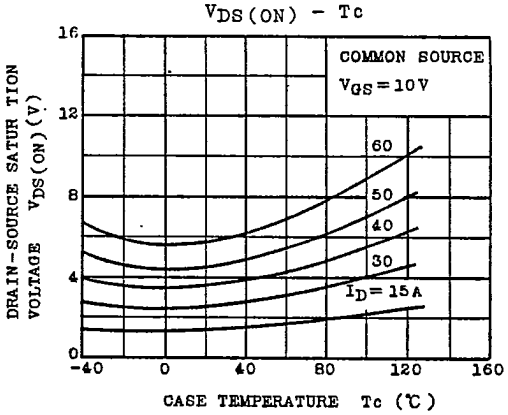
V_{DS} – V_{GS}



I_D – V_{GS}



$V_{DS(ON)}$ – Tc



MG50G2DM1-3

TOSHIBA CORPORATION

TOSHIBA SEMICONDUCTOR
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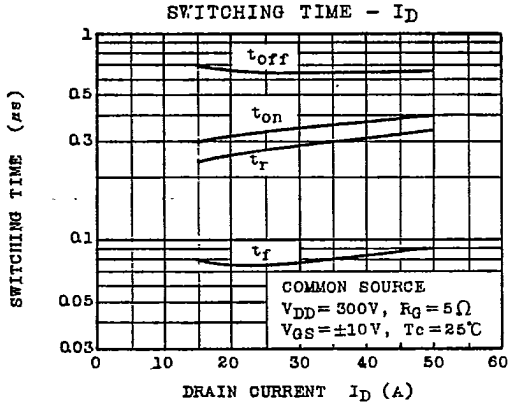
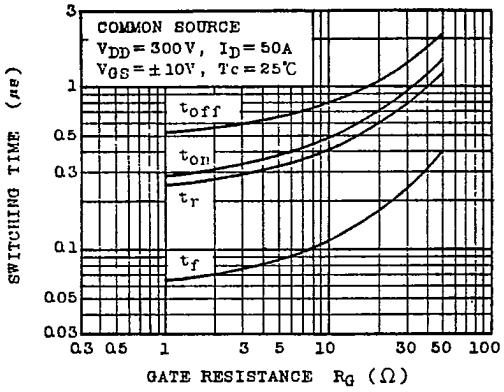
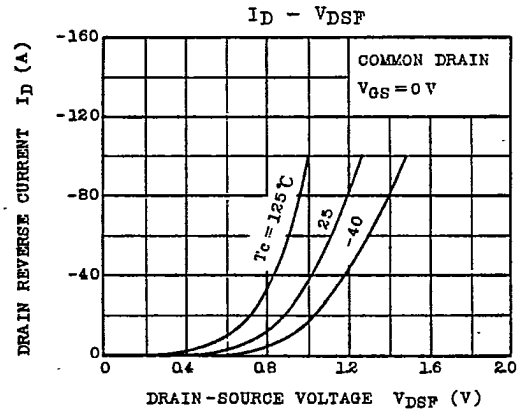
SWITCHING TIME – I_D



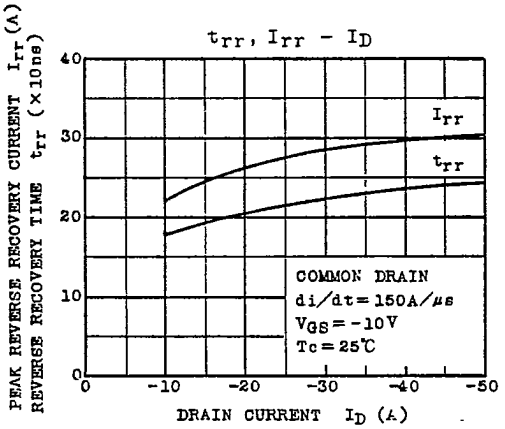
SWITCHING TIME – R_G



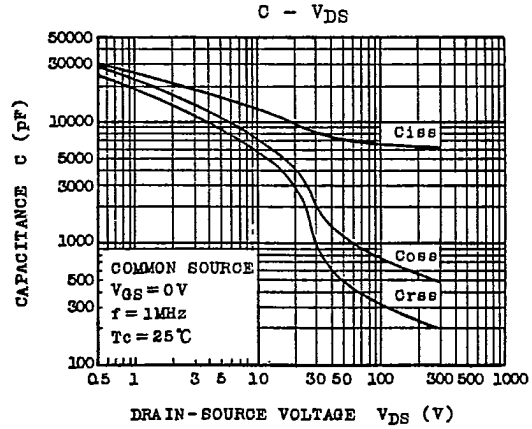
I_D – V_{DSF}



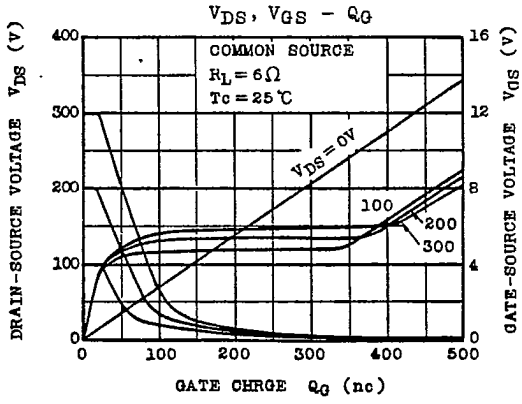
t_{rr}, I_{rr} – I_D



C – V_{DS}



V_{DS}, V_{GS} – Q_G



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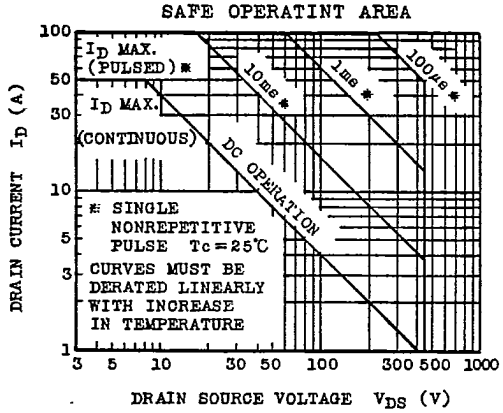
SAFE OPERATINT AREA



$R_{th(ch-c)} - t_w$