TOSHIBA

INSULATED GATE BIPOLAR TRANSISTOR

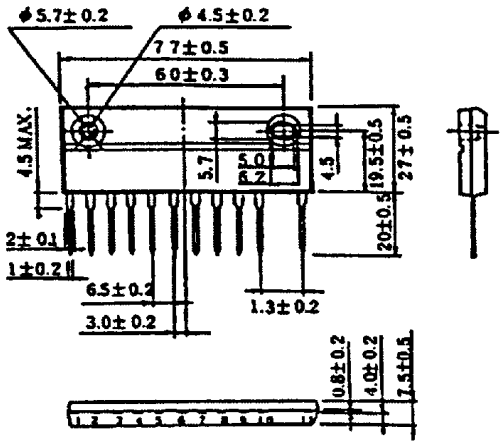
MP6753

Unit in mm

High Power Switching Applications

Motor Control Applications

- The Electrodes are Isolated from Case.
- 6 IGBTs are Built Into 1 Package.
- Enhancement-Mode
- Low Saturation Voltage
  : $V_{CE(sat)}$ = 2.7V (Max.) (I_C = 20A)
- High Speed
  : t_f = 1.0μs (Max.) (I_C = 20A)
  : t_{rr} = 0.15μs (Max.) (I_F = 20A)

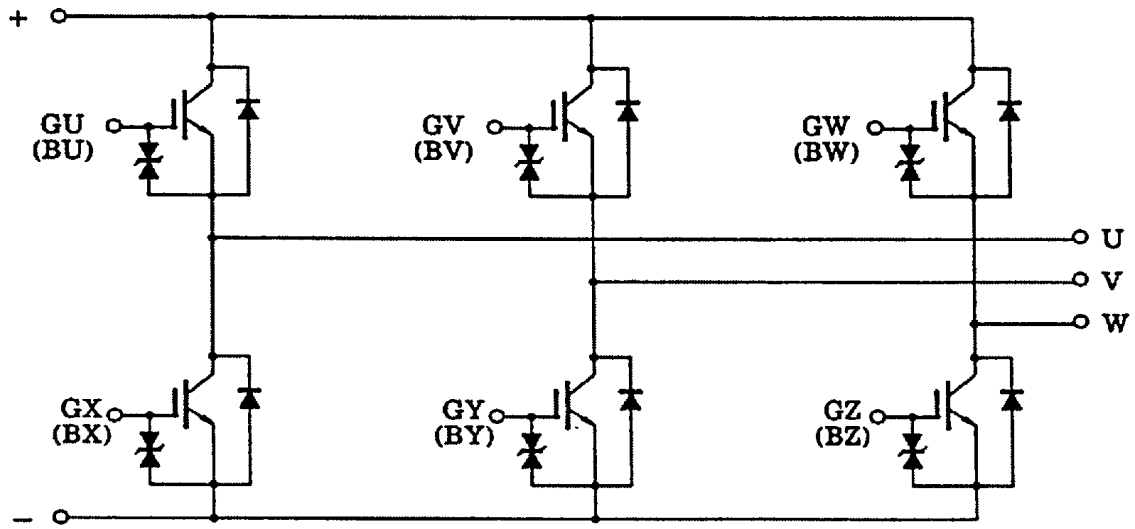


1. (+) 2. GU 3. U 4. GV 5. V 6. GW
7. W 8. GX 9. GY 10. GZ 11. (−)

JEDEC	—
EIAJ	—
TOSHIBA	2-78A1A

Weight : 44g

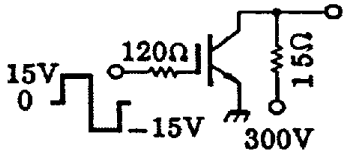
Equivalent Circuit



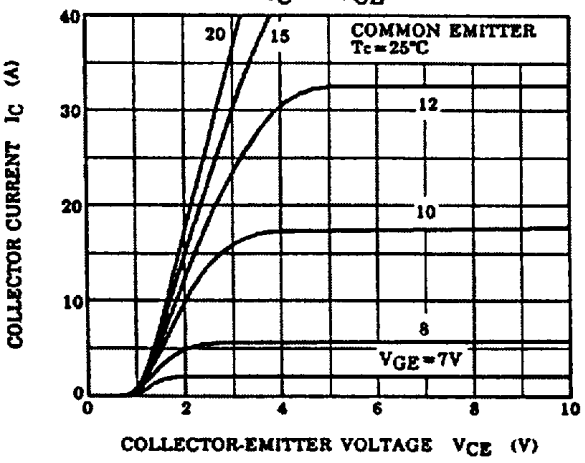
Maximum Ratings (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage		V_{CES}	600	V
Gate-Emitter Voltage		V_{GES}	±20	V
Collector Current	DC	I_C	20	A
	1ms	I_{CP}	40	
Forward Current	DC	I_F	20	A
	1ms	I_{FM}	40	
Collector Power Dissipation (Tc = 25°C)		P_C	60	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	-40 ~ 125	°C
Isolation Voltage		V_{Isol}	2500 (AC 1 minute)	V
Screw Torque		–	1.5	N•m

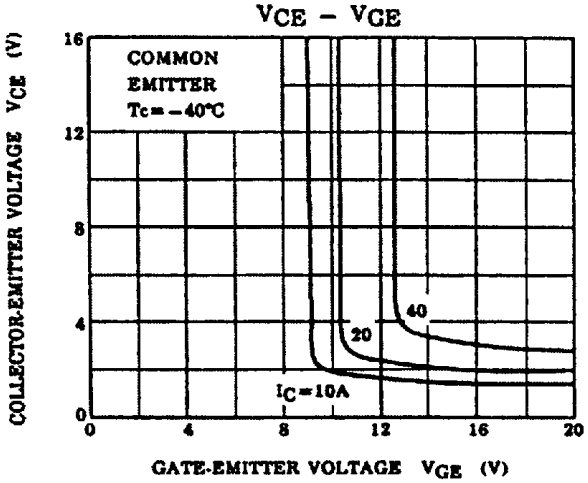
Electrical Characteristics (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MX.	UNIT
Gate Leakage Current		I_{GES}	V_{GE} = ±20V, V_{CE} = 0	–	–	±20	μA
Collector Cut-off Current		I_{CES}	V_{CE} = 600V, V_{GE} = 0	–	–	1.0	mA
Collector-Emitter Breakdown Voltage		$V_{(BR)CES}$	I_C = 10mA, B_{GE} = 0	600	–	–	V
Gate-Emitter Cut-off Voltage		$V_{GE(OFF)}$	V_{CE} = 5V, I_C = 20mA	3.0	–	6.0	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$	I_C = 20A, V_{GE} = 15V	–	2.3	2.8	V
Input Capacitance		C_{ies}	V_{CE} = 10V, V_{GE} = 0, f = 1MHz	–	1300	–	pF
Switching Time	Rise Time	t_r		–	0.3	0.6	μs
	Turn-on Time	t_{on}		–	0.4	0.8	
	Fall Time	t_f		–	0.6	1.0	
	Turn-off Time	t_{off}		–	1.0	1.6	
Forward Voltage		V_F	I_F = 15A, V_{GE} = 0	–	1.7	2.5	V
Reverse Recovery Time		t_{rr}	I_F = 20A, V_{GE} = -10V di/dt = 50A/μs	–	0.08	0.15	μs
Thermal Resistance		$R_{th(j-c)}$	Transistor	–	–	2.08	°C/W
			Diode	–	–	3.09	

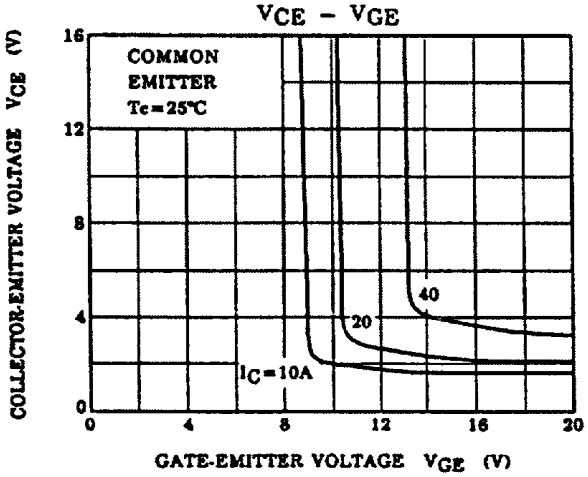
I_C – V_{CE}



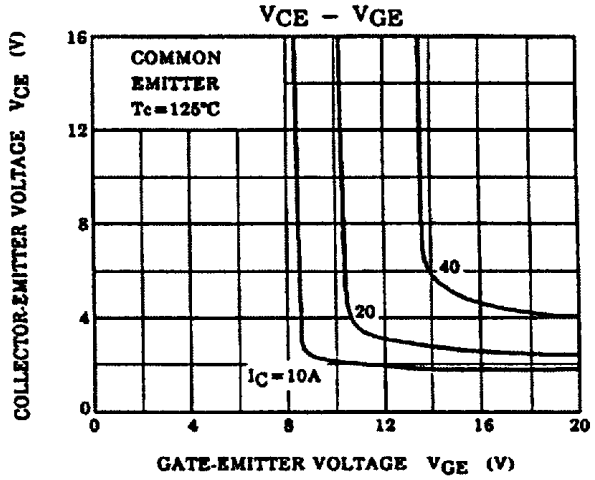
V_{CE} – V_{GE}



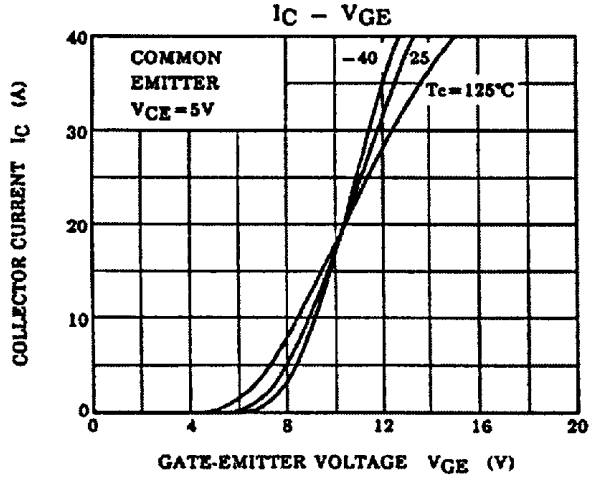
V_{CE} – V_{GE}



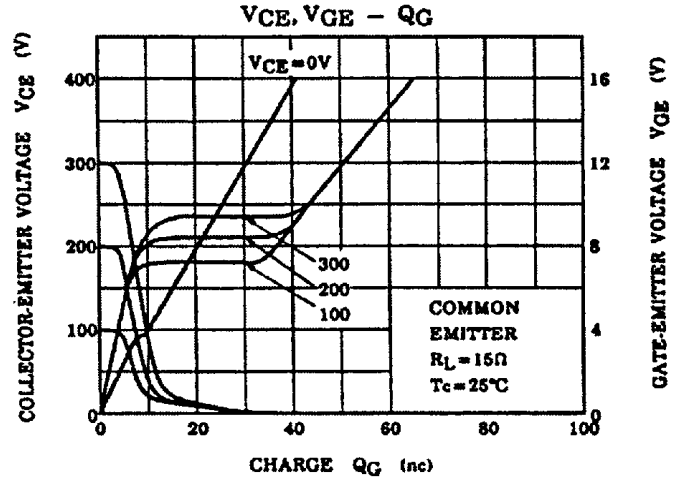
V_{CE} – V_{GE}



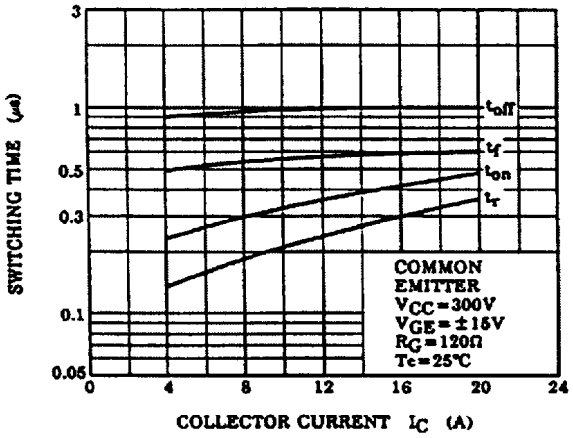
I_C – V_{GE}



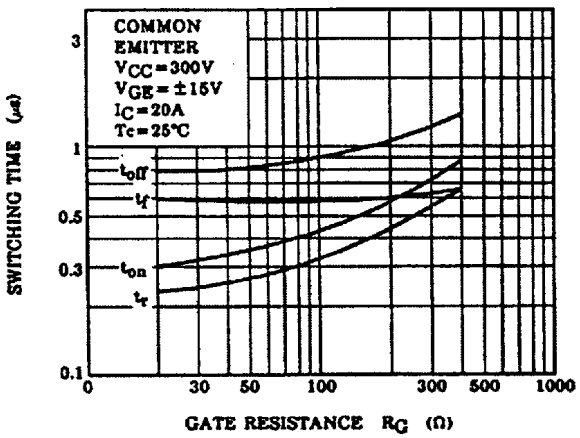
V_{CE}, V_{GE} – Q_G



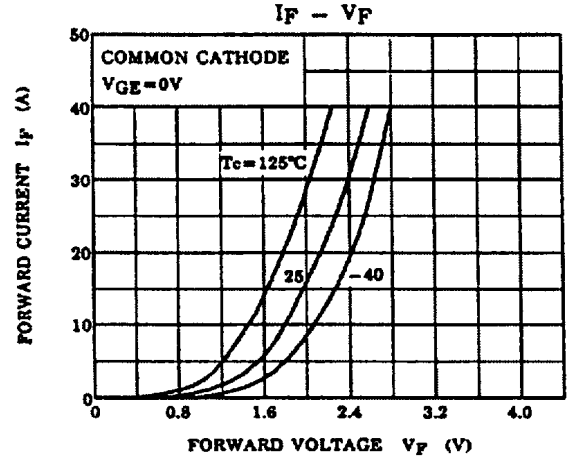
SWITCHING TIME – I_C



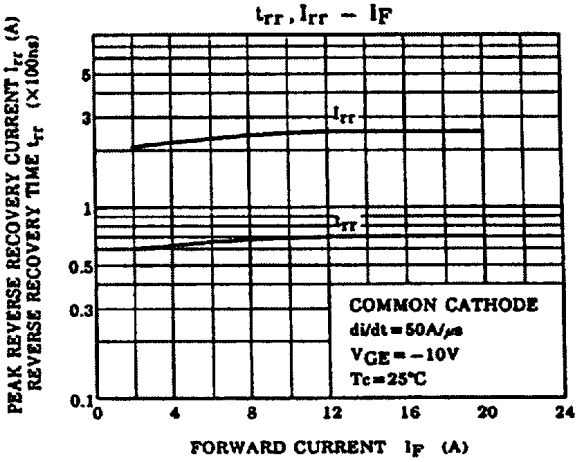
SWITCHING TIME – R_G



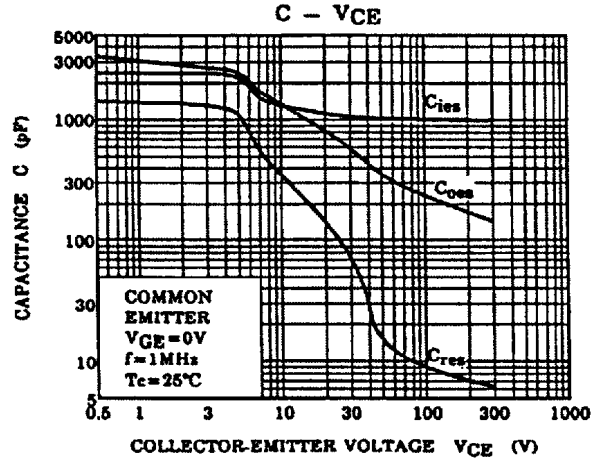
I_F – V_F



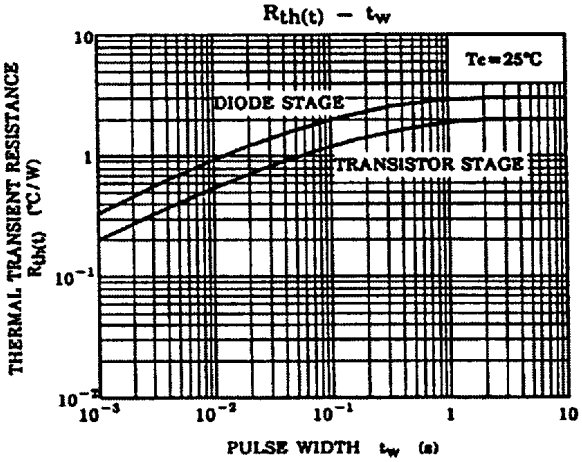
t_{rr}, I_{rr} – I_F



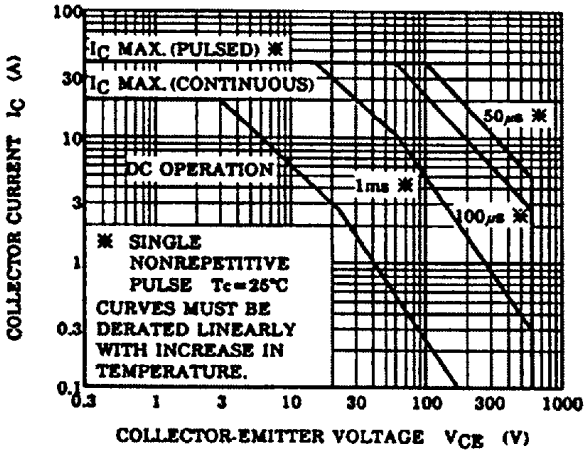
C – V_{CE}



$R_{th(t)}$ – t_w



SAFE OPERATING AREA



REVERSE BIAS SOA