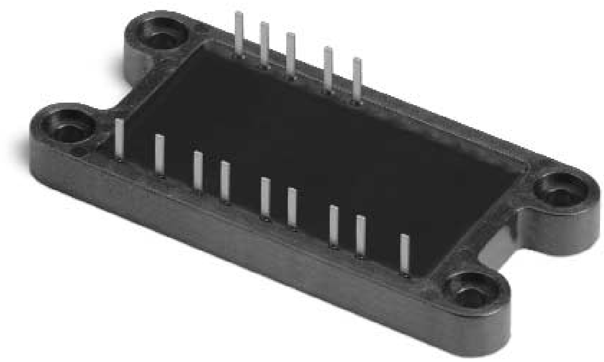
MODEL 7700 SERIES

Power Factor Correction Power Module

NEW HIGHER POWER VERSION



MODELS/RANGE

7700B	1,500 Watts / 3,000 Watts
7700-2A	2,000 Watts / 4,000 Watts

FEATURES AND BENEFITS

- Module contains all power components necessary to provide power factor correction in a switching power supply.
  - Rectifier bridge with SCRs for inrush current limiting
  - Ultrafast platinum output diode
  - 500V .1Ω Max. FET (7700B)
  - Low gate charge, 500V, .0675Ω max. FET (7700-2A)
- Provides optimum use of available line current
- Allows power supply to meet harmonic requirement
- Module design reduces cost of heat sink
- Saves significant space and assembly time
- Low cost
- Internal temperature sensing
- Replaces up to 10 each TO-220 or TO-247 discrete power semiconductors
- Custom module versions available to meet specific requirements such as:
  - Motor drives
  - Power servo amplifiers
  - Solenoid drivers
  - Solid state relays
  - 3 phase rectifier bridges

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APPLICATIONS

Designed to optimally facilitate a boost type power factor correction (PFC) system for designs with up to 36A rms input current.

Standard applications include switching power supplies from 1,000 watts to 4,000 watts with line voltages up to 300 V rms.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions[1]	Model	Min.	Typ.	Max.	Units
MOS FET							
Continuous Drain Current	I_D	T_C = 25°C	B			56	A
			-2A			80	A
		T_C = 100°C	B			34.8	A
			-2A			48	A
Pulsed Drain Current	I_{DM}		B			224	A
			-2A			320	A
Single Pulse Avalanche Energy	E_{AS}		B			760	mJ
			-2A			960	mJ
Repetitive Avalanche Energy	E_{AR}		B			19	mJ
			-2A			28	mJ
Avalanche Current	I_{AR}		B			8.7	A
			-2A			20	A
Gate to Source Voltage	V_{GS}		B, -2A			±30	V
Leakage Current	I_{DSS}	V_{GS} = 0V, V_{DS} = 500V	B, -2A			100	µA
Drain to Source ON Voltage	$V_{DS(ON)}$	I_C = 28A, V_{GS} = 10V	B	1.5		2.8	V
			-2A	1.0		2.7	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 1mA	B, -2A	2.0		4.0	V
Gate Leakage Current	I_{GSS}	V_{GS} ±20V	B, -2A			±400	nA
Total Gate Charge	Qg	I_D = 56A, V_{DS} = 400V	B			600	nC
Gate Source Charge	Qgs	V_{GS} = 10V	B			80	nC
Gate Drain (Miller) Charge	Qgd		B			320	nC
Total Gate Charge	Qg	I_D = 80A, V_{DS} = 400V	-2A			480	nC
Gate Source Charge	Qgs	V_{GS} = 10V	-2A			128	nC
Gate Drain (Miller) Charge	Qgd		-2A			196	nC
Continous Source Current	I_S		B			56	A
(Body Diode)			-2A			80	A
Pulsed Source Current	I_{SM}		B			224	A
(Body Diode)			-2A			320	A
Body Diode Forward Voltage	V_{SD}	I_S = 56A, V_{GS} = 0V	B	0.4		1.4	V
		I_S = 80A, V_{GS} = 0V	-2A	0.5		1.8	V
Reverse Recovery Time	trr	I_F = 56A, di/dt = 400Aµs	B			810	ns
(Body Diode)		I_F = 80A, di/dt = 400Aµs	-2A			860	ns
Reverse Recovery Charge	Qrr	I_F = 56A, di/dt = 400Aµs	B			28.8	ns
(Body Diode)		I_F = 80A, di/dt = 400Aµs	-2A			39.6	ns
Internal Gate Resistor	R_G		B		1.25		Ω
			-2A		0.25		Ω
Junction Temperature	T_J		B, -2A			150	°C
Thermal Resistance	R_{THJC}		B		0.20	.025	°C/W
			-2A		.15	.20	°C/W

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions[1]	Model	Min.	Typ.	Max.	Units
SCRS							
Average On Current	$I_{T(AV)}$	T_C = 75°C, 180° half sine wave	B			20	A
			-2A			35	A
RMS On Current (As AC switch)	I_{RMS}		B			30	A
			-2A			55	A
Peak Repetitive Off Voltage	V_{RRM}/ V_{DRM}		B			600	V
			-2A			800	V
Peak One Cycle Non-Repetitive Surge Current	I_{TSM}	$T_J = T_J$Max., t = 10ms (50 Hz), sine	B			300	A
			-2A			400	A
Reverse and Direct Leakage Current	I_R/I_D	$V_R = V_{RRM}$, $V_D = V_{DRM}$	B			25	µA
			-2A			300	µA
On Voltage	V_T	I_T = 25A	B	0.5		1.6	V
		I_T = 45A	-2A	0.5		1.6	V
Gate Trigger Voltage (Includes drop across R_G)	V_{GT}	V_D= 6V, 22Ω	B, -2A	0.2		3.5	V
		V_D= 6V, 22Ω. T_J = -40°C	B, -2A	0.3		1.5	V
		V_D= 6V, 22Ω. T_J = 125°C	B, -2A	0.1		1.5	V
Gate Trigger Current (Each SCR Individually)	V_{GT}	V_D= 6V, 22Ω	B, -2A	5		60	mA
		V_D= 6V, 22Ω. T_J = -40°C	B, -2A	10		120	mA
		V_D= 6V, 22Ω. T_J = 125°C	B, -2A	2		35	mA
Holding Current	I_H	(Each SCR Individually)	B			100	mA
			-2A			100	mA
Internal Gate Resistor	R_G	Connected to each SCR	B		10		Ω
			-2A		10		Ω
Junction Temperature	T_j		B, -2A			150	°C
Thermal Resistance	R_{thjc}		B		1.4	2.0	°C/W
			-2A		0.7	1.0	°C/W
Bridge Diodes							
Average Forward Current	$I_{F(AV)}$	T_C= 105°C, 180°, half sine wave	B			20	A
			-2A			40	A
Peak Repetitive Reverse Voltage	V_{RRM}		B			600	V
			-2A			800	V
Peak One Cycle Non-Repetitive Surge Current	I_{FSM}	$T_J = T_J$ Max., t = 10ms (50 Hz), sine	B			300	A
			-2A			400	A
Reverse Leakage Current	$I_{R/}$	$V_R = V_{RRM}$	B			100	µA
			-2A			300	µA
Forward Voltage	V_F	I_F = 25A	B	0.5		1.2	V
		I_F = 40A	-2A	0.5		1.2	V
Junction Temperature	T_J		B, -2A			150	°C
Thermal Resistance	R_{THJC}		B		1.5	1.8	°C/W
			-2A		1.0	1.2	°C/W

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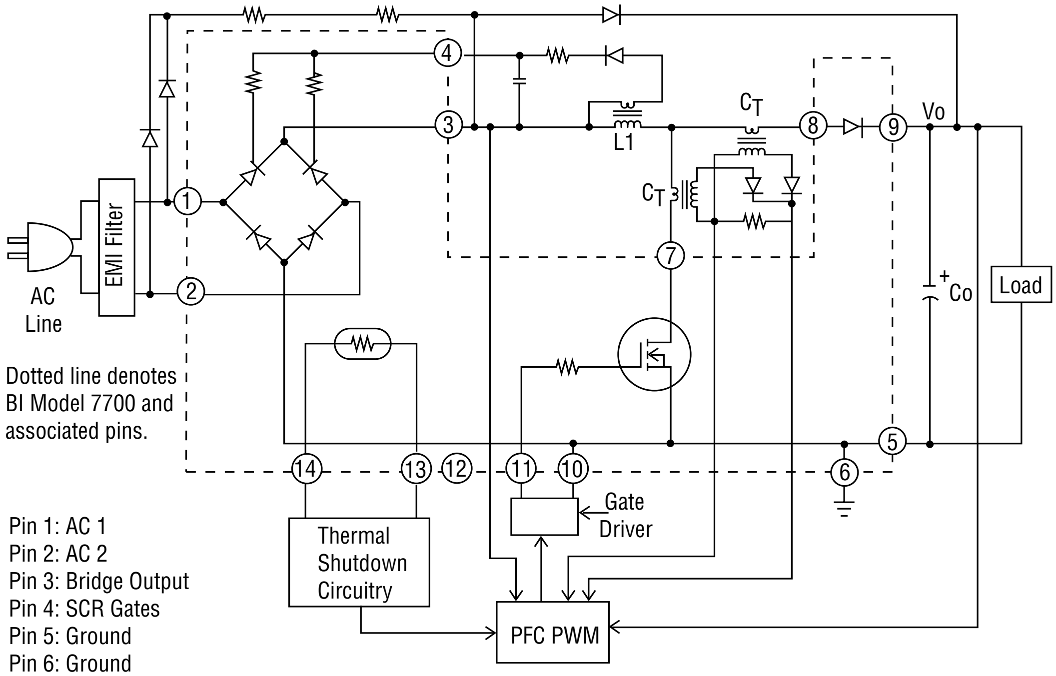
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions[1]	Model	Min.	Typ.	Max.	Units
Output Diode							
Average Forward Current	$I_{F(AV)}$	T_C= 120°C	B			24	A
			-2A			60	A
Peak Repetitive Reverse Voltage	V_{RRM}		B, -2A			600	V
Peak One Cycle Non-Repetitive Surge Current	I_{FSM}	T_J = T_JMax., t = 10ms (50 Hz), sine	B			500	A
			-2A			500	A
Reverse Leakage Current	$I_{R/}$	$V_R = V_{RRM}$	B			60	µA
			-2A			1	mA
Forward Voltage	V_F	I_F = 24A	B	1.0		2.8	V
		I_F = 50A	-2A	0.5		2.8	V
Reverse Recovery Time	trr	I_F = 6A, di/dt = 300Aµs	B			35	ns
		I_F = 2A, di/dt = 200Aµs	-2A			40	ns
Junction Temperature	T_J		B, -2A			175	°C
Thermal Resistance	R_{THJC}		B		0.9	1.0	°C/W
			-2A		0.75	0.9	°C/W
TH1 NTC Thermistor							
Resistance	R_{25}	I = 1mA	B, -2A	22.5	25	27.5	KΩ
Resistance Ratio	R_T/R_{25}	T = 80°C	B, -2A	.126			
		T = 90°C	B, -2A	.0916			
		T = 100°C	B, -2A	.0679			
		T = 110°C	B, -2A	.0511			
Dissipation Constant	P_D		B, -2A		1.0		mW/°C
Thermal Time Constant	t		B, -2A			10	sec

1 - TCase = 25°C unless otherwise specified.

SYSTEM DIAGRAM



Pin 1: AC 1
Pin 2: AC 2
Pin 3: Bridge Output
Pin 4: SCR Gates
Pin 5: Ground
Pin 6: Ground
Pin 7: FET Drain
Pin 8: Ultrafast Anode
Pin 9: Ultrafast Cathode
Pin 10: Gate Ground
Pin 11: Gate Drive
Pin 12: N.C.
Pin 13: TH 1
Pin 14: TH 2

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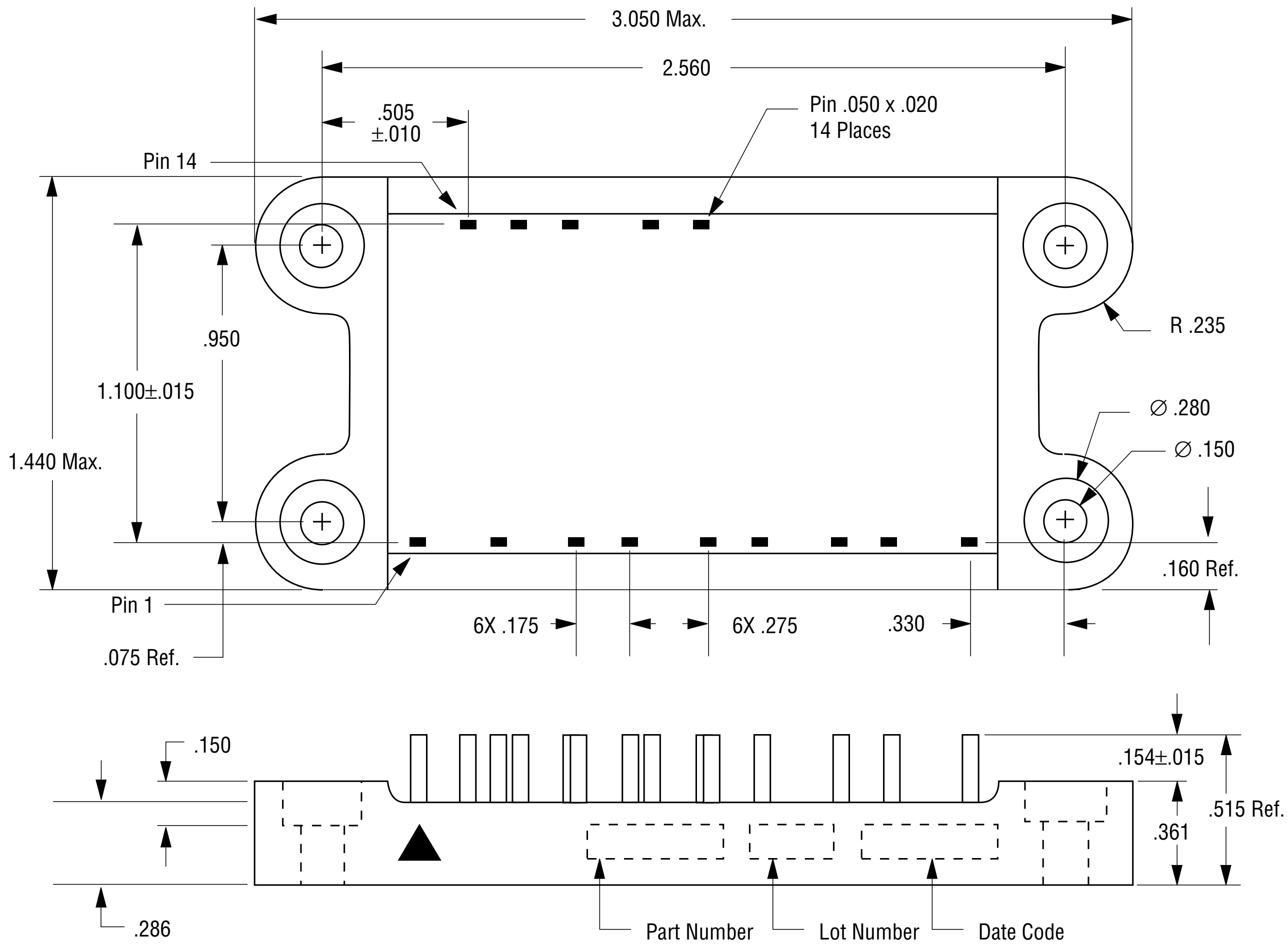
OUTLINE DIMENSIONS (Inch)



ORDERING INFORMATION

77 0 0 B

Model — 77

Package — 0

Circuit Function:
0 = Power Factor Correction

Range, Watts:
B = 1,500 to 3,000 Watts
-2A = 2,000 to 4,000 Watts

OUTPUT VOLTAGE

The dc output voltage must be greater than the highest peak line voltage expected:

$$V_0 > V_{IN\ MAX} \times 1.414$$

DISCONTINUOUS CONDUCTION

When the line voltage approaches zero volts the PFC PWM will be forced towards its maximum duty cycle. This will cause the current to become discontinuous, which will result in some distortion. The line voltage at which the current will become discontinuous will be:

$$V_{IN\ discontinuous} = \frac{V_0 \times (1 - DC_{MAX})}{DC_{MAX}}$$

The line voltage at which the PWM will be duty cycle limited will be:

$$V_{IN\ duty\ cycle\ limited} = V_0 \times (1 - DC_{MAX})$$

INDUCTOR L1

The inductor value controls the amplitude of the 100KHz current ripple. This can greatly effect the amount of distortion and thus the amount of EMI filtering required on the input. Ripple current can be calculated for any point along the input sine wave:

$$I_{P-P}(t) = \frac{V_{IN}(t) \times DC(t)}{L \times f}$$

Where: $DC(t)=1-V_{IN}(t)/V_O$, L is the inductance of L1, and f is the switching frequency.

A good starting point would be to set Ip-p equal to 20% of the 120 Hz peakcurrent, solving for L:

$$L \geq \frac{5 \times V_{IN}^2 \times \left(1 - \frac{1.414 \times V_{IN}}{V_0}\right)}{P_{IN} \times f}$$

OUTPUT CAPACITOR

The output capacitor size is often limited by the line dropout requirements of the power supply:

$$C_{O\ MIN} = \frac{2 \times P_{OUT} \times t_d}{V_0^2 - V_{O\ MIN}^2}$$

Where: P_{OUT} is the output power, td is the dropout time, and $V_{O\ MIN}$ is the minimum allowed output voltage.

The 120Hz output voltage ripple can be calculated to insure it meets the system requirements:

$$V_{O\ P-P\ 120} = \left(\frac{2 \times P_0}{V_0}\right) \times \left(\frac{1}{2 \times \pi \times f \times C_0} + ESR\right)$$

The maximum rms 120Hz ripple current will be:

$$I_{RMS\ 120} = \frac{1.414 \times P_0}{V_0}$$

The 100KHz output voltage ripple will be:

$$V_{O\ P-P\ 100K} = \frac{V_{IN} \times \left(1 - \frac{(1.414 \times V_{IN})}{V_0}\right)}{L \times f} \times \left(\frac{1}{2 \times \pi \times f \times C_0} + ESR\right)$$

The maximum rms 100KHz ripple current will be:

$$I_{RMS\ 100K} = \frac{V_{IN} \times \left(1 - \frac{1.414 \times V_{IN}}{V_0}\right)}{2.828 \times L \times f}$$

GATE DRIVE REQUIREMENTS

FET switching times must be fast enough to insure that the FET turns off when the PWM is at maximum duty cycle. Snubbing circuits across the FET will slow the turn off time and should not be used.

A discrete gate driver circuit will allow the fastest possible switching times. The Unitrode UC3710 or Telcom TC4422 drivers offer a single chip approach with only slightly slower switching times. The gate driver must be located as close to the module as possible. Ground sense pin 10 should be used to insure the fastest possible switching times.

HEAT RADIATOR

The heat radiator requirements can be determined by the maximum power dissipated (at low line) and the maximum ambient temperature. The back side of the module should be limited to about 100°C by utilizing the internal thermistor.

$$R_{\Theta} = \frac{100 - T_{MAX\ AMB}}{P_{O\ LOWLINE}}$$

Care should be used when attaching the module to the heat radiator. The screws must be tightened incrementally in a crisscross pattern. A torque limiting screwdriver should be used.

The high current levels require currrent sense transformers to maintain a reasonable efficiency. We recommend BI Technologies HM31-20200.

PFC PWM VENDORS

Popular sources are:
Unitrode UC3854
Micro Linear ML4812
Linear Technology LT1248