October 27, 2010

DS90LV032A

3V LVDS Quad CMOS Differential Line Receiver

General Description

The DS90LV032A is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV032A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports open, shorted and terminated (100Ω) input Fail-safe. The receiver output will be HIGH for all fail-safe conditions.

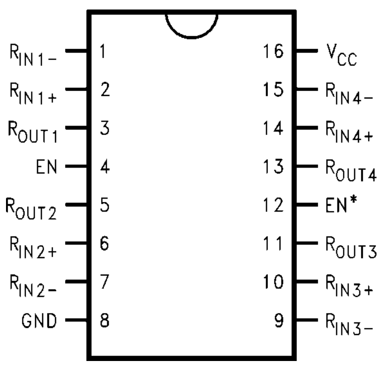
The DS90LV032A and companion LVDS line driver (eg. DS90LV031A) provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- 0.1 ns channel-to-channel skew (typical)
- 0.1 ns differential skew (typical)
- 3.3 ns maximum propagation delay
- 3.3V power supply design
- Power down high impedance on LVDS inputs
- Low Power design (40mW @ 3.3V static)
- Interoperable with existing 5V LVDS networks
- Accepts small swing (350 mV typical) VID
- Supports open, short and terminated input fail-safe
- Compatible with ANSI/TIA/EIA-644
- Industrial temp. operating range (-40°C to +85°C)
- Available in SOIC and TSSOP Packaging

Connection Diagram

Dual-in-Line



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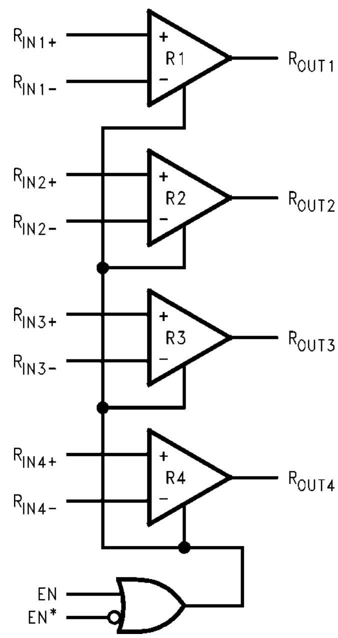
Order Number DS90LV032ATM or DS90LV032ATMTC See NS Package Number M16A or MTC16

Functional Diagram



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Truth Table

ENABLES		INPUTS	OUTPUT
EN	EN*	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (R_{IN+}, R_{IN-})	−0.3V to +3.9V
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (R_{OUT})	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation @ +25°C	
M Package	1025 mW
MTC Package	866 mW
Derate M Package	8.2 mW/°C above +25°C
Derate MTC Package	6.9 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
(Soldering 4 sec.)	+260°C
Maximum Junction Temperature	+150°C
ESD Rating (Note 10)	
(HBM 1.5 kΩ, 100 pF)	≥ 4.5 kV
(EIAJ 0 Ω, 200 pF)	≥ 250 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		+3.0	V
Operating Free Air Temperature (T_A)	−40	25	+85	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V (Note 13)		R_{IN+}, R_{IN-}		+20	+100	mV
V_{TL}	Differential Input Low Threshold				−100	−20		mV
VCMR	Common-Mode Voltage Range	VID = 200 mV peak to peak (Note 5)			0.1		2.3	V
I_{IN}	Input Current	V_{IN} = +2.8V	V_{CC} = 3.6V or 0V		−10	±1	+10	μA
		V_{IN} = 0V			−10	±1	+10	μA
		V_{IN} = +3.6V	V_{CC} = 0V		-20		+20	μA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	2.7	3.0		V
		I_{OH} = −0.4 mA, Input terminated			2.7	3.0		V
		I_{OH} = −0.4 mA, Input shorted			2.7	3.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.1	0.25	V
I_{OS}	Output Short Circuit Current	Enabled, V_{OUT} = 0V (Note 11)			−15	−48	−120	mA
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} = 0V or V_{CC}			−10	±1	+10	μA
V_{IH}	Input High Voltage			EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Low Voltage				GND		0.8	V
I_I	Input Current	V_{IN} = 0V or V_{CC}, Other Input = V_{CC} or GND			−10	±1	+10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current Receivers Enabled	EN, EN* = V_{CC} or GND, Inputs Open		V_{CC}		10	15	mA
		EN, EN* = 2.4V or 0.5V, Inputs Open				10	15	mA
I_{CCZ}	No Load Supply Current Receivers Disabled	EN = GND, EN* = V_{CC}, Inputs Open				3	5	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 3, Note 4, Note 7, Note 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 10 pF	1.8		3.3	ns
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200 mV	1.8		3.3	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Note 6)	(Figure 1 and Figure 2)	0	0.1	0.35	ns
t_{SKD2}	Differential Channel-to-Channel Skew-same device (Note 7)		0	0.1	0.5	ns
t_{SKD3}	Differential Part to Part Skew (Note 8)				1.0	ns
t_{SKD4}	Differential Part to Part Skew (Note 9)				1.5	ns
t_{TLH}	Rise Time			0.35	1.2	ns
t_{THL}	Fall Time			0.35	1.2	ns
t_{PHZ}	Disable Time High to Z	R_L = 2 kΩ		8	12	ns
t_{PLZ}	Disable Time Low to Z	C_L = 10 pF		6	12	ns
t_{PZH}	Enable Time Z to High	(Figure 3 and Figure 4)		11	17	ns
t_{PZL}	Enable Time Z to Low			11	17	ns
f_{MAX}	Maximum Operating Frequency (Note 14)	All Channels Switching	200	250		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.

Note 4: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.

Note 5: The VCMR range is reduced for larger VID. Example: if VID = 400mV, the VCMR is 0.2V to 2.2V. The fail-safe condition with inputs shorted is valid over a common-mode range of 0V to 2.3V. A VID up to V_{CC} – 0V may be applied to the R_{IN+}/ R_{IN-} inputs with the Common-Mode voltage set to V_{CC}/2. Propagation delay and Differential Pulse skew decrease when VID is increased from 200mV to 400mV. Skew specifications apply for 200mV ≤ VID ≤ 800mV over the common-mode range .

Note 6: t_{SKD1} is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel

Note 7: t_{SKD2}, Channel-to-Channel Skew, is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.

Note 8: t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC}, and within 5°C of each other within the operating temperature range.

Note 9: t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max – Min| differential propagation delay.

Note 10: ESD Rating:

HBM (1.5 kΩ, 100 pF) ≥ 4.5kV

EIAJ (0Ω, 200 pF) ≥ 250V

Note 11: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Note 12: C_L includes probe and jig capacitance.

Note 13: V_{CC} is always higher than R_{IN+} and R_{IN-} voltage. R_{IN-} and R_{IN+} are allowed to have a voltage range –0.2V to V_{CC} – VID/2. However, to be compliant with AC specifications, the common voltage range is 0.1V to 2.3V

Note 14: f_{MAX} generator input conditions: t_r = t_f < 1ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35V peak to peak). Output Criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), Load = 10 pF (stray plus probes)

Parameter Measurement Information

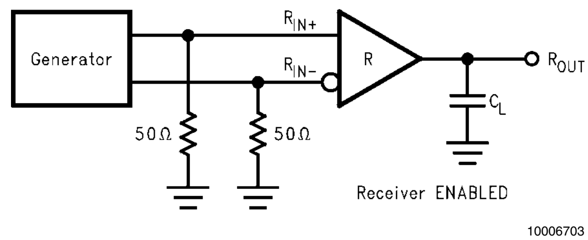


FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit

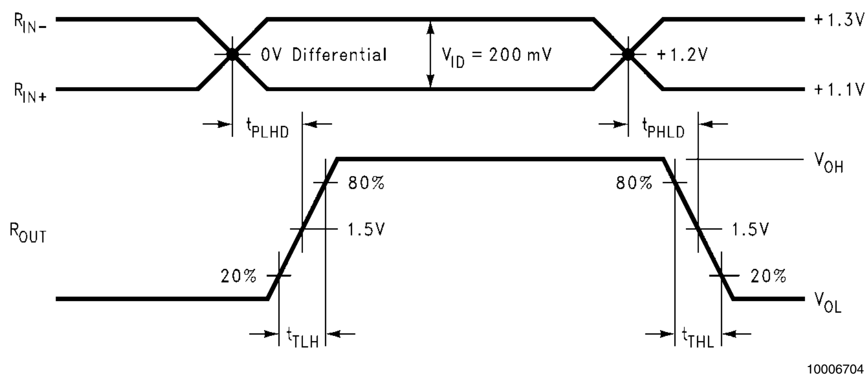
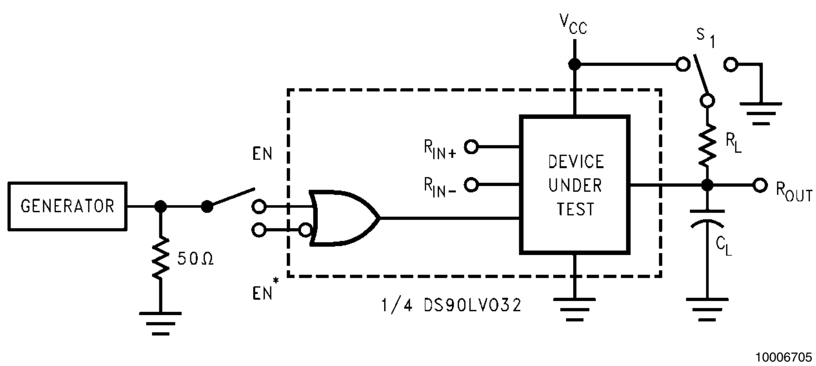


FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms



C_L includes load and test jig capacitance.
S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S_1 = GND for t_{PZH} and t_{PHZ} measurements.

FIGURE 3. Receiver TRI-STATE Delay Test Circuit

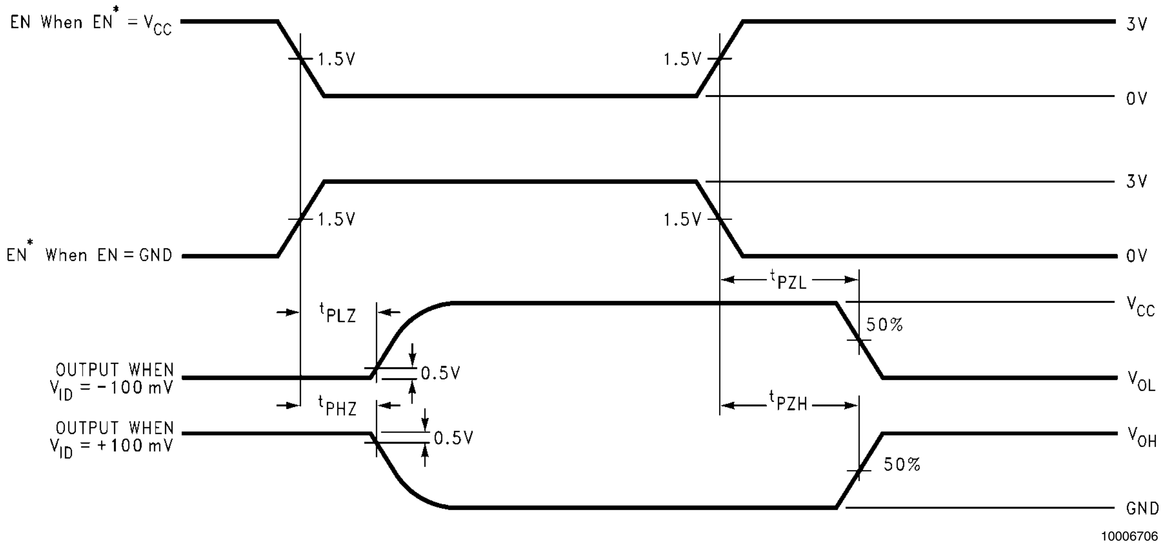


FIGURE 4. Receiver TRI-STATE Delay Waveforms

Typical Application

Balanced System

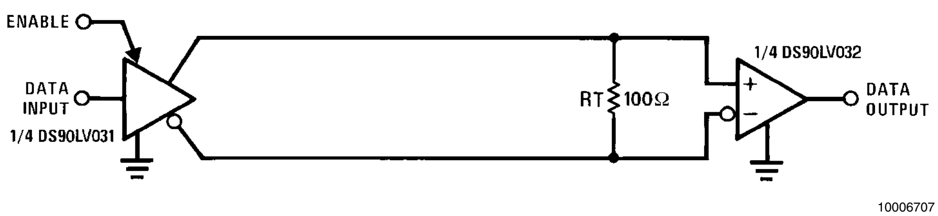


FIGURE 5. Point-to-Point Application

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: www.national.com/lvds.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 5*. This configuration provides a clean signaling environment for the fast edge rates of the drivers . The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV032A differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins have a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

Power Decoupling Recommendations:

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1µF in parallel with 0.01µF, in parallel with 0.001µF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC Board considerations:

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

Differential Traces:

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

Termination:

Use a resistor which best matches the differential impedance of your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <10mm (12mm MAX)

Probing LVDS Transmission Lines:

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

Cables and Connectors, General Comments:

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the receiver. For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

Fail-Safe Feature:

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV032A is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left

OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.

3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

The footprint of the DS90LV032A is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

Pin Descriptions

Pin No.	Name	Description
2, 6, 10, 14	R_{IN+}	Non-inverting receiver input pin
1, 7, 9, 15	R_{IN-}	Inverting receiver input pin
3, 5, 11, 13	R_{OUT}	Receiver output pin
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +3.3V ± 0.3V
8	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40°C to +85°C	SOP/M16A	DS90LV032ATM
−40°C to +85°C	TSSOP/MTC16	DS90LV032ATMTC

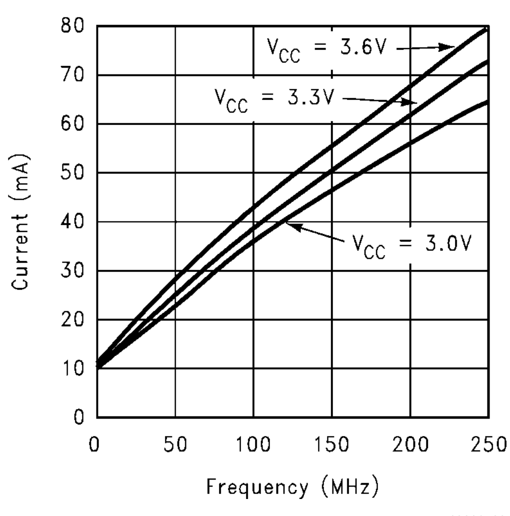


FIGURE 6. ICC vs Frequency, four channels switching

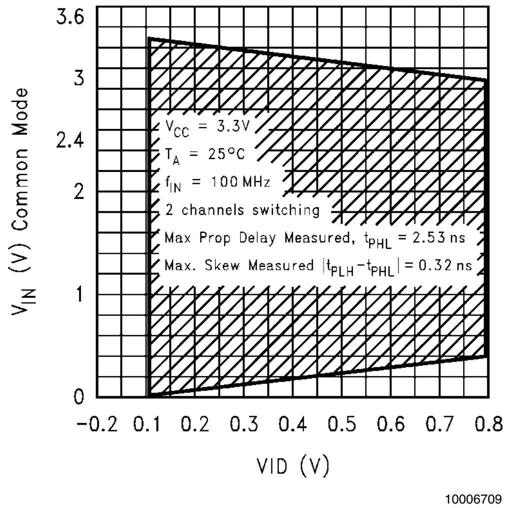


FIGURE 7. Typical Common-Mode Range variation with respect to amplitude of differential input

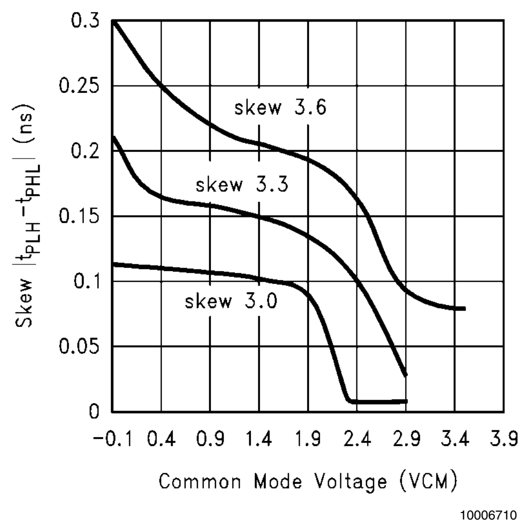


FIGURE 8. Typical Pulse Skew variation versus common-mode voltage

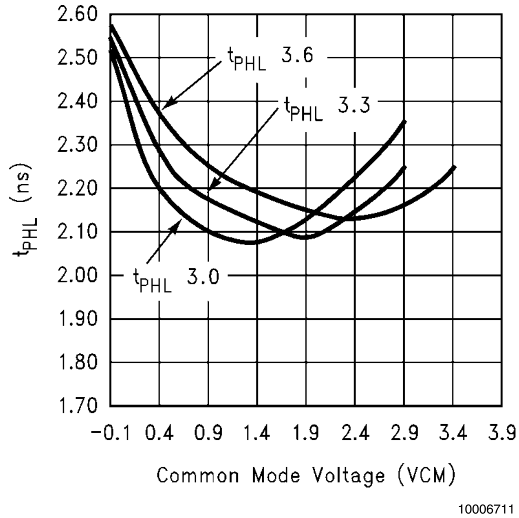


FIGURE 9. Variation in High to Low Propagation Delay versus VCM

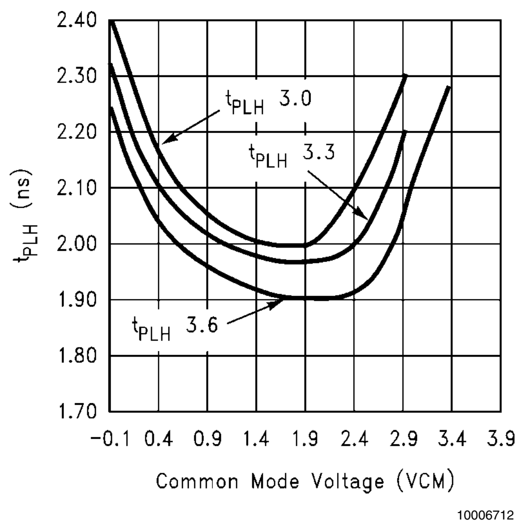
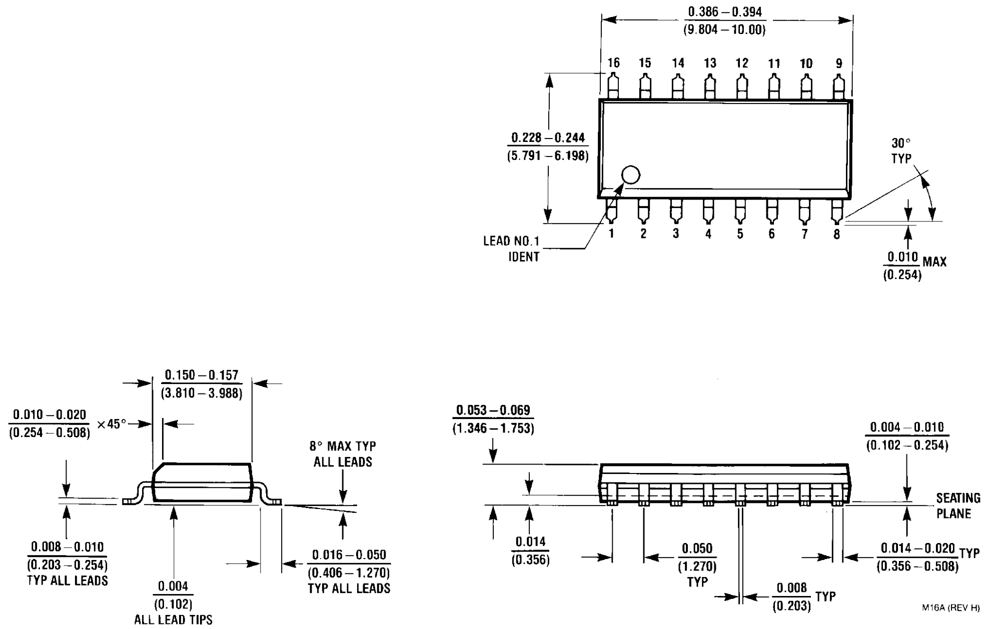
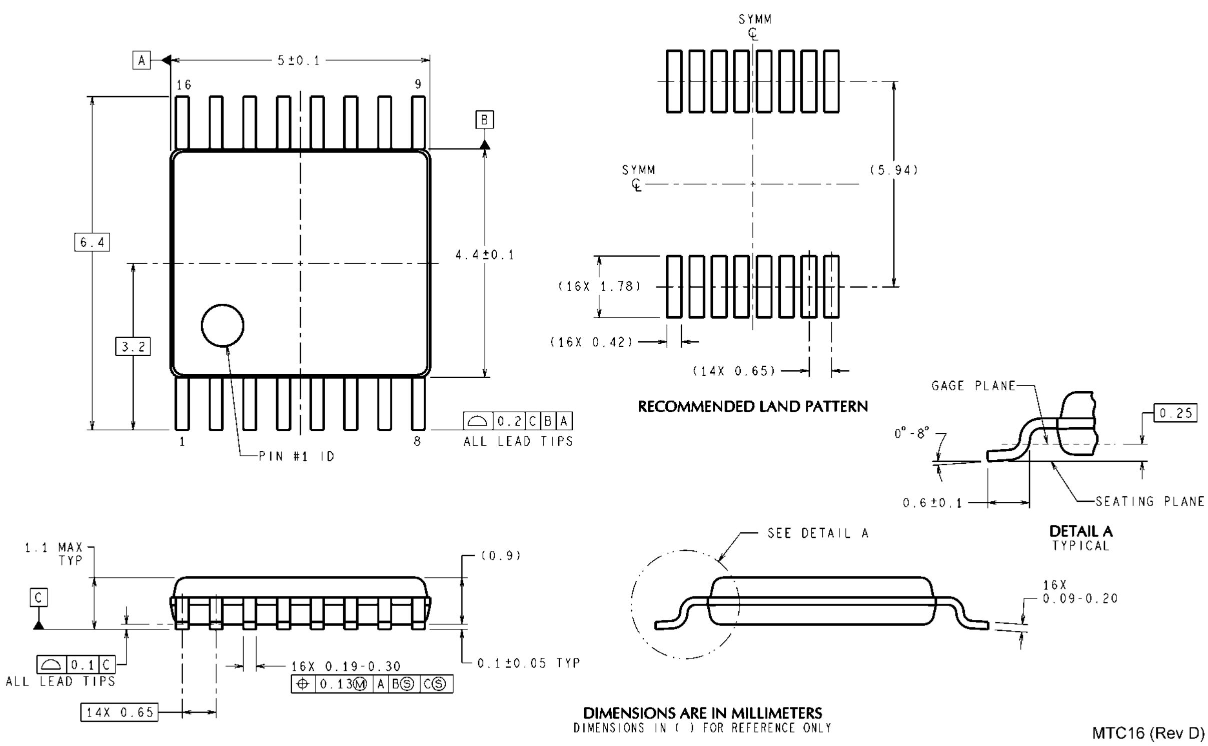


FIGURE 10. Variation in Low to High Propagation Delay versus VCM

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC
Order Number DS90LV032ATM
NS Package Number M16A



16-Lead (0.100″ Wide) Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90LV032ATMTC
NS Package Number MTC16

Notes

Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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