1800 MHz to 2700 MHz 2-Stage 1W RF Driver Amplifier

Preliminary Technical Data

ADL5606

FEATURES

Operation from 1800 MHz to 2700 MHz
Gain of 23.8 dB at 2140 MHz
OIP3 of 45.7 dBm at 2140 MHz
P1dB of 30.7 dBm at 2140 MHz
Noise figure of 4.8 dB at 2140 MHz
Power supply 5 V
Power supply current 360 mA typical
Internal active biasing
Power down function
Compact 4mm x 4mm 16-lead LFCSP
ESD rating of ±1 kV (Class 1C)
Pin-Compatible with the ADL5605, 700 – 1000 MHz

FUNCTIONAL BLOCK DIAGRAM

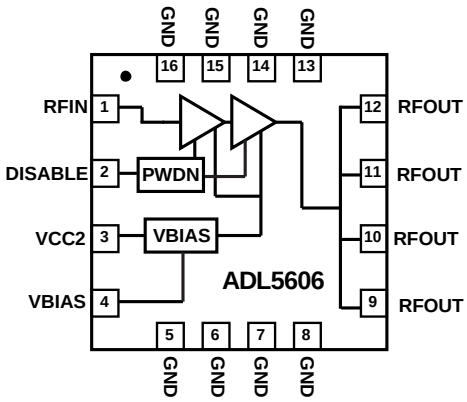

Figure 1

GENERAL DESCRIPTION

The ADL5606 is a broadband 2-stage 1 W RF driver amplifier that operates over a frequency range of 1800 MHz to 2700 MHz. The device can be used in a wide variety of wired and wireless applications including ISM, MC-GSM, W-CDMA, TD-SCDMA and LTE.

The ADL5606 operates on a 5 V supply voltage and a supply current of 360 mA. The driver also incorporates a fast turn on/off function for TDD applications, applications requiring a power saving mode, or for applications that intermittently transmit data.

The ADL5606 is fabricated on a GaAs HBT process. The device is packaged in a compact 4mm x 4mm 16-lead LFCSP that uses an exposed paddle for excellent thermal impedance. It operates from −40°C to +85°C, and a fully populated evaluation board is available.

Rev. PrA

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SPECIFICATIONS

VCC = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		1800		2700	MHz
FREQUENCY = 1960±30 MHz					
Gain			22.7		dB
vs. Frequency	±30 MHz		±0.7		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Output 1 dB Compression Point			30		dBm
vs. Frequency	±30 MHz	29.5			dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C	29.3			dB
vs. Supply	4.75 V to 5.25 V	29.2			dB
ACP	Pout =19dBm, 1 Carrier WCDMA 64 DPCH		-55		dBc
Output Third-Order Intercept	Δf = 1 MHz, POUT = 14 dBm per tone		47		dBm
vs. Frequency	±30 MHz	46.3			dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C	46.5			dB
vs. Supply	4.75 V to 5.25 V	46.2			dB
Noise Figure			5.3	7	dB
Input Return Loss	±30 MHz		-10		dB
Output Return Loss	±30 MHz		-8		dB
FREQUENCY = 2140±30MHz					
Gain		19.5	22.4	22.5	dB
vs. Frequency	±30 MHz		±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Output 1 dB Compression Point			30		dBm
vs. Frequency	±30 MHz	29.2			dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C	29			dB
vs. Supply	4.75 V to 5.25 V	29			dB
ACP	Pout =19dBm, 1 Carrier WCDMA 64 DPCH		-55		dBc
Output Third-Order Intercept	Δf = 1 MHz, POUT = 14 dBm per tone		47		dBm
vs. Frequency	±30 MHz	46.5			dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C	46.5			dB
vs. Supply	4.75 V to 5.25 V	46.2			dB
Noise Figure			5	7	dB
Input Return Loss	±30 MHz		-15		dB
Output Return Loss	±30MHz		-8	-6	dB

Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY = 2655±35MHz					
Gain			21.6		dB
vs. Frequency	±35 MHz		±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Output 1 dB Compression Point			28.4		dBm
vs. Frequency	±35 MHz	28.3			dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C	28.1			dB
vs. Supply	4.75 V to 5.25 V	28.2			dB
ACP	Pout =19dBm, 1Carrier WCDMA64 DPCH		-55		dBc
Output Third-Order Intercept	Δf = 1 MHz, POUT = 14 dBm per tone		47		dBm
vs. Frequency	±35 MHz	46.5			dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C	46.5			dB
vs. Supply	4.75 V to 5.25 V	46.5			dB
Noise Figure			6.6	7	dB
Input Return Loss	±35 MHz		-10		dB
Output Return Loss	±35 MHz		-8	-6	dB
POWER-DOWN INTERFACE	Pin DISABLE				
Logic Level to Enable	VPWDN decreasing	0.5	TBD	4.5	V
Logic Level to Disable	VPWDN increasing	0.5	TBD	4.5	V
Enable Pin Current	VPWDN Enabled		0.75	1	mA
VCC1 Pin Current	VPWDN Disabled		30		mA
Enable Time	10-90%		TBD	8	µs
Disable Time	10-90%		TBD	11	µs
POWER INTERFACE	Pin RFOUT				
Supply Voltage		4.75	5	5.25	V
Supply Current			360	TBD	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		TBD		mA

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

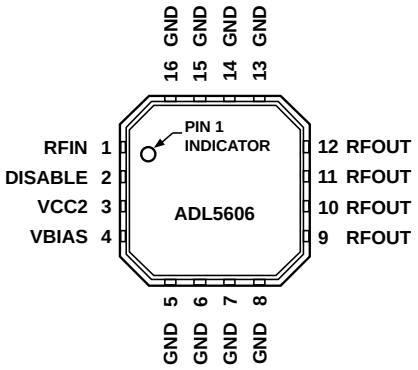

Figure 2 Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. Requires a dc blocking capacitor.
5, 6, 7, 8, 13,14, 15, 16	GND	Solder to a low impedance electrical and thermal ground plane.
2	DISABLE	Connect disable pin to 5V to disable the part, draws around 5mA under the disabled state
3	VCC2	Under normal operation, this pin is connected to the power supply and draws around 360 mA of current. This pin when grounded along with the VBIAS pin disables the device and draws around 10uA of current
4	VBIAS	Applying 5 V to this pin enables the bias circuit. Grounding this pin disables the device and draws around 10uA of current
9, 10, 11, 12	RFOUT	RF Output, DC bias is provided to this pin through an inductor that is connected to the 5 V power supply. The RF path requires a dc blocking capacitor.
	EP	The exposed paddle is connected internally to ground. Solder to a low impedance electrical and thermal ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

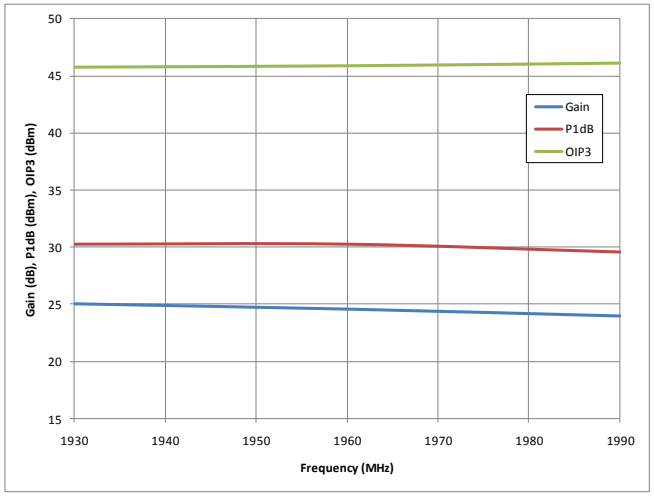

Figure 3 Gain, P1dB, OIP3 at P_{OUT}=14 dBm/Tone vs. Frequency

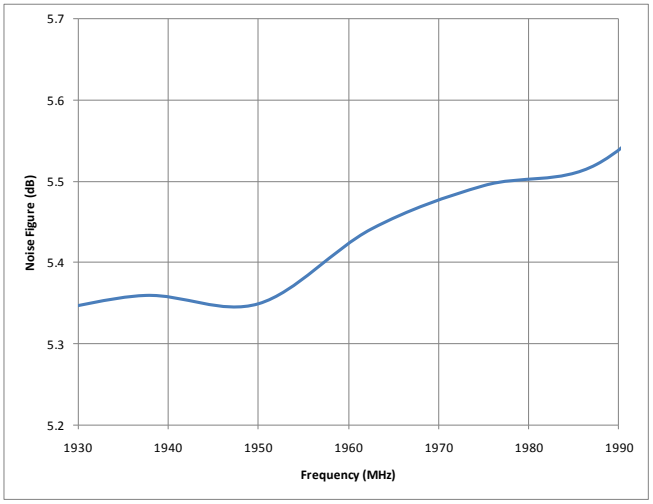

Figure 6 Noise Figure vs. Frequency

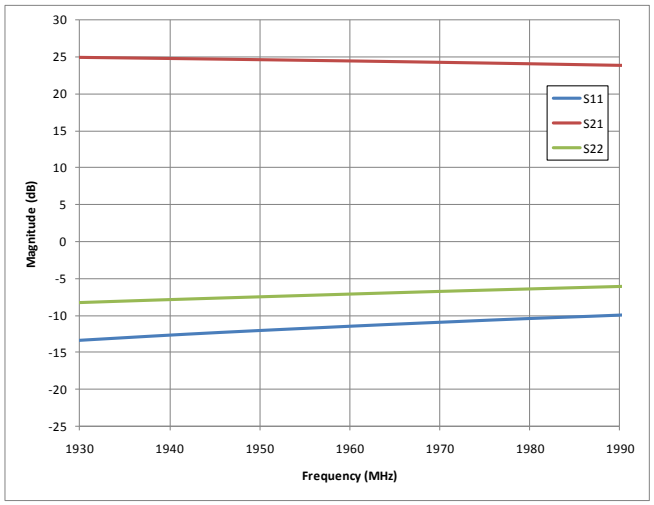

Figure 4 Input Return Loss (S11), Output Return Loss (S22), and Gain (S21) vs. Frequency

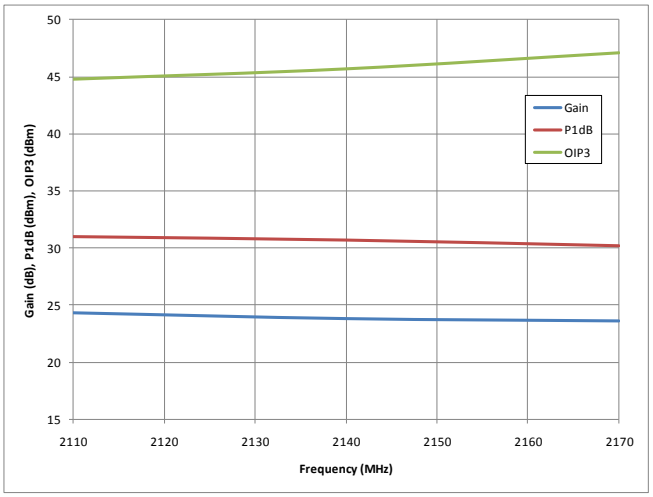

Figure 7 Gain, P1dB, OIP3 at P_{OUT}=TBD dBm/Tone vs. Frequency

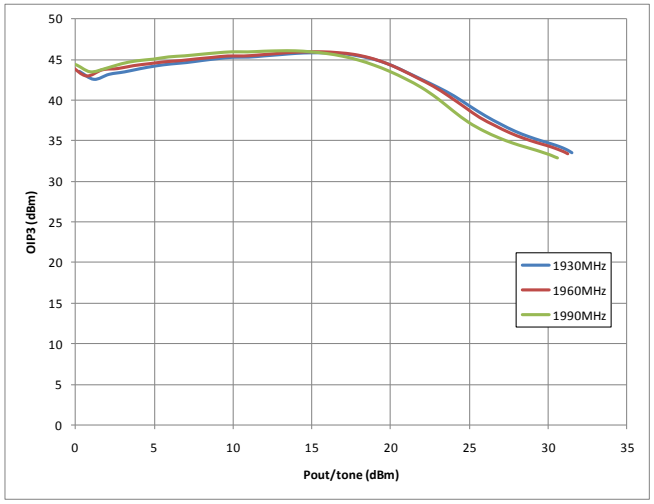

Figure 5 OIP3 vs. P_{OUT} and Frequency

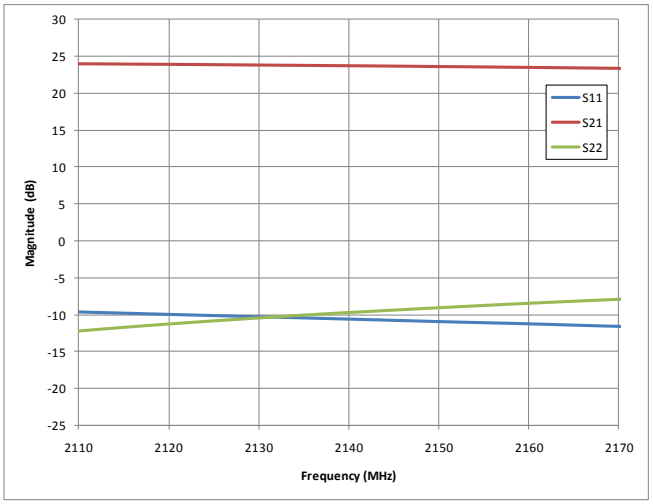

Figure 8 Input Return Loss (S11), Output Return Loss (S22), andGain (S21) vs. Frequency

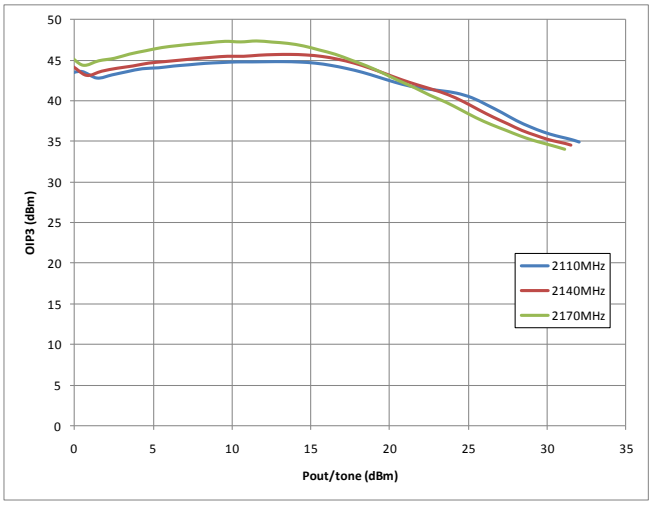

Figure 9 OIP3 vs. P_{OUT} and Frequency

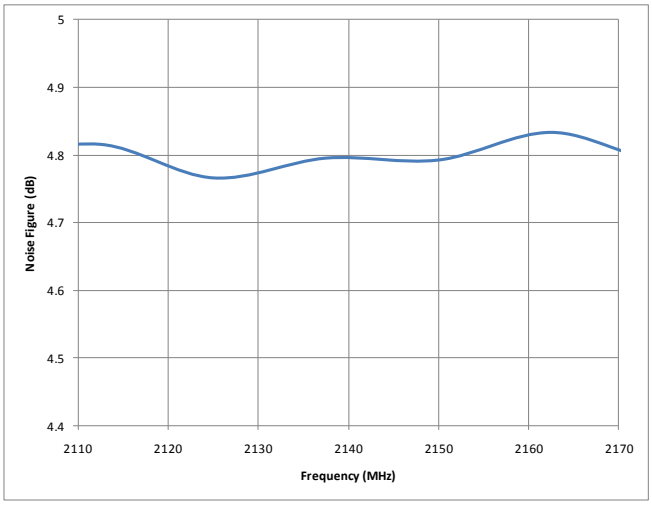

Figure 10 Noise Figure vs. Frequency

OUTLINE DIMENSIONS

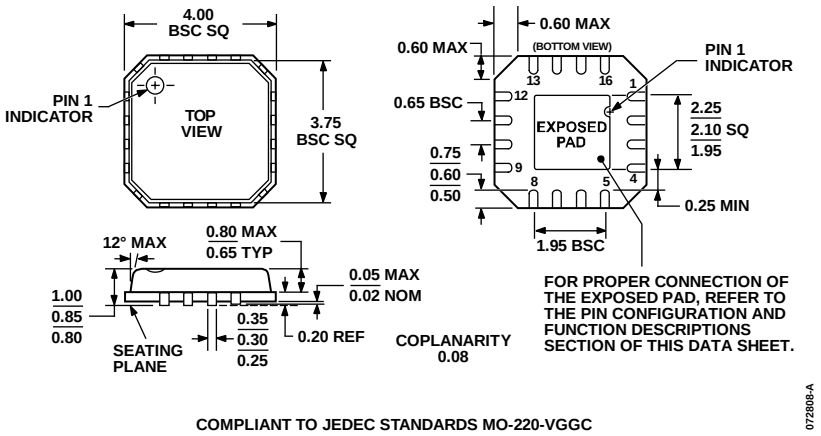

Figure 11. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model [1]	Temperature Range	Package Description	Package Option
ADL5606ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADL5606-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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