

# VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO) 10 MHz TO 1.4 GHz

## Features

- Available with any-rate output frequencies from 10 to 945 MHz and selected frequencies to 1.4 GHz
- 3rd generation DSPLL<sup>®</sup> with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Lead-free/RoHS-compliant

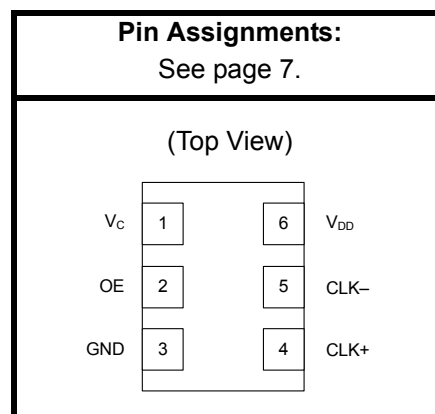
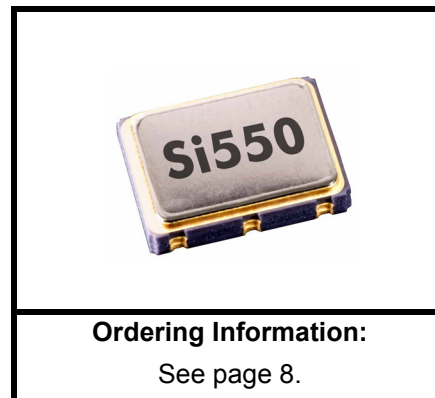
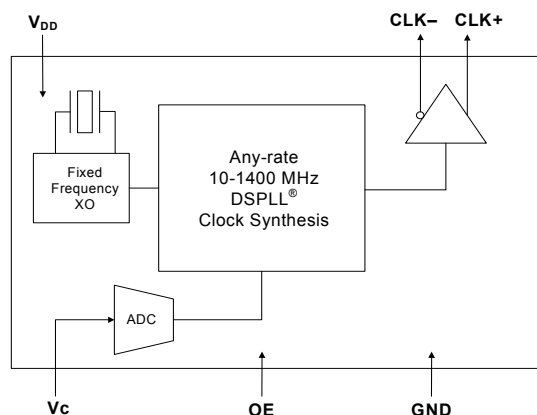
## Applications

- SONET/SDH
- xDSL
- 10 GbE LAN/WAN
- Low-jitter clock generation
- Optical modules
- Clock and data recovery

## Description

The Si550 VCXO utilizes Silicon Laboratories' advanced DSPLL<sup>®</sup> circuitry to provide a low-jitter clock at high frequencies. The Si550 is available with any-rate output frequency from 10 to 945 MHz and selected frequencies to 1400 MHz. Unlike traditional VCXOs, where a different crystal is required for each output frequency, the Si550 uses one fixed crystal to provide a wide range of output frequencies. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low-jitter clocks in noisy environments typically found in communication systems. The Si550 IC-based VCXO is factory-configurable for a wide variety of user specifications, including frequency, supply voltage, output format, tuning slope, and temperature stability. Specific configurations are factory programmed at time of shipment, thereby eliminating the long lead times associated with custom oscillators.

## Functional Block Diagram



## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage <sup>1</sup>	V <sub>DD</sub>	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I <sub>DD</sub>	Output enabled LVPECL	—	120	130	mA
		CML	—	108	117	
		LVDS	—	99	108	
		CMOS	—	90	98	
		tristate mode	—	60	75	
Output Enable (OE) <sup>2</sup>		V <sub>IH</sub>	0.75 x V <sub>DD</sub>	—	—	V
		V <sub>IL</sub>	—	—	0.5	
Operating Temperature Range	T <sub>A</sub>		−40	—	85	°C

**Notes:**

- Selectable parameter specified by part number. See 3. "Ordering Information" on page 8 for further details.
- OE pin includes a 17 kΩ resistor to V<sub>DD</sub>.

**Table 2. V<sub>C</sub> Control Voltage Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope <sup>1,2,3</sup>	K <sub>V</sub>	10 to 90% of V <sub>DD</sub>	—	33	—	ppm/V
				45		
				90		
				135		
				180		
				356		
Control Voltage Linearity <sup>4</sup>	L <sub>VC</sub>	BSL	−5	±1	+5	%
		Incremental	−10	±5	+10	
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V <sub>C</sub> Input Impedance	Z <sub>VC</sub>		500	—	—	kΩ
Nominal Control Voltage	V <sub>CNOM</sub>	@ f <sub>O</sub>	—	V <sub>DD</sub> /2	—	V
Control Voltage Tuning Range	V <sub>C</sub>		0		V <sub>DD</sub>	V

**Notes:**

- Positive slope; selectable option by part number. See 3. "Ordering Information" on page 8.
- For best jitter and phase noise performance, always choose the smallest K<sub>V</sub> that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K<sub>V</sub>), Stability, and Absolute Pull Range (APR)" for more information.
- K<sub>V</sub> variation is ±10% of typical values.
- BSL determined from deviation from best straight line fit with V<sub>C</sub> ranging from 10 to 90% of V<sub>DD</sub>. Incremental slope determined with V<sub>C</sub> ranging from 10 to 90% of V<sub>DD</sub>.

Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency <sup>1,2,3</sup>	f <sub>O</sub>	LVDS/CML/LVPECL	10	—	945	MHz
		CMOS	10	—	160	
Temperature Stability <sup>1,4</sup>		T <sub>A</sub> = -40 to +85 °C	-20 -50 -100	— — —	+20 +50 +100	ppm
Absolute Pull Range <sup>1,4</sup>	APR		±25	—	±375	ppm
Aging		Frequency drift over first year.	—	—	±3	ppm
		Frequency drift over 15 year life.	—	—	±10	
Power up Time <sup>5</sup>	t <sub>OSC</sub>		—	—	10	ms

**Notes:**

- See Section 3. "Ordering Information" on page 8 for further details.
- Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
- Nominal output frequency set by V<sub>CNOM</sub> = V<sub>DD</sub>/2.
- Selectable parameter specified by part number.
- Time from power up or tristate mode to f<sub>O</sub>.

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option <sup>1</sup>	V <sub>O</sub>	mid-level	V <sub>DD</sub> - 1.42	—	V <sub>DD</sub> - 1.25	V
	V <sub>OD</sub>	swing (diff)	1.1	—	1.9	V <sub>PP</sub>
	V <sub>SE</sub>	swing (single-ended)	0.55	—	0.95	V <sub>PP</sub>
LVDS Output Option <sup>2</sup>	V <sub>O</sub>	mid-level	1.125	1.20	1.275	V
	V <sub>OD</sub>	swing (diff)	0.5	0.7	0.9	V <sub>PP</sub>
CML Output Option <sup>2</sup>	V <sub>O</sub>	mid-level	—	V <sub>DD</sub> - 0.75	—	V
	V <sub>OD</sub>	swing (diff)	0.70	0.95	1.20	V <sub>PP</sub>
CMOS Output Option <sup>3</sup>	V <sub>OH</sub>	I <sub>OH</sub> = 32 mA	0.8 x V <sub>DD</sub>	—	V <sub>DD</sub>	V
	V <sub>OL</sub>	I <sub>OL</sub> = 32 mA	—	—	0.4	
Rise/Fall time (20/80%)	t <sub>R</sub> , t <sub>F</sub>	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C <sub>L</sub> = 15 pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V <sub>DD</sub> - 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V <sub>DD</sub> /2	45	—	55	%

**Notes:**

- 50 Ω to V<sub>DD</sub> - 2.0 V.
- R<sub>term</sub> = 100 Ω (differential).
- C<sub>L</sub> = 15 pF

**Table 5. CLK± Output Phase Jitter**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) <sup>1,2,3</sup> for F <sub>OUT</sub> ≥ 500 MHz	$\phi_J$	Kv = 33 ppm/V				ps
		12 kHz to 20 MHz (OC-48)	—	0.26	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 45 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.27	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 90 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.32	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 135 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.40	—	
		50 kHz to 80 MHz (OC-192)	—	0.27	—	
Kv = 180 ppm/V						
12 kHz to 20 MHz (OC-48)	—	0.49	—			
50 kHz to 80 MHz (OC-192)	—	0.28	—			
Kv = 356 ppm/V						
12 kHz to 20 MHz (OC-48)	—	0.87	—			
50 kHz to 80 MHz (OC-192)	—	0.33	—			

**Notes:**

1. Differential Modes: LVPECL/LVDS/CML. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest  $K_V$  that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ( $K_V$ ), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCXO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.

Table 5. CLK± Output Phase Jitter (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) <sup>1,2,3</sup> for F <sub>OUT</sub> of 125 to 500 MHz	$\phi_J$	Kv = 33 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.37 0.33	— —	ps
		Kv = 45 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.37 0.33	— —	
		Kv = 90 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.43 0.34	— —	
		Kv = 135 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.50 0.34	— —	
		Kv = 180 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.59 0.35	— —	
		Kv = 356 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	1.00 0.39	— —	

**Notes:**

1. Differential Modes: LVPECL/LVDS/CML. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest  $K_V$  that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ( $K_V$ ), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCXO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.

Table 6. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	$J_{PER}$	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	

\*Note: Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

**Table 7. CLK± Output Phase Noise (Typical)**

Offset Frequency	74.25 MHz 90 ppm/V LVPECL	491.52 MHz 45 ppm/V LVPECL	622.08 MHz 135 ppm/V LVPECL	Units
100 Hz	-87	-75	-65	dBc/Hz
1 kHz	-114	-100	-90	
10 kHz	-132	-116	-109	
100 kHz	-142	-124	-121	
1 MHz	-148	-135	-134	
10 MHz	-150	-146	-146	
100 MHz	n/a	-147	-147	

**Table 8. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T <sub>AMAX</sub>	85	°C
Supply Voltage	V <sub>DD</sub>	-0.5 to +3.8	Volts
Input Voltage	V <sub>I</sub>	-0.5 to V <sub>DD</sub> + 0.3	Volts
Storage Temperature	T <sub>S</sub>	-55 to +125	°C
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	Volts
Soldering Temperature (Pb-free profile) <sup>2</sup>	T <sub>PEAK</sub>	260	°C
Soldering Temperature Time @ T <sub>PEAK</sub> (Pb-free profile) <sup>2</sup>	t <sub>p</sub>	20–40	seconds

**Notes:**

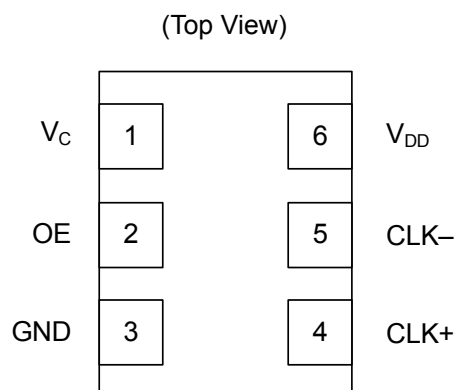
- Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download from [www.silabs.com/VCXO](http://www.silabs.com/VCXO) for further information, including soldering profiles.

**Table 9. Environmental Compliance**

The Si550 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016

## 2. Pin Descriptions



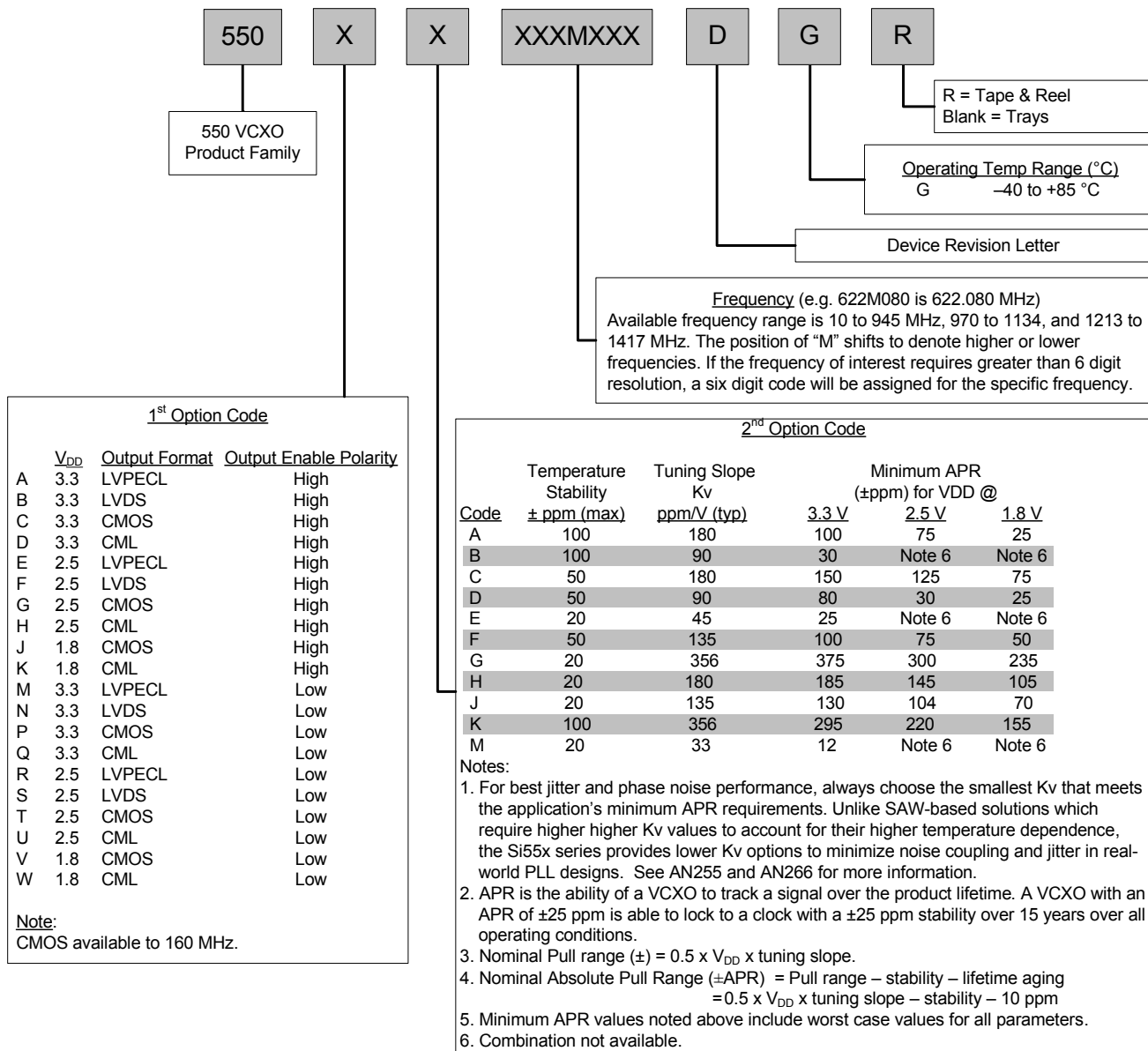
**Table 10. Si550 Pin Descriptions**

Pin	Name	Type	Function
1	$V_C$	Analog Input	Control Voltage
2	OE*	Input	Output Enable (Polarity = High): 0 = clock output disabled (outputs tri-stated) 1 = clock output enabled
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK- (N/A for CMOS)	Output	Complementary Output (N/C for CMOS)
6	$V_{DD}$	Power	Power Supply Voltage

**\*Note:** OE includes 17 k $\Omega$  pullup resistor to  $V_{DD}$ . See Section 3. "Ordering Information" on page 8 for details on OE polarity ordering options.

## 3. Ordering Information

The Si550 supports a variety of options including frequency, temperature stability, tuning slope, output format, and  $V_{DD}$ . Specific device configurations are programmed into the Si550 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to [www.silabs.com/VCXOPartNumber](http://www.silabs.com/VCXOPartNumber) to access this tool and for further ordering instructions. The Si550 VCXO series is supplied in an industry-standard, RoHS compliant, lead-free, 6-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.



Example Part Number: 550AF622M080DGR is a 5 x 7 mm VCXO in a 6 pad package. The nominal frequency is 622.080 MHz, with a 3.3 V supply, LVPECL output, and Output Enable active high polarity. Temperature stability is specified as  $\pm 50$  ppm and the tuning slope is 135 ppm/V. The part is specified for a -40 to +85 °C ambient temperature range operation and is shipped in tape and reel format.

**Figure 1. Part Number Convention**



## 4. Si55x Mark Specification

Figure 2 illustrates the mark specification for the Si550. Table 11 lists the line information.

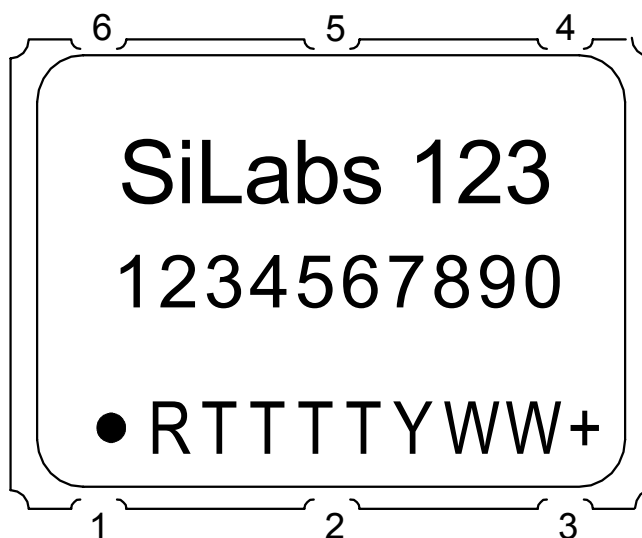


Figure 2. Mark Specification

Table 11. Si55x Top Mark Description

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 5xx (First 3 characters in part number)
2	1–10	Si550: Option1+Option2+Freq(7)+Temp Si552, Si554, Si550 w/ 8-digit resolution: Option1+Option2+ConfigNum(6)+Temp
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

## 5. Outline Diagram and Suggested Pad Layout

Figure 3 illustrates the package details for the Si550. Table 12 lists the values for the dimensions shown in the illustration.

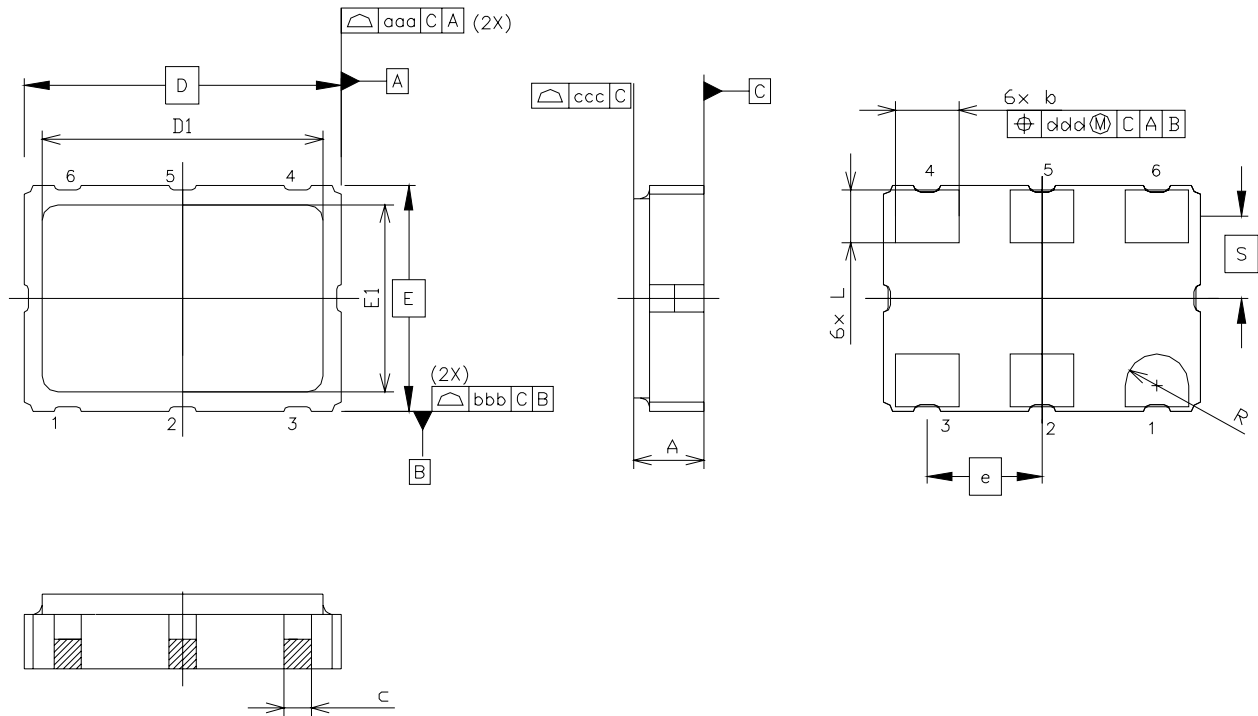


Figure 3. Si550 Outline Diagram

Table 12. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.45	1.65	1.85
b	1.2	1.4	1.6
c	0.60 TYP.		
D	7.00 BSC.		
D1	6.10	6.2	6.30
e	2.54 BSC.		
E	5.00 BSC.		
E1	4.30	4.40	4.50
L	1.07	1.27	1.47
S	1.815 BSC.		
R	0.7 REF.		
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10

## 6. 6-Pin PCB Land Pattern

Figure 4 illustrates the 6-pin PCB land pattern for the Si550. Table 13 lists the values for the dimensions shown in the illustration.

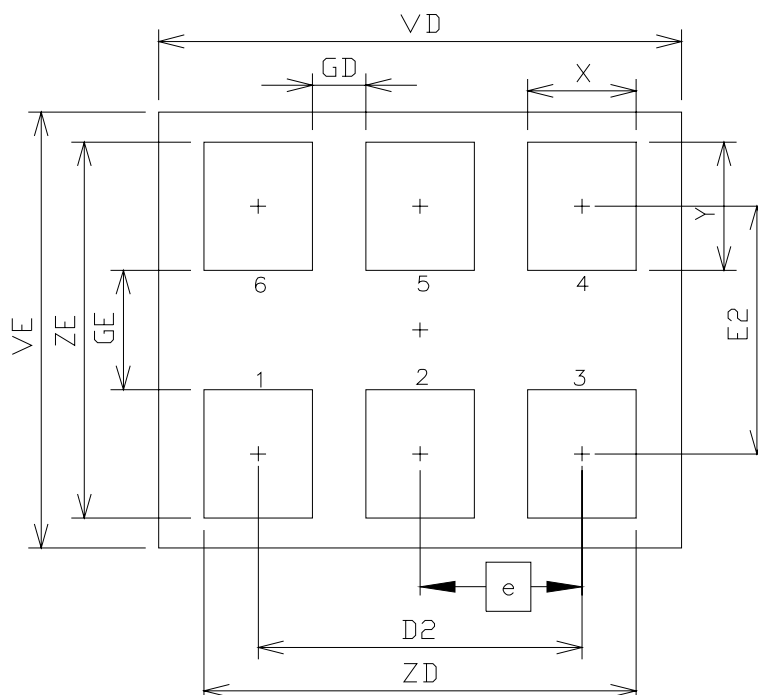


Figure 4. Si550 PCB Land Pattern

Table 13. PCB Land Pattern Dimensions (mm)

Dimension	Min	Max
D2	5.08 REF	
e	2.54 BSC	
E2	4.15 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X	1.70 TYP	
Y	2.15 REF	
ZD	—	6.78
ZE	—	6.30

**Notes:**

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

## DOCUMENT CHANGE LIST

### Revision 0.3 to Revision 0.4

- Updated Table 1, “Recommended Operating Conditions,” on page 2.
  - Added maximum supply current specifications.
  - Specified relationship between temperature at startup and operation temperature.
- Added Output Enable active polarity as an option in Figure 1, “Part Number Convention,” on page 8.

### Revision 0.4 to Revision 0.5

- Updated Note 3 in Table 1, “Recommended Operating Conditions,” on page 2.
- Updated Figure 1, “Part Number Convention,” on page 8.

### Revision 0.5 to Revision 0.6

- Updated Table 1, “Recommended Operating Conditions,” on page 2.
  - Device maintains stable operation over  $-40$  to  $+85$  °C operating temperature range.
  - Supply current specifications updated for revision D.
- Updated Table 4, “CLK $\pm$  Output Levels and Symmetry,” on page 3.
  - Updated LVDS differential peak-peak swing specifications.
- Updated Table 5, “CLK $\pm$  Output Phase Jitter,” on page 4.
- Updated Table 6, “CLK $\pm$  Output Period Jitter,” on page 5.
  - Revised period jitter specifications.
- Updated Table 8, “Absolute Maximum Ratings<sup>1</sup>,” on page 6 to reflect the soldering temperature time at 260 °C is 20–40 sec per JEDEC J-STD-020C.
- Updated 3. “Ordering Information” on page 8.
  - Changed ordering instructions to revision D.
- Added 4. “Si55x Mark Specification” on page 9.

**NOTES:**

## CONTACT INFORMATION

### Silicon Laboratories Inc.

400 West Cesar Chavez

Austin, TX 78701

Tel: 1+(512) 416-8500

Fax: 1+(512) 416-9669

Toll Free: 1+(877) 444-3032

Email: [VCXOinfo@silabs.com](mailto:VCXOinfo@silabs.com)

Internet: [www.silabs.com](http://www.silabs.com)

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories, Silicon Labs, and DSPLL are trademarks of Silicon Laboratories Inc.

Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.