



# FAST CMOS 12-BIT TRI-PORT BUS EXCHANGER

**IDT74FCT16260AT/CT/ET**

## FEATURES:

- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 5V \pm 10\%$
- High drive outputs (-32mA  $I_{OH}$ , 64mA  $I_{OL}$ )
- Power off disable outputs permit "live insertion"
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1.0V at  $V_{cc} = 5V$ ,  $T_A = 25^\circ C$
- Power off disable outputs permit "live insertion"
- Available in SSOP and TSSOP packages

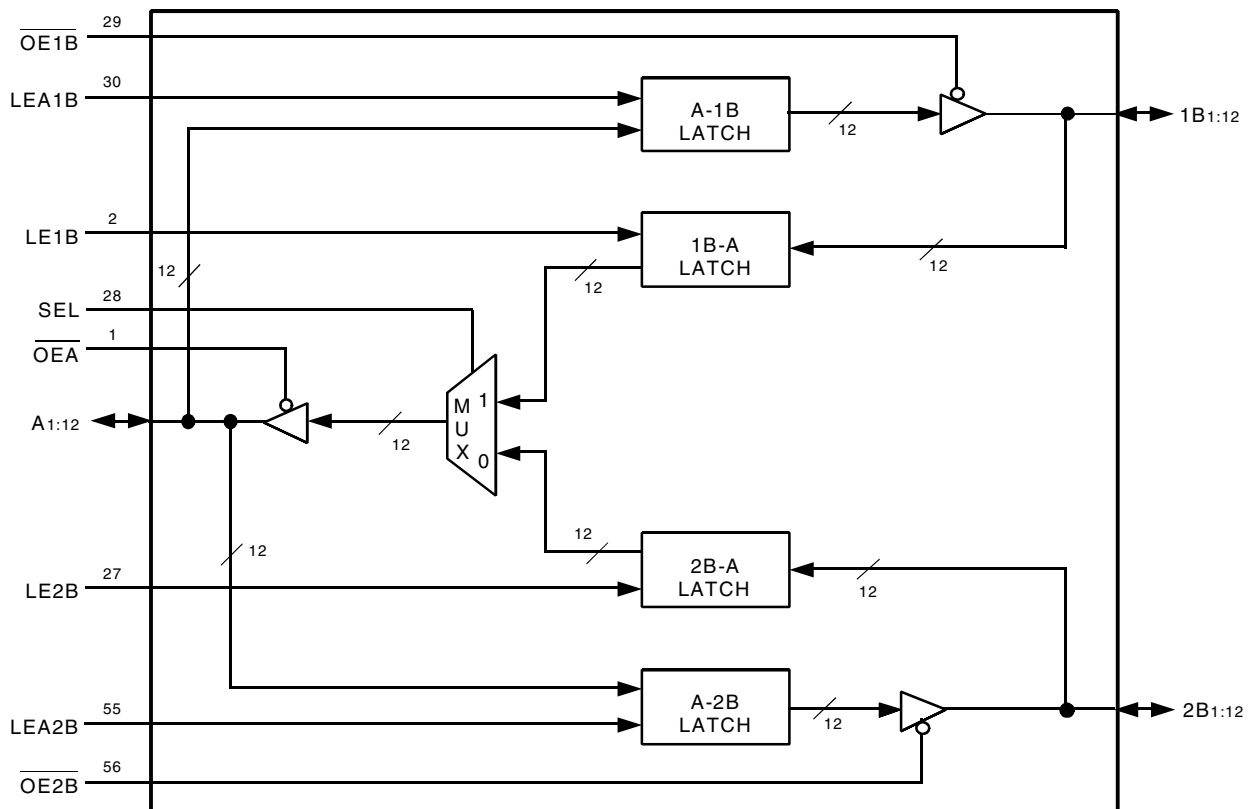
## DESCRIPTION:

The FCT16260T Tri-Port Bus Exchangers are high-speed 12-bit latched bus multiplexers/transceivers for use in high-speed microprocessor applications. These Bus Exchangers support memory interleaving with latched outputs on the B ports and address multiplexing with latched inputs on the B ports.

The Tri-Port Bus Exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The latch enable (LE1B, LE2B, LEA1B and LEA2B) inputs control data storage. When a latch-enable input is high, the latch is transparent. When a latch-enable input is low, the data at the input is latched and remains latched until the latch enable input is returned high. Independent output enables ( $\overline{OE1B}$  and  $\overline{OE2B}$ ) allow reading from one port while writing to the other port.

The FCT16260T is ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

## FUNCTIONAL BLOCK DIAGRAM

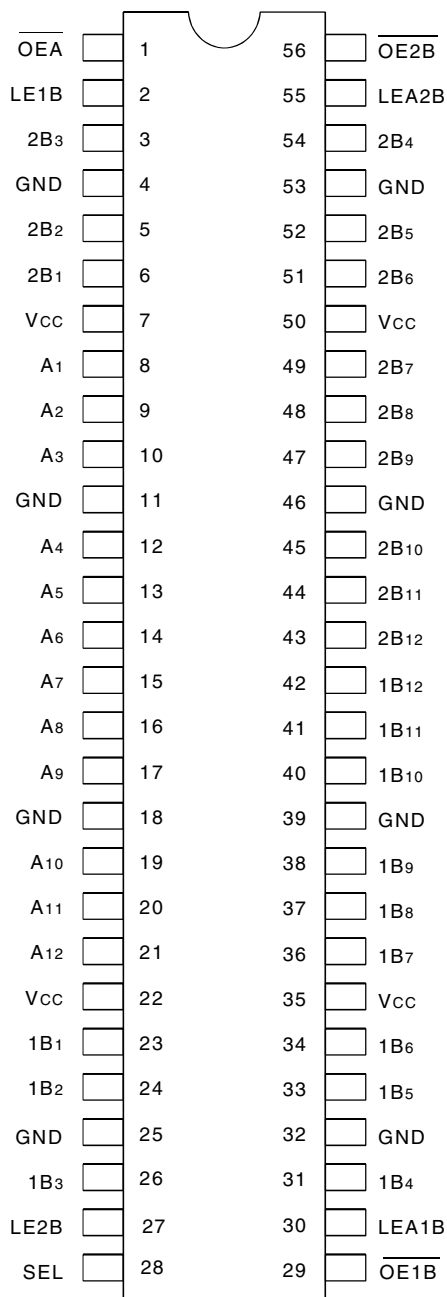


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INDUSTRIAL TEMPERATURE RANGE

JANUARY 2002

PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals for FCT162XXX.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COU	Output Capacitance	VOUT = 0V	3.5	8	pF

NOTE:

1. This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Signal	I/O	Description
A(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.
1B(1:12)	I/O	Bidirectional Data Port 1B. Connected to the even path or even bank of memory.
2B(1:12)	I/O	Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory.
LEA1B	I	Latch Enable Input for A-1B Latch. The Latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B.
LEA2B	I	Latch Enable Input for A-2B Latch. The Latch is open when LEA2B is HIGH. Data from the A-Port is latched on the HIGH to LOW transition of LEA2B.
LE1B	I	Latch Enable Input for the 1B-A Latch. The Latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B.
LE2B	I	Latch Enable Input for the 2B-A Latch. The Latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B.
SEL	I	1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port.
$\overline{OE}A$	I	Output Enable for A Port (Active LOW)
$\overline{OE}1B$	I	Output Enable for 1B Port (Active LOW)
$\overline{OE}2B$	I	Output Enable for 2B Port (Active LOW)

## FUNCTION TABLES<sup>(1)</sup>

Inputs						Output
1B	2B	SEL	LE1B	LE2B	$\overline{OE}A$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A <sup>(1)</sup>
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A <sup>(1)</sup>
X	X	X	X	X	H	Z

Inputs					Outputs	
A	LEA1B	LEA2B	$\overline{OE}1B$	$\overline{OE}2B$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	B <sup>(1)</sup>
L	H	L	L	L	L	B <sup>(1)</sup>
H	L	H	L	L	B <sup>(1)</sup>	H
L	L	H	L	L	B <sup>(1)</sup>	L
X	L	L	L	L	B <sup>(1)</sup>	B <sup>(1)</sup>
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

### NOTES:

- Output level before the indicated steady-state input conditions were established.
- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_i = \text{GND}$	—	—	$\pm 1$	$\mu\text{A}$
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_o = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	5	500	$\mu\text{A}$

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_o$	Output Drive Current	$V_{CC} = \text{Max.}, V_o = 2.5\text{V}^{(3)}$		-50	—	-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -15\text{mA}$	2.4	3.5	—	
			$I_{OH} = -32\text{mA}^{(4)}$	2	3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.2	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN}$ or $V_o \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open One Output Port Enabled $L_{EXX} = V_{CC}$ One Input Bit Toggling One Output Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	60	100	$\mu A/$ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle One Output Port Enabled $L_{EXX} = V_{CC}$ One Input Bit Toggling One Output Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle One Output Port Enabled $L_{EXX} = V_{CC}$ Twelve Input Bits Toggling Twelve Output Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	1.8	3.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	4.8	12.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $GND$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$$

$$I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$$

$$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$$

$$D_H = \text{Duty Cycle for TTL Inputs High}$$

$$N_T = \text{Number of TTL Inputs at } D_H$$

$$I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$$

$$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$$

$$N_{CP} = \text{Number of Clock Inputs at } f_{CP}$$

$$f_i = \text{Input Frequency}$$

$$N_i = \text{Number of Inputs at } f_i$$

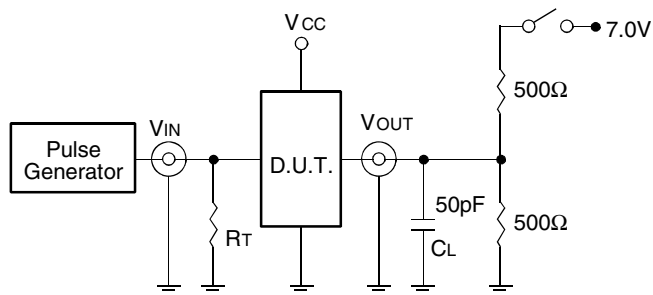
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT16260AT		FCT16260CT		FCT16260ET		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ax to 1Bx or Ax to 2Bx	CL = 50pF RL = 500Ω	1.5	5.2	1.5	4.7	1.5	3.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay 1Bx to Ax or 2Bx to Ax		1.5	5.6	1.5	5	1.5	3.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LExB to Ax		1.5	5.2	1.5	4.7	1.5	4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEA1B to 1Bx or LEA2B to 2Bx		1.5	4.7	1.5	4.4	1.5	4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SEL to Ax		1.5	5.2	1.5	4.7	1.5	4	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OE}A$ to Ax, $\overline{OE}1B$ to 1Bx, or $\overline{OE}2B$ to 2Bx		1.5	5.7	1.5	5.1	1.5	4.4	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OE}A$ to Ax, $\overline{OE}1B$ to 1Bx, or $\overline{OE}2B$ to 2Bx		1.5	4.4	1.5	4	1.5	4	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW Data to Latch		1.5	—	1	—	1	—	ns
t <sub>H</sub>	Hold Time, Latch to Data		1	—	1	—	1	—	ns
t <sub>w</sub>	Pulse Width, Latch HIGH <sup>(4)</sup>		3	—	3	—	3	—	ns
t <sub>SK(φ)</sub>	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	—	0.5	ns

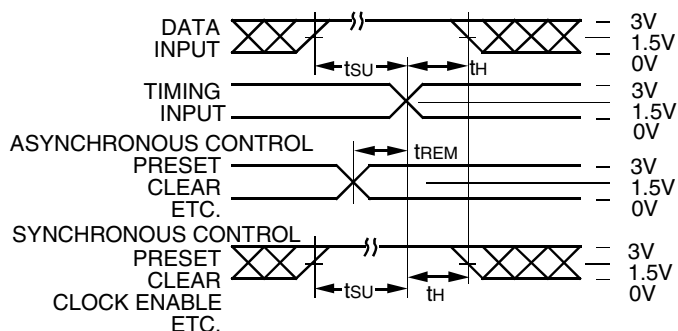
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

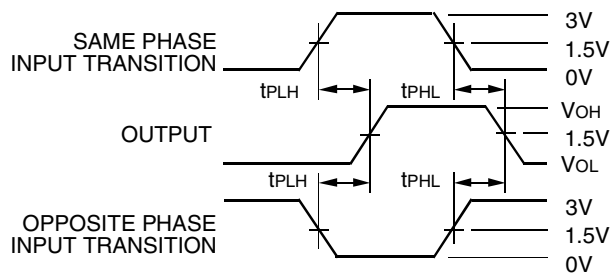
## TEST CIRCUITS AND WAVEFORMS



*Test Circuits for All Outputs*



*Set-up, Hold, and Release Times*



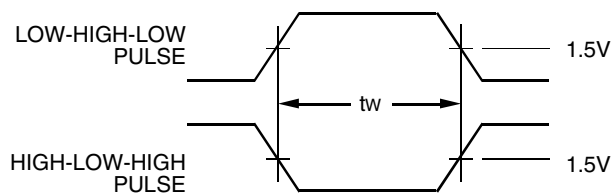
*Propagation Delay*

## SWITCH POSITION

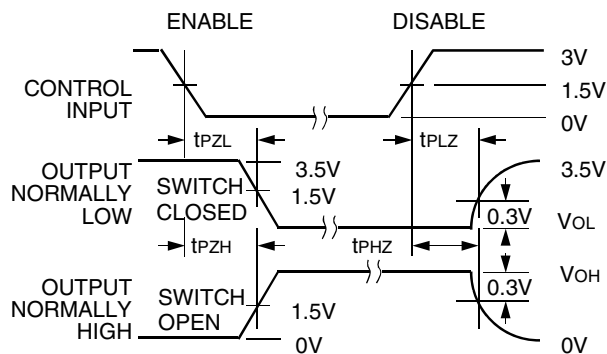
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

**DEFINITIONS:**

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



*Pulse Width*

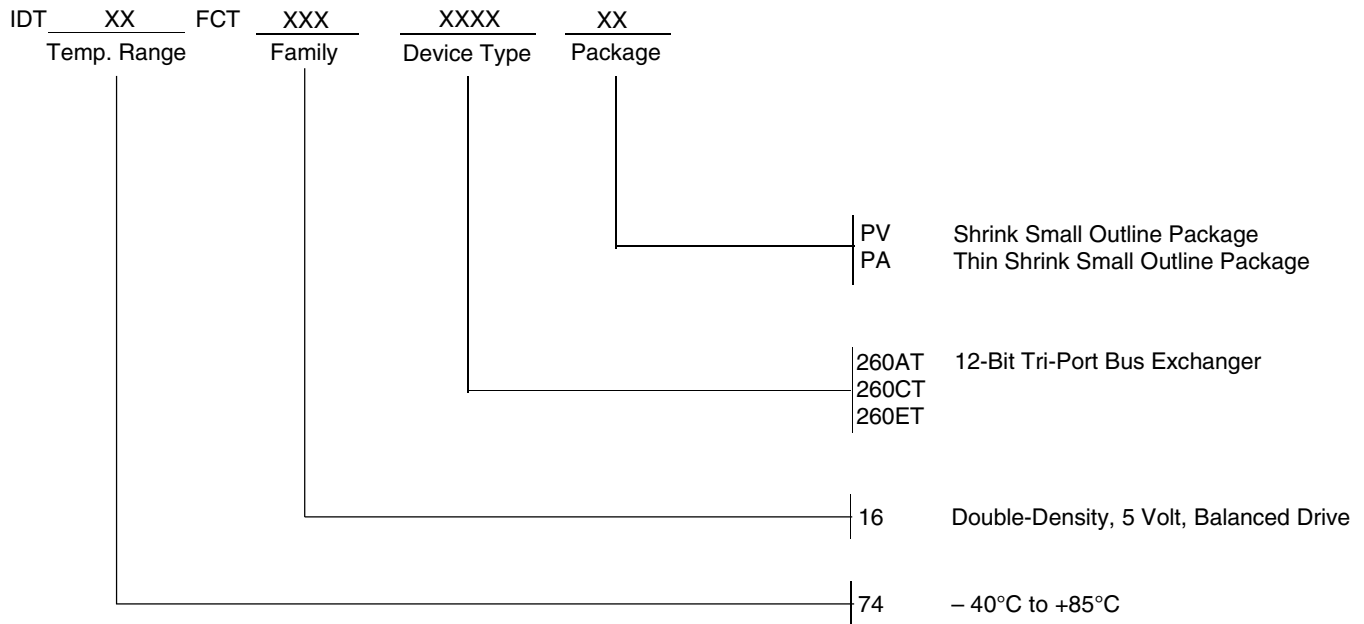


*Enable and Disable Times*

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
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