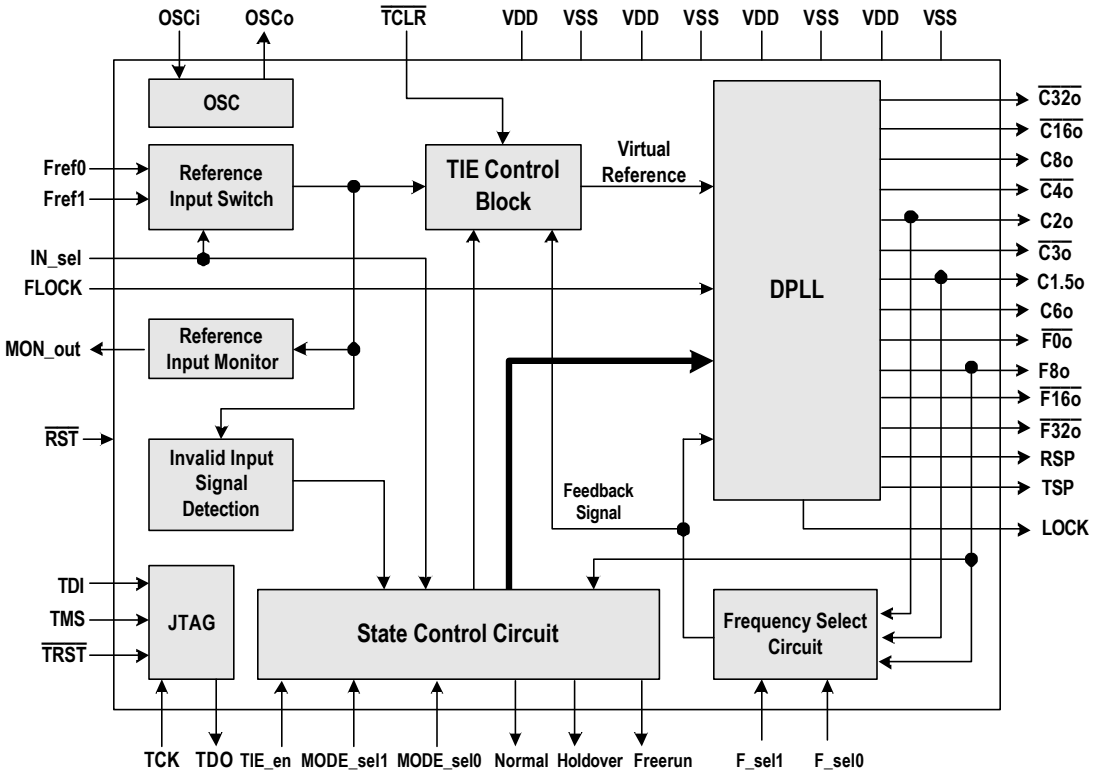
WAN PLL WITH DUAL REFERENCE INPUTS

PRELIMINARY
IDT82V3002

FEATURES

- Supports AT&T TR62411 and Telcordia GR-1244-CORE Stratum 3, Stratum 4 Enhanced and Stratum 4 timing for DS1 interfaces
- Supports ITU-T G.813 Option 1 clocks for 2048 kbit/s interfaces
- Supports ITU-T G.812 Type IV clocks for 1544 kbit/s interface and 2048 kbit/s interfaces
- Supports ETSI ETS 300 011, TBR 4, TBR 12 and TBR 13 timing for E1 interface
- Selectable input reference signal: 8 kHz, 1.544 MHz or 2.048 MHz
- Accepts reference inputs from two independent sources
- Provides C1.5o, $\overline{C3o}$, C2o, $\overline{C4o}$, C6o, C8o, $\overline{C16o}$ and $\overline{C32o}$ output clock signals
- Provides six types of 8 kHz framing pulses: $\overline{F0o}$, F8o, $\overline{F16o}$, $\overline{F32o}$, RSP and TSP
- Holdover frequency accuracy of 0.025 ppm
- Phase slope of 5 ns/125 ms
- Attenuates wander from 2.1 Hz
- Fast lock mode
- Provides Time Interval Error (TIE) correction
- MTIE of 600 ns
- JTAG boundary scan
- Holdover status indication
- Freerun status indication
- Normal status indication
- Lock status indication
- Input primary reference quality indication
- 3.3 V operation with 5 V tolerant I/O
- Package available: 56 pin SSOP

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

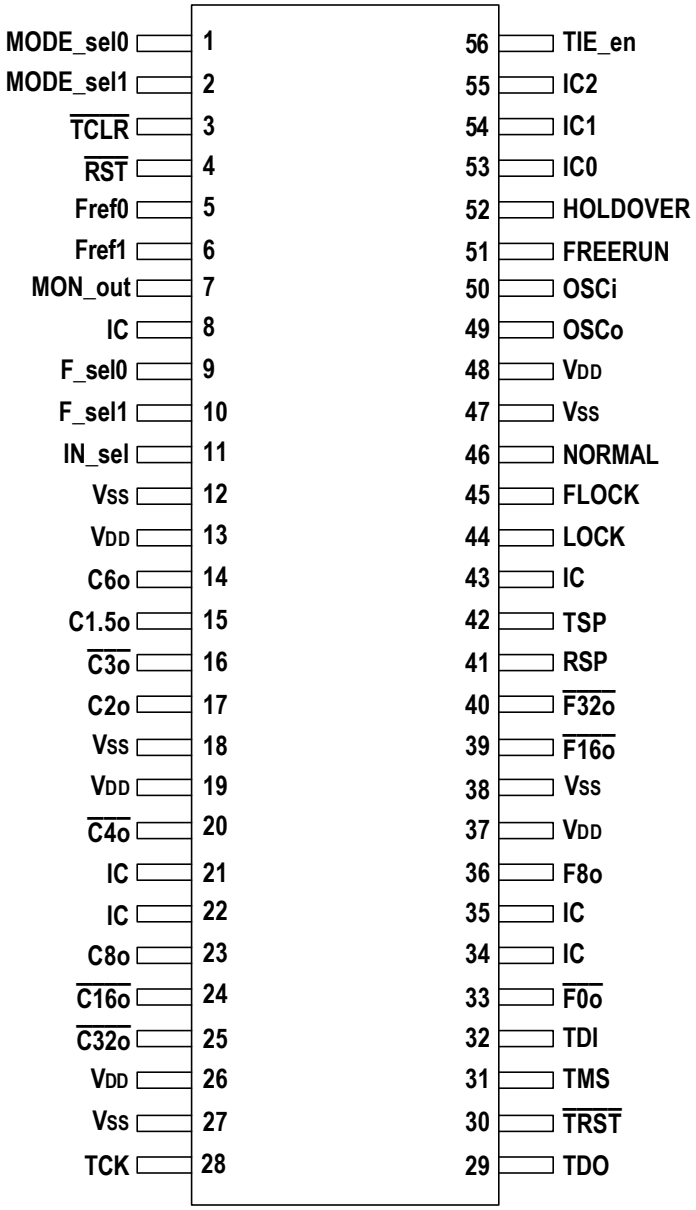
The IDT82V3002 is a WAN PLL with dual reference inputs. It contains a Digital Phase-Locked Loop (DPLL), which generates ST-BUS clocks and framing signals that are phase locked to the 2.048 MHz, 1.544 MHz or 8 kHz input reference.

The IDT82V3002 provides eight types of clock signals (C1.5o, $\overline{C3o}$, C6o, C2o, $\overline{C4o}$, C8o, $\overline{C16o}$, $\overline{C32o}$) and six types of framing signals ($\overline{F0o}$, F8o, $\overline{F16o}$, $\overline{F32o}$, RSP, TSP) for the multitrunk T1 and E1 primary rate transmission links.

The IDT82V3002 is compliant with AT&T TR62411, Telcordia GR-1244-CORE Stratum 3, Stratum 4 Enhanced and Stratum 4, ETSI ETS 300 011, ITU-T G.813 Option 1 for 2048 kbit/s interface, and ITU-T G.812 Type IV clocks for 1544 kbit/s interface and 2048 kbit/s interface. It meets the jitter/wander tolerance, jitter/wander transfer, intrinsic jitter/wander, frequency accuracy, capture range, phase change slope, holdover frequency accuracy and MTIE (Maximum Time Interval Error) requirements for these specifications.

The IDT82V3002 can be used in synchronization and timing control for T1 and E1 systems, or used as ST-BUS clock and frame pulse sources. It also can be used in access switch, access routers, ATM edge switches, wireless base station controllers, or IADs (Integrated Access Devices), PBXs and line cards.

PIN CONFIGURATIONS



PIN DESCRIPTION

Name	Type	Pin Number	Description
V_{SS}	Power	12, 18, 27 38, 47	**Ground**. 0 V. All V_{SS} pins should be connected to the ground.
V_{DD}	Power	13, 19, 26 37, 48	**Positive Supply Voltage**. All V_{DD} pins should be connected to +3.3 V nominal.
OSCo	(CMOS) O	49	**Oscillator Master Clock**. For crystal operation, a 20 MHz crystal is connected from this pin to OSCi. For clock oscillator operation, this pin is left unconnected.
OSCi	(CMOS) I	50	**Oscillator Master Clock.** For crystal operation, a 20 MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin is connected to a clock source.
Fref0	I	5	**Reference Input 0.** This is one of the input reference sources (falling edge) used for synchronization. One of three possible frequencies (8 kHz, 1.544 MHz, or 2.048 MHz) may be used. The selection of the input reference is based upon IN_sel control input. See Table 3. The Fref0 pin is internally pulled up to V_{DD}.
Fref1	I	6	**Reference Input 1.** See Pin description for Fref0. This pin is internally pulled up to V_{DD}.
IN_sel	I	11	**Reference Switch Input Control.** A logic low selects Reference Input 0 (Fref0) and a logic high selects Reference Input 1 (Fref1). The logic level of this input is gated in by the rising edge of F8o. This Pin is internally pulled down to V_{SS}.
F_sel1	I	10	**Input Frequency Select 1 .** This input, in conjunction with F_sel0, selects which of three possible frequencies (8 kHz, 1.544 MHz, or 2.048 MHz) may be input to the Reference Input 0 and Reference Input 1. See Table 2.
F_sel0	I	9	**Input Frequency Select 0.** See Pin description for F_sel1.
MODE_sel1	I	2	**Mode/Control Select 1**. This input, in conjunction with MODE_sel0, determines the state (Normal, Holdover or Freerun) of operation. The logic level at this input is gated in by the rising edge of F8o. This pin is internally pulled down to V_{SS}. See Table 1.
MODE_sel0	I	1	**Mode/Control Select 0**. See pin description for MODE_sel1.The logic level at this input is gated in by the rising edge of F8o This pin is internally pulled down to V_{SS}.
$\overline{RST}$	I	4	**Reset Input.** A logic low at this pin resets the IDT82V3002. To ensure proper operation, the device must be reset after reference signal frequency changes and power-up. The $\overline{RST}$ pin should be held low for a minimum of 300 ns. While the $\overline{RST}$ pin is low, all framing and clock outputs are at logic high.
$\overline{TCLR}$	I	3	**TIE Circuit Reset.** Logic low at this input resets the TIE (Maximum Time Interval Error) control block resulting in a realignment of output phase with input phase. The $\overline{TCLR}$ pin should be held low for a minimum of 300 ns. This pin is internally pulled up to V_{DD}.
TIE_en	I	56	**TIE Enable.** A logic high at this pin enables the TIE control block while a logic low at this pin disables the TIE control block. The logic level at this input is gated in by the rising edging of F8o. This pin is internally pulled up to V_{DD}.
FLOCK	I	45	**Fast Lock Mode**. Set high to allow the DPLL to quickly lock to the input reference (less than 500 ms locking time).
LOCK	(CMOS) O	44	**Lock Indicator**. This output goes high when the DPLL is frequency locked to the input reference.
HOLDOVER	(CMOS) O	52	**Holdover Indicator**. This output goes to a logic high whenever the DPLL goes into Holdover Mode.
NORMAL	(CMOS) O	46	**Normal Indicator.** This output goes to a logic high whenever the DPLL goes into Normal Mode.

PIN DESCRIPTION (CONTINUED)

Name	Type	Pin Number	Description
FREERUN	(CMOS) O	51	**Freerun Indicator**. This output goes to a logic high whenever the DPLL goes into Freerun Mode.
MON_out	O	7	**Monitor Reference Out Of Capture Range**. A logic high at this pin indicates that the reference is off the nominal frequency by more than ±12ppm.
$\overline{C32o}$	(CMOS) O	25	**Clock 32.768 MHz**. This output is used for ST-BUS operation with a 32.768 MHz clock.
$\overline{C16o}$	(CMOS) O	24	**Clock 16.384 MHz**. This output is used for ST-BUS operation with a 16.384 MHz clock.
C8o	(CMOS) O	23	**Clock 8.192 MHz**. This output is used for ST-BUS operation with an 8.192 MHz clock.
$\overline{C4o}$	(CMOS) O	20	**Clock 4.096 MHz**. This output is used for ST-BUS operation with a 4.096 MHz clock.
C2o	(CMOS) O	17	**Clock 2.048 MHz**. This output is used for ST-BUS operation with a 2.048 MHz clock.
$\overline{C3o}$	(CMOS) O	16	**Clock 3.088 MHz**. This output is used for T1 applications.
C1.5o	(CMOS) O	15	**Clock 1.544 MHz**. This output is used for T1 applications.
C6o	(CMOS) O	14	**Clock 6.312 MHz.** This output is used for DS2 applications.
$\overline{F32o}$	(CMOS) O	40	**Frame Pulse ST-BUS 8.192 Mb/s**. This is an 8 kHz 31 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s.
$\overline{F16o}$	(CMOS) O	39	**Frame Pulse ST-BUS 8.192 Mb/s**. This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s.
F8o	(CMOS) O	36	**Frame Pulse.** This is an 8 kHz 122 ns active high framing pulse, which marks the beginning of a frame.
$\overline{F0o}$	(CMOS) O	33	**Frame Pulse ST-BUS 2.048 Mb/s**. This is an 8 kHz 244 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s.
RSP	(CMOS) O	41	**Receive Sync Pulse**. This is an 8 kHz 488 ns active high framing pulse, which marks the beginning of a ST-BUS frame. This is typically used for connection to the Siemens MUNICH-32 device.
TSP	(CMOS) O	42	**Transmit Sync Pulse.** This is an 8 kHz 488 ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for connection to the Siemens MUNICH-32 device.
TDO	(CMOS) O	29	**Test Serial Data Out**. JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TDI	I	32	**Test Serial Data In**. JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}.
$\overline{TRST}$	I	30	**Test Reset**. Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin is internally pulled up to V_{DD}. It is connected to the ground for normal applications.
TCK	I	28	**Test Clock.** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}.
TMS	I	31	**Test Mode Select**. JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}.
IC0, IC1, IC2	-	53, 54, 55	**These pins should be connected to V_{SS}.**
IC	-	8, 21, 22, 34 35, 43	**These pins should be left open.**

FUNCTIONAL DESCRIPTION

The IDT82V3002 is a WAN PLL with dual reference inputs, providing timing (clock) and synchronization (framing) signals to interface circuits for T1 and E1 Primary Rate Digital Transmission links. See the functional block diagram. The detail is described in the following sections.

STATE CONTROL CIRCUIT

The State Control Circuit is an important part in the IDT82V3002. As shown in Figure 1, based on the DPLL mode selection inputs MODE_sel0 and MODE_sel1, reference selection input IN_sel, TIE enable input TIE_en and the result of the Invalid Input Signal Detection, the State Control Circuit outputs signals to enable/disable the TIE Control Block and control the work mode of the DPLL Block.

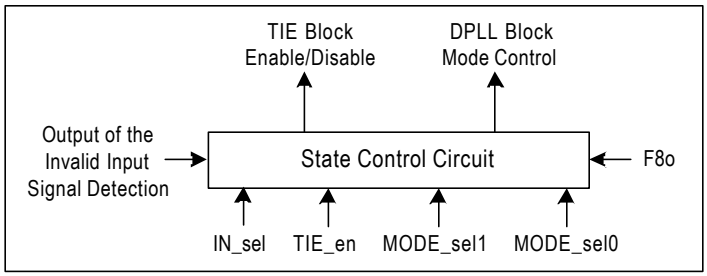


Figure 1. State Control Block

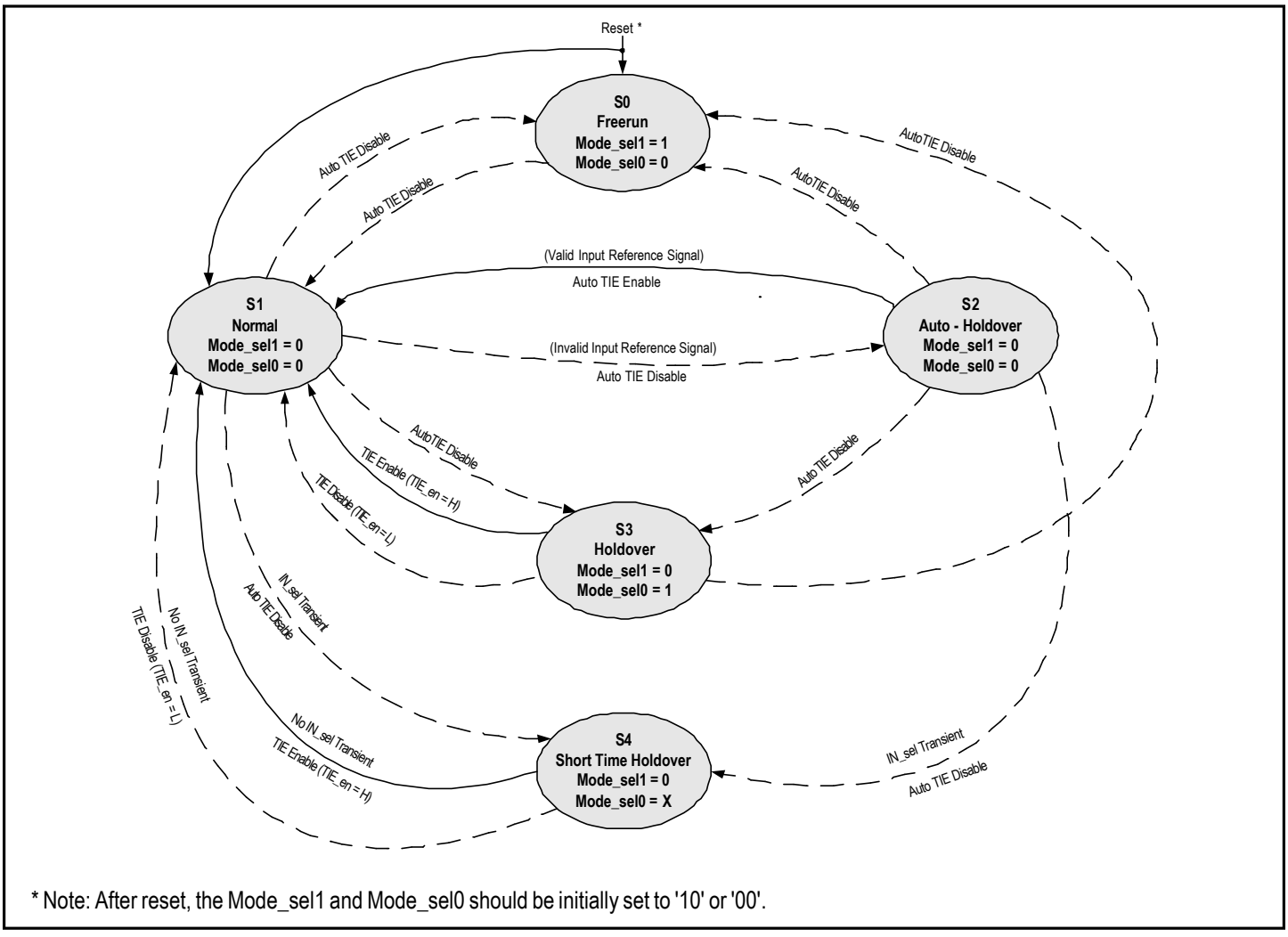
The IDT82V3002 has three possible modes of operation: Normal, Holdover and Freerun. The Mode Select pins MODE_sel1 and MODE_sel0 select the operation mode, see Table 1.

TABLE 1 —— OPERATING MODES AND STATUS

MODE_sel1	MODE_sel0	Mode
0	0	Normal
0	1	Holdover
1	0	Freerun
1	1	Reserved

Figure 2 shows the state control diagram. All state changes occur synchronously on the rising edge of F8o. The three operating modes, Normal (S1), Holdover (S3) and Freerun (S0) can be switched from one to another by changing the MODE_sel0 and MODE_sel1 logic levels.

The mode changes between Normal (S1) and Auto-Holdover (S2) are triggered by the Invalid Input Reference Detection Circuit and irrelative to the logic levels on MODE_sel0 and MODE_sel1 pins. That is, when the IDT82V3002 is operating in the Normal mode (S1), if an invalid input reference is detected (input reference is out of the capture range), the operating mode will be changed automatically from Normal (S1) to Auto-



* Note: After reset, the Mode_sel1 and Mode_sel0 should be initially set to '10' or '00'.

Figure 2. State Control Diagram

Holdover (S2). At the stage of S2, if an IN_sel transient is detected, the device will change to the Short Time Holdover Mode (S4) with the TIE Control Block disabled. Otherwise, if the input reference becomes valid, the device will be changed back to Normal (S1) automatically. Refer to "Invalid Input Reference Detection" for more information.

While the changes between Normal (S1) and Short Time Holdover (S4) is determined by the IN_sel pin, which controls the input reference selection. A transient voltage occurs at the In_sel pin will make the device change from Normal (S1) to Short Time Holdover (S4) automatically. See "Reference Input Switch" for details.

When the operating mode is changed from one state to another, the TIE control block will be enabled or disabled automatically as shown along the lines in Figure 2, except the changes from Holdover (S3) to Normal (S1) and from Short Time Holdover (S4) to Normal (S1), which depend on the logic level of the TIE_en pin.

Normal Mode

The Normal Mode is typically used when a slave clock source synchronized to the network is required.

In this mode, the IDT82V3002 provides timing (C1.5o, $\overline{C3o}$, C2o, $\overline{C4o}$, C8o, $\overline{C16o}$ and $\overline{C32o}$) and synchronization ($\overline{F0o}$, F8o, $\overline{F16o}$, $\overline{F32o}$, TSP, RSP) signals, which are synchronous to one input reference. The input reference signal have a nominal frequency of 8 kHz, 2.048 MHz or 1.544 MHz.

From a reset condition, the IDT82V3002 will take maximum 30 seconds to make the output signals synchronous (phase locked) to the input reference.

Whenever the IDT82V3002 enters Normal Mode, it will give an indication by setting the NORMAL pin high.

Fast Lock Mode

Fast Lock Mode is a submode of Normal Mode, it is used for the IDT82V3002 to lock to a reference more quickly than in Normal Mode. Typically, the DPLL will lock to the input reference within 500 ms if the FLOCK pin is high.

Holdover Mode

Holdover Mode is typically used for short duration (e.g., 2 seconds) while network synchronization is temporarily disrupted.

In Holdover Mode, the IDT82V3002 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal.

In Normal Mode, when the output frequency is locked to the input reference signal, a numerical value corresponding to the output frequency is stored alternately in two memory locations every 30 ms. When the device is switched into Holdover Mode, the stored value from between 30 ms and 60 ms is used to set the output frequency of the device.

The frequency accuracy of Holdover Mode is ±0.025 ppm, which corresponds to a worst case of 18 frame (125 µs per frame) slips in 24 hours. This meets the AT&T TR62411 and Telcordia GR-1244-CORE Stratum 3 requirement of ±0.37 ppm (255 frame slips per 24 hours).

The HOLDOVER pin is set to logic high whenever the IDT82V3002 goes into the Holdover Mode.

Freerun Mode

Freerun Mode is typically used when a master clock source is required, or used when a system is just powered up and the network synchronization has not been achieved.

In Freerun Mode, the IDT82V3002 provides timing and synchronization signals which are based on the master clock frequency (OSCi) only, and are not synchronized to the input reference signal.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32 ppm output clock is required, the master clock must also be ±32 ppm. Refer to the "OSC" section for more information.

The FREERUN pin goes high whenever the IDT82V3002 works in Freerun Mode.

FREQUENCY SELECT CIRCUIT

The frequency of the input reference can be 8 kHz, 1.544 MHz or 2.048 MHz. As shown in Table 2, the F_sel1 and F_sel0 pins determine which of the three frequencies is selected for the reference. Note that both the reference inputs Fref0 and Fref1 must have the same frequency applied to them. Every time the frequency selection is changed, the device must be reset to make the change effective.

TABLE 2 —— INPUT REFERENCE SELECTION

F_sel1	F_sel0	Input Frequency
0	0	Reserved
0	1	8 kHz
1	0	1.544 MHz
1	1	2.048 MHz

REFERENCE INPUT SWITCH

The IDT82V3002 accepts two simultaneous reference input signals Fref0 and Fref1, and operates on the falling edges. The reference is selected by the IN_sel pin, as shown in Table 3. The selected reference signal is sent to the TIE control block, Reference Input Monitor and Invalid Input Signal Detection block to be further processed.

TABLE 3 ¾ REFERENCE INPUT SWITCH CONTROL

IN_sel	Input Reference
0	Fref0
1	Fref1

When a transient voltage occurs at the IN_sel pin, the IDT82V3002 will automatically switch to the Short Time Holdover Mode (S4) with the TIE Control Block disabled. At the S4 stage, if no IN_sel transient occurs, the reference signal will be changed from one to the other and the device will switch back to the Normal Mode (S1) automatically. During the change from S4 to S1, the TIE Control Block can be manually enabled or disabled. See Figure 2 for full details.

REFERENCE INPUT MONITOR

The Telcordia GR-1244-CORE standard recommends that the DPLL should be able to reject the references that are off the nominal frequency by more than ±12 ppm. The IDT82V3002 monitors TIE Control Block input frequency and outputs a MON_out signal to indicate the monitoring result. Whenever the reference frequency is off the nominal frequency by more than ±12 ppm, the MON_out pin goes high. The MON_out signal is updated every 2 second.

INVALID INPUT SIGNAL DETECTION

This circuit monitors the input reference signal to the IDT82V3002 and

automatically enables the Holdover Mode (Auto-Holdover) when the frequency of the incoming signal is out of the capture range (See AC Electrical Characteristics - Performance). This includes a complete loss of input reference, or a large frequency shift in the input reference. When the input reference returns to normal, the DPLL returns to Normal Mode with the output signal locked to the input reference signal. The holdover output signal in the IDT82V3002 is based on the input reference signal 30 ms to 60 ms prior to entering the Holdover Mode. The amount of phase drift while in holdover is negligible because the Holdover Mode is very accurate (e.g., 0.025 ppm). Consequently, the phase delay between the input and output after switching back to Normal Mode is preserved.

TIE CONTROL BLOCK

If the current reference is badly damaged or lost, it is necessary to use the other reference or the one generated by the storage techniques instead. But when switching the reference, a step change in phase on the input reference will occur. And a step change in phase at the input of the DPLL would lead to unacceptable phase changes in the output signals. The TIE control block, when enabled, prevents a step change in phase on the input reference signals from causing a step change in phase at the output of the DPLL block. Figure 3 shows the TIE Control Block diagram.

When the TIE Control Block is enabled (by the TIE_en pin or TIE auto-enable logic generated by the State Control Circuit), it will work under the control of the Step Generation circuit.

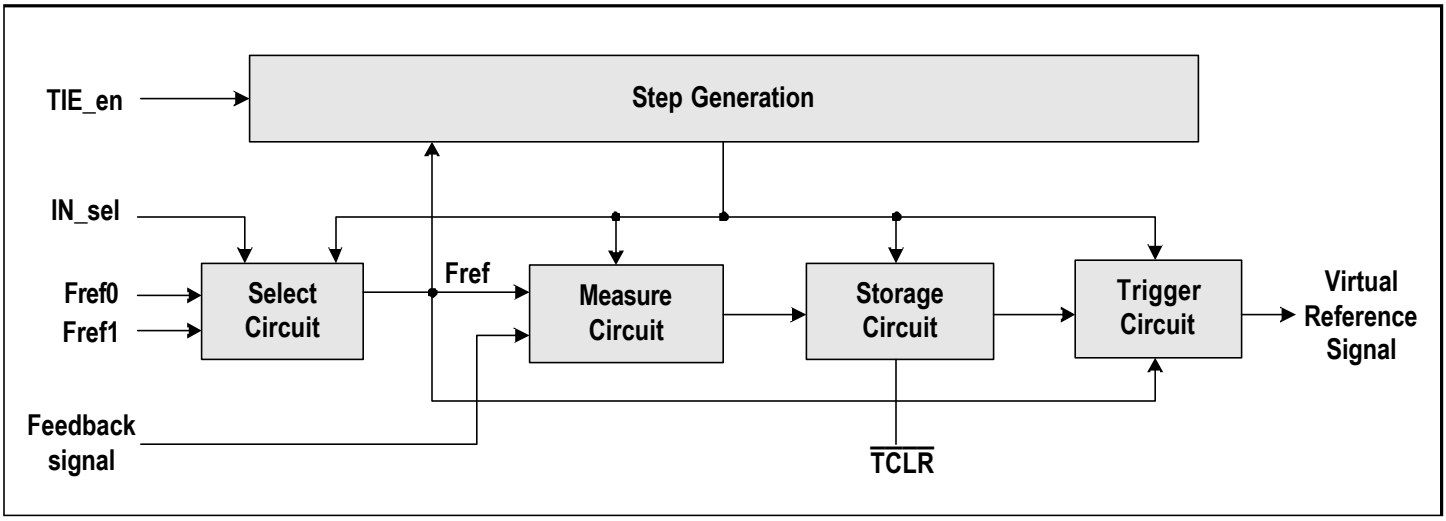


Figure 3. TIE Control Circuit Diagram

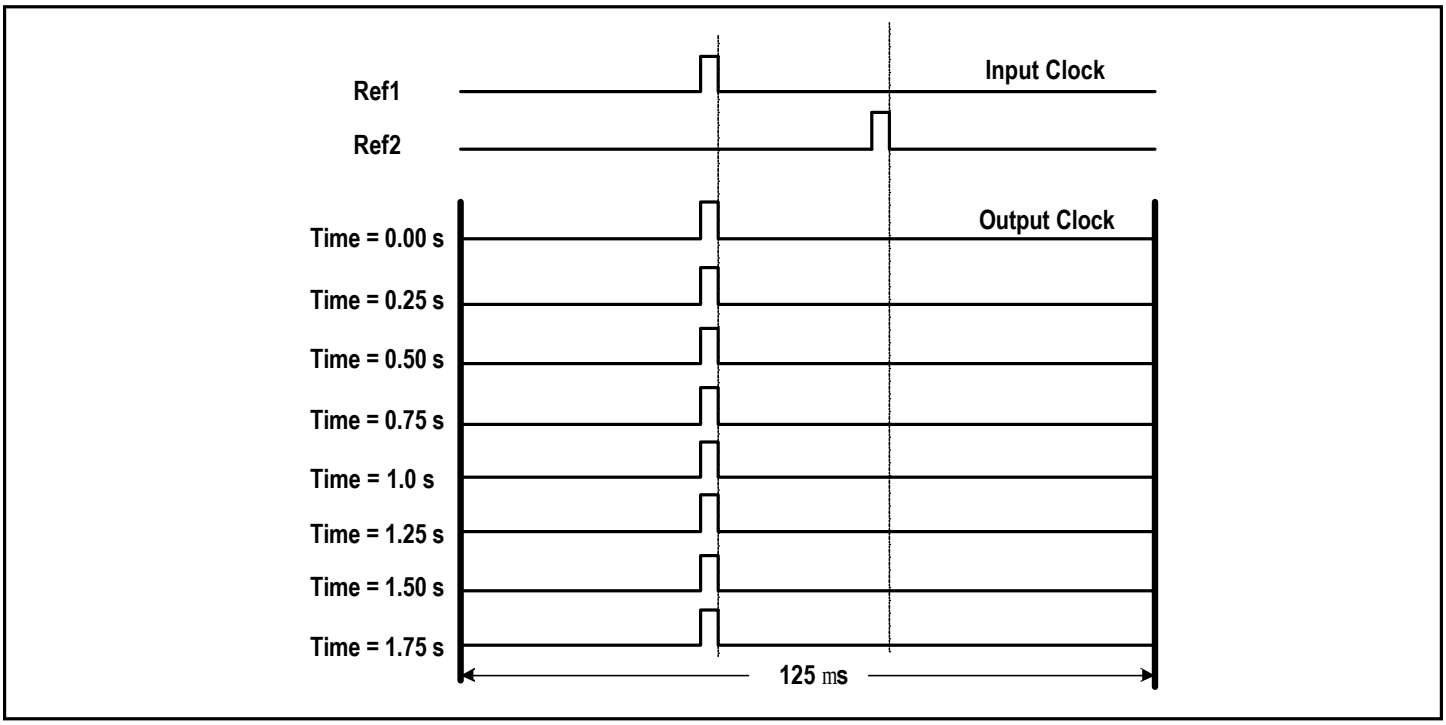


Figure 4. Reference Switch with TIE Control Block Enabled

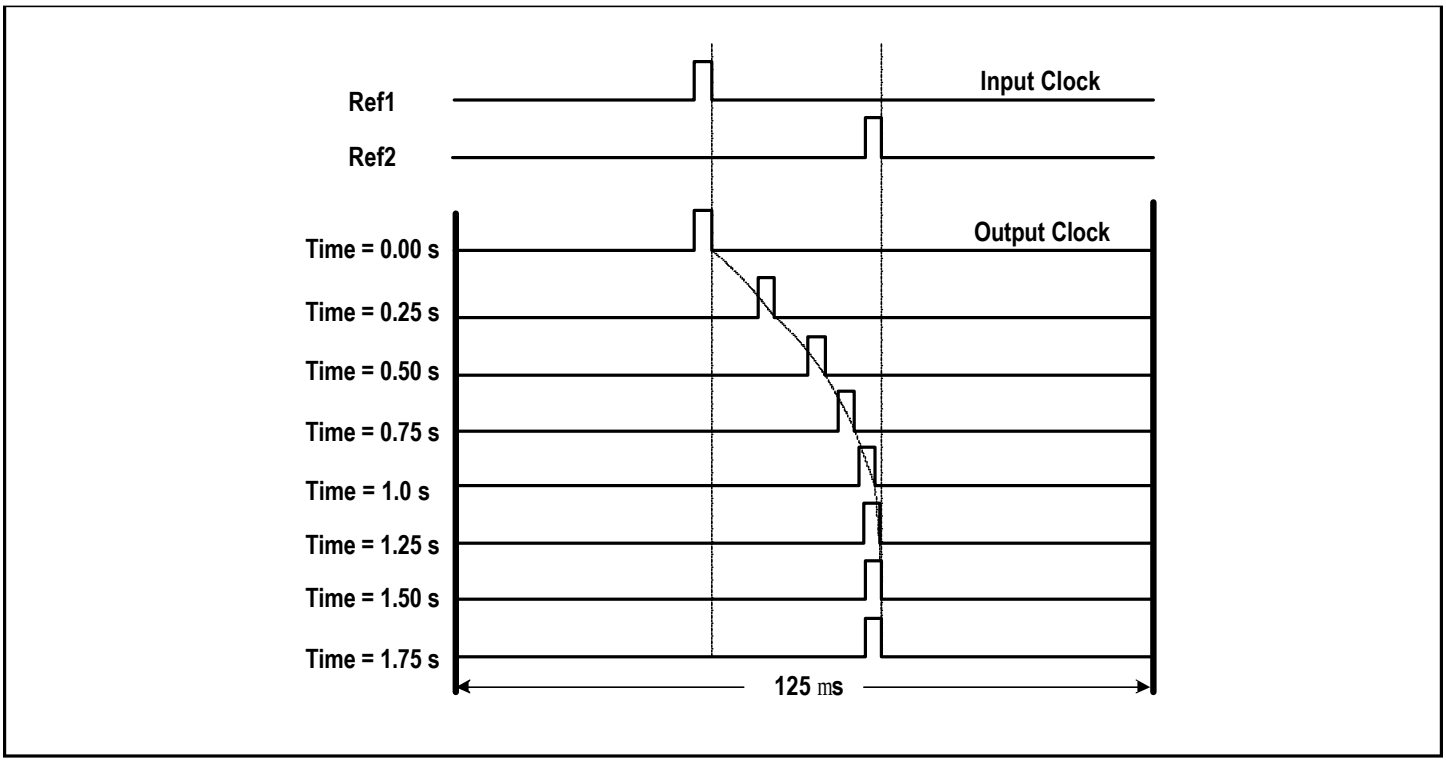


Figure 5. Reference Switch with TIE Control Block Disabled

The selected reference signal is compared with the feedback signal (current output feedback from the Frequency Select Circuit) by the Measure Circuit. The phase difference between input reference and the feedback signal is sent to the Storage Circuit for TIE correction. The Trigger Circuit, depending on the value stored in the Storage Circuit, generates a virtual reference with the phase corrected to the same position as the previous reference. With this TIE correction mechanism, the reference is switched without generating a step change in phase.

Figure 4 shows the phase transient that would result if a reference switch is performed with the TIE Control Block enabled.

The value of the phase difference in the Storage Circuit can be cleared by applying a logic low pulse to the TIE Control Circuit reset pin $\overline{TCLR}$. The reset pulse should be at least 300 ns.

When the IDT82V3002 primarily enters Holdover Mode for short time periods and then turns back to Normal Mode, the TIE Control Circuit should not be enabled. This will prevent unwanted accumulated phase change between the input and output.

If the TIE Control Block is disabled (by the TIE_en pin or TIE auto-disable logic generated by the State Control Circuit) during the reference switching, the phase of the output signal will align with the new reference, with the phase slope limited to 5 ns per 125 µs. Figure 5 shows the phase transient results from a reference switch with the TIE Control Block disabled.

DPLL BLOCK

As shown in Figure 6, the DPLL Block consists of a Phase Detector, a Limiter, a Loop Filter, a Digital Control Oscillator and Divider Circuits.

Phase Detector (PHD)

In Normal Mode, the Phase Detector compares the virtual reference signal from the TIE Control Circuit with the feedback signal from the Frequency Select Circuit, and outputs an error signal corresponding to the phase difference between the two. This error signal is then sent to the Limiter circuit for phase slope control.

The feedback signal can be 8 kHz, 2.048 MHz or 1.544 MHz, selected by pins F_sel1 and F_sel0. Refer to Table 2 for details.

In Freerun or Holdover Mode, the Frequency Select Circuit, the Phase Detector and the Limiter are not active and the input reference signal is not used.

Limiter

The Limiter is used for ensuring that the DPLL responds to all input transient conditions with a maximum output phase slope of 5ns per 125 µs. This well meets the AT&T TR62411 and Telcordia GR-1244-CORE specifications, which specify the maximum phase slope of 7.6 ns per 125 µs and 81 ns per 1.326 ms, respectively.

In Normal Mode, the Limiter receives the error signal from the Phase Detector, limits the phase slope within 5 ns per 125 µs and sends the limited signal to the Loop Filter.

The fast lock mode is a submode of the Normal Mode. By setting the FLOCK pin high, the device will enter fast lock mode. In this case, the Limiter is disabled, the DPLL will lock to the incoming reference within 500 ms, which is much shorter than that needed in Normal Mode.

Loop Filter

The Loop Filter ensures that the jitter transfer meets the ETS 300 011 and AT&T TR624411 requirements. This Loop Filter works similarly to a first order low pass filter with 2.1 Hz cutoff frequency for the three valid input reference signals (8 kHz, 2.048 MHz or 1.544 MHz).

The output of the Loop Filter goes directly or through the Fraction blocks

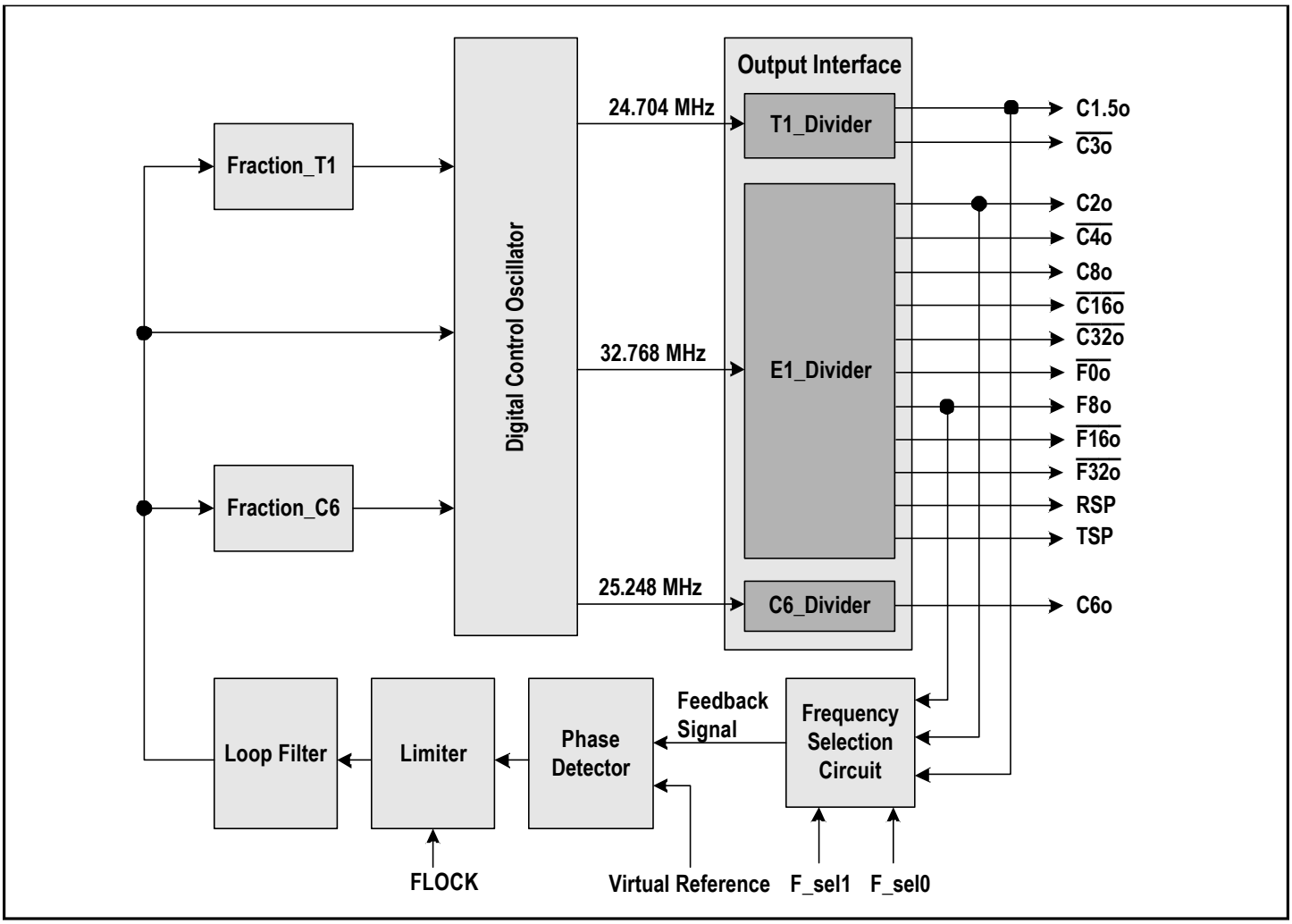


Figure 6. DPLL Block Diagram

to the Digital Control Oscillator, at which a E1, T1 and C6 signals are generated.

Fraction Block

By applying some algorithms on the incoming E1 signal, the Fraction_C6 and Fraction_T1 blocks generate C6 and T1 signals, respectively.

Digital Control Oscillator (DCO)

In Normal Mode, the DCO receives the three limited and filtered signals from Loop Filter or Fraction blocks. Based on the values of the received signals, the DCO generates three digital outputs: 25.248 MHz, 32.768 MHz and 24.704 MHz for C6, E1 and T1 dividers, respectively.

In Holdover mode, the DCO is running with the signal generated by using storage techniques.

In Freerun mode, the DCO is running with the master frequency signal generated by OSC.

Lock Indicator

If the center frequency of the DPLL is identical to the line frequency, and the input phase offset is small enough so that no slope limiting is exhibited, the LOCK pin will be set high.

Output Interface

The Output Interface uses the three output signals of the DCO to generate total eight types of clock signals and six types of framing signals.

The 32.768 MHz signal is used by the E1_divider circuit to generate five types of clock signals (C2o, $\overline{C4o}$, C8o, $\overline{C16o}$ and $\overline{C32o}$) with nominal 50% duty cycle and six types of framing signals (F0o, F8o, $\overline{F16o}$, $\overline{F32o}$, RSP and TSP).

The 24.704 MHz signal is used by the T1_divider circuit to generate two types of T1 signals (C1.5o and $\overline{C3o}$) with nominal 50% duty cycle.

The 25.248 MHz signal is used by the C6_divider circuit to generate the C6o signal with nominal 50% duty cycle.

All these output signals are synchronous to F8o.

OSC

The IDT82V3002 can use either a clock or crystal as the master timing source.

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the OSCi pin. For applications not requiring an accurate Freerun Mode, tolerance of the master timing source may be ±100 ppm. For applications requiring an accurate Freerun Mode, such as AT&T TR62411, the tolerance of the master timing source

must be no greater than ±32 ppm.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the IDT82V3002 will always equal 230 ppm. For example, if the master timing source is 100 ppm, then the capture range will be 130 ppm.

Clock Oscillator

When selecting a Clock Oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle.

For applications requiring ±32 ppm clock accuracy, the following clock oscillator module may be used.

FOX F7C-2E3-20.0 MHz

Frequency:	20 MHz
Tolerance:	25 ppm 0°C to 70°C
Rise & Fall Time:	10 ns (0.33 V 2.97 V 15 pF)
Duty Cycle:	40% to 60%

The output clock should be connected directly (not AC coupled) to the OSCi input of the IDT82V3002, and the OSCo output should be left open as shown in Figure 7.

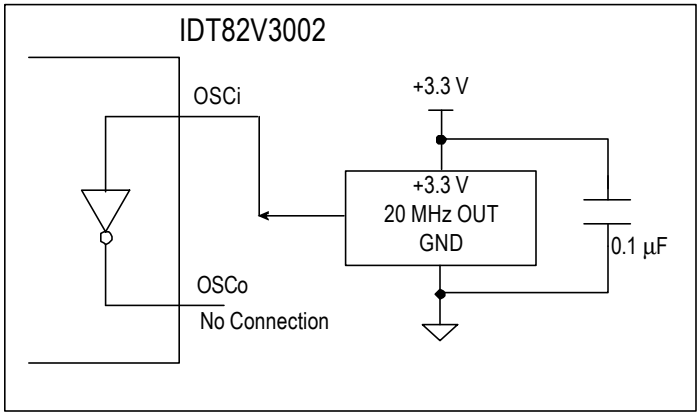


Figure 7. Clock Oscillator Circuit

Crystal Oscillator

Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 8.

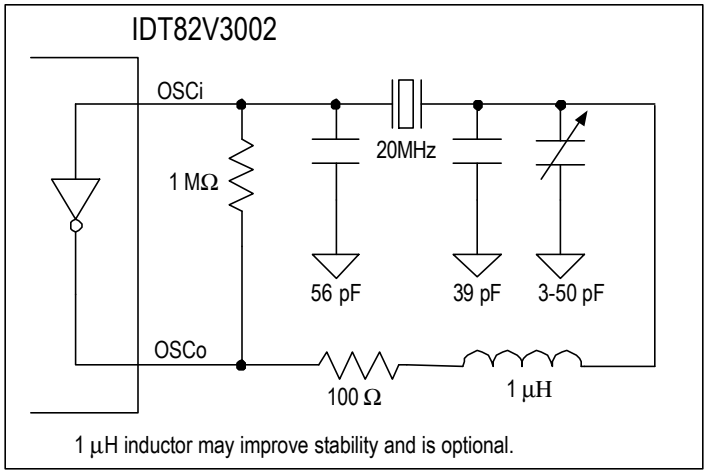


Figure 8. Crystal Oscillator Circuit

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances, and stray capacitance have a major effect on the accuracy of the oscillator frequency.

The trimmer capacitor shown in Figure 8 may be used to compensate for capacitate effects. If accuracy is not a concern, then the trimmer may be removed, the 39 pF capacitor may be increased to 56 pF, and a wider tolerance crystal may be substituted.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows:

Frequency:	20 MHz
Tolerance:	As required
Oscillation Mode:	Fundamental
Resonance Mode:	Parallel
Load Capacitance:	32 pF
Maximum Series Resistance:	35 Ω
Approximate Drive Level:	1 mW

e.g., R1B23B32-20.0 MHz
(20 ppm absolute, ±6 ppm 0°C to 50°C, 32 pF, 25 Ω)

JTAG

The IDT82V3002 support IEEE 1149.1 JTAG Scan.

Reset Circuit

A simple power up reset circuit with about a 50 µs reset low time is shown in Figure 9.

Resistor Rp is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300 ns.

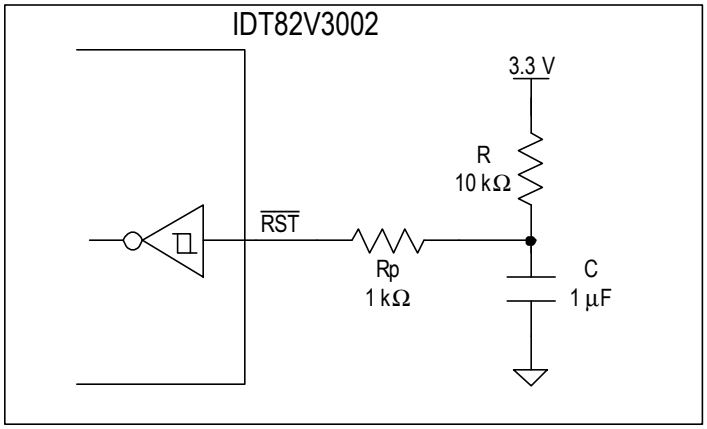


Figure 9. Power-Up Reset Circuit

MEASURES OF PERFORMANCE

The following are some synchronizer performance indicators and their corresponding definitions.

INTRINSIC JITTER

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band limiting filters depending on the applicable standards. In the IDT82V3002, the intrinsic Jitter is limited to less than 0.02 UI on the 2.048 MHz and 1.544 MHz clocks.

JITTER TOLERANCE

Jitter tolerance is a measure of the ability of a DPLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

JITTER TRANSFER

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the IDT82V3002, two internal elements determine the jitter attenuation. This includes the internal 2.1 Hz low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to 5 ns/125 µs. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5 ns/125 µs.

The IDT82V3002 has fourteen outputs with three possible input frequencies for a total of 39 possible jitter transfer functions. Since all outputs are derived from the same signal, the jitter transfer values for the three cases, 8 kHz to 8 kHz, 1.544 MHz to 1.544 MHz and 2.048 MHz to 2.048 MHz can be applied to all outputs.

It should be noted that 1 UI at 1.544 MHz is 644 ns, which is not equal to 1 UI at 2.048 MHz, which is 488 ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds).

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the three jitter transfer functions provided. Note that the resulting jitter transfer functions for all combinations of inputs (8 kHz, 1.544 MHz, 2.048 MHz) and outputs (8 kHz, 1.544 MHz, 3.088 MHz, 6.312 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz, 32.768 MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

FREQUENCY ACCURACY

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the IDT82V3002, the Freerun accuracy is equal to the Master Clock (OSCi) accuracy.

HOLDOVER ACCURACY

Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the IDT82V3002, the storage value is determined while the device is in Normal Mode and locked to an external reference signal.

The absolute Master Clock (OSCi) accuracy of the IDT82V3002 does not affect Holdover accuracy, but the change in OSCi accuracy while in Holdover Mode does.

CAPTURE RANGE

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The IDT82V3002 capture range is equal to ±230 ppm minus the accuracy of the master clock (OSCi). For example, a 32 ppm master clock results in a capture range of 198 ppm.

The Telcordia GR-1244-CORE standard, recommends that the DPLL should be able to reject references that are off the nominal frequency by more than ±12 ppm. The IDT82V3002 provides one pin, MON_out, to indicate whether the primary reference are within the ±12 ppm of the nominal frequency.

LOCK RANGE

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the IDT82V3002.

PHASE SLOPE

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

TIME INTERVAL ERROR (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

MAXIMUM TIME INTERVAL ERROR (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

PHASE CONTINUITY

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

In the case of the IDT82V3002, the output signal phase continuity is maintained to within ±5 ns at the instance (over one frame) of all mode changes. The total phase shift, depending on the type of mode change,

may accumulate up to 200 ns over many frames. The rate of change of the 200 ns phase shift is limited to a maximum phase slope of approximately 5 ns/125 μs. This meets the AT&T TR62411 maximum phase slope requirement of 7.6 ns/125 μs and Telcordia GR-1244-CORE (81 ns/1.326 ms).

PHASE LOCK TIME

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors, which include:

i) Initial input to output phase difference
ii) Initial input to output frequency difference
iii) Synchronizer loop filter
iv) Synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The IDT82V3002 loop filter and limiter were optimized to meet the AT&T TR62411 jitter transfer and phase slope requirements. Consequently, phase lock time, which is not a standards requirement, may be longer than in other applications. See AC Electrical Characteristics - Performance for Maximum Phase Lock Time.

IDT82V3002 provides a fast lock pin (FLOCK), which, when set high enables the DPLL to lock to an incoming reference within approximately 500 ms.

ABSOLUTE MAXIMUM RATINGS*

Rating	Min.	Max.	Unit
Power Supply Voltage	-0.5	5.0	V
Voltage on Any Pin with Respect to Ground	-0.5	V_{DD} + 0.5	V
Package Power Dissipation		200	mW
Storage Temperature	-55	125	°C

NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40		+85	°C
Power Supply Voltage	3.0		3.6	V

DC ELECTRICAL CHARACTERISTICS*

Parameter	Description	Min	Typ.	Max	Units	Test Conditions
I_{DDS}	Supply current with: OSCi = 0 V			300	µA	Outputs unloaded
I_{DD}	Supply current with: OSCi = Clock		35	50	mA	Outputs unloaded
V_{CIH}	CMOS high-level input voltage	0.7V_{DD}			V	OSCi, Fref0 and Fref1
V_{CIL}	CMOS low-level input voltage			0.3V_{DD}	V	OSCi, Fref0 and Fref1
V_{TIH}	TTL high-level input voltage	2.0			V	All input pins except for OSCi, Fref0 and Fref1
V_{TIL}	TTL low-level input voltage			0.8	V	All input pins except for OSCi, Fref0 and Fref1
I_{IL}	Input leakage current: Normal (low level) Normal (high level) Pull up (low level) Pull up (high level) Pull down (low level) Pull down (high level)	 -15 -15 -100 -15 -15 0		 15 15 0 15 15 100	µA	V_I = V_{DD} or 0 V
V_{OH}	High-level output voltage	2.4			V	I_{OH} = 8 mA
V_{OL}	Low-level output voltage			0.4	V	I_{OL} = 8 mA

AC ELECTRICAL CHARACTERISTICS*

Performance

Description	Min	Typ.	Max	Units	Test Conditions / Notes†
Freerun Mode accuracy with OSCi at : 0 ppm	-0		+0	ppm	5-8
Freerun Mode accuracy with OSCi at : ±32 ppm	-32		+32	ppm	5-8
Freerun Mode accuracy with OSCi at : ±100 ppm	-100		+100	ppm	5-8
Holdover Mode accuracy with OSCi at : 0 ppm	-0.025		+0.025	ppm	1, 2, 4, 6-8, 40, 41
Holdover Mode accuracy with OSCi at : ±32 ppm	-0.025		+0.025	ppm	1, 2, 4, 6-8, 40, 41
Holdover Mode accuracy with OSCi at : ±100 ppm	-0.025		+0.025	ppm	1, 2, 4, 6-8, 40, 41
Capture range with OSCi at : 0 ppm	-230		+230	ppm	1-3, 6-8
Capture range with OSCi at : ±32 ppm	-198		+198	ppm	1-3, 6-8
Capture range with OSCi at : ±100 ppm	-130		+130	ppm	1-3, 6-8
Phase lock time		50		s	1-3, 6-14, 42
Output phase continuity with reference switch			200	ns	1-3, 6-14
Output phase continuity with mode switch to Normal			200	ns	1-2, 4-14
Output phase continuity with mode switch to Freerun			200	ns	1-2, 5-14
Output phase continuity with mode switch to Holdover			50	ns	1-3, 6-14
MON_out is low level – Reference frequency accuracy must be:	-12		+12	ppm	
MTIE (maximum time interval error)			600	ns	1-14, 27
Output phase slope			40	µs/s	1-14, 27
Reference input for Auto-Holdover with 8 kHz	-18 k		+18 k	ppm	1-3, 6, 9-11
Reference input for Auto-Holdover with 1.544 MHz	-36 k		+36 k	ppm	1-3, 7, 9-11
Reference input for Auto-Holdover with 2.048 MHz	-36 k		+36 k	ppm	1-3, 8, 9-11

*Note: Voltages are with respect to ground (V_{SS}) unless otherwise stated.

† See “Notes” in page 17.

Intrinsic Jitter Unfiltered

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Intrinsic jitter at F8o (8 kHz)			0.0001	UIpp	1-14, 21-24, 28
Intrinsic jitter at $\overline{F0o}$ (8 kHz)			0.0001	UIpp	1-14, 21-24, 28
Intrinsic jitter at $\overline{F16o}$ (8 kHz)			0.0001	UIpp	1-14, 21-24, 28
Intrinsic jitter at C1.5o (1.544 MHz)			0.015	UIpp	1-14, 21-24, 29
Intrinsic jitter at $\overline{C3o}$ (3.088 MHz)			0.03	UIpp	1-14, 21-24, 31
Intrinsic jitter at C2o (2.048 MHz)			0.01	UIpp	1-14, 21-24, 30
Intrinsic jitter at C6o (6.312 MHz)			0.06	UIpp	1-14, 21-24,
Intrinsic jitter at $\overline{C4o}$ (4.096 MHz)			0.02	UIpp	1-14, 21-24, 32
Intrinsic jitter at C8o (8.192 MHz)			0.04	UIpp	1-14, 21-24, 33
Intrinsic jitter at $\overline{C16o}$ (16.834 MHz)			0.04	UIpp	1-14, 21-24, 34
Intrinsic jitter at TSP (8 kHz)			0.0001	UIpp	1-14, 21-24, 34
Intrinsic jitter at RSP (8 kHz)			0.0001	UIpp	1-14, 21-24, 34
Intrinsic jitter at $\overline{C32o}$ (32.768 MHz)			0.08	UIpp	1-14, 21-24, 35

C1.5o (1.544 MHz) Intrinsic Jitter Filtered

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Intrinsic jitter (4 Hz to 100 kHz filter)			0.008	UIpp	1-14, 21-24, 29
Intrinsic jitter (10 Hz to 40 kHz filter)			0.006	UIpp	1-14, 21-24, 29
Intrinsic jitter (8 kHz to 40 kHz filter)			0.006	UIpp	1-14, 21-24, 29
Intrinsic jitter (10 Hz to 8 kHz filter)			0.003	UIpp	1-14, 21-24, 29

C2o (2.048 MHz) Intrinsic Jitter Filtered

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Intrinsic jitter (4 Hz to 100 kHz filter)			0.005	UIpp	1-14, 21-24, 30
Intrinsic jitter (10 Hz to 40 kHz filter)			0.004	UIpp	1-14, 21-24, 30
Intrinsic jitter (8 kHz to 40 kHz filter)			0.003	UIpp	1-14, 21-24, 30
Intrinsic jitter (10 Hz to 8 kHz filter)			0.002	UIpp	1-14, 21-24, 30

8 kHz Input to 8 kHz Output Jitter Transfer

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Jitter attenuation for 1 Hz@0.01 UIpp input	0		6	dB	1-3, 6, 9-14, 21-22, 24, 28, 35
Jitter attenuation for 1 Hz@0.54 UIpp input	6		16	dB	1-3, 6, 9-14, 21-22, 24, 28, 35
Jitter attenuation for 10 Hz@0.10 UIpp input	15		22	dB	1-3, 6, 9-14, 21-22, 24, 28, 35
Jitter attenuation for 60 Hz@0.10 UIpp input	32		38	dB	1-3, 6, 9-14, 21-22, 24, 28, 35
Jitter attenuation for 300 Hz@0.10 UIpp input	42			dB	1-3, 6, 9-14, 21-22, 24, 28, 35
Jitter attenuation for 3600 Hz@0.005 UIpp input	50			dB	1-3, 6, 9-14, 21-22, 24, 28, 35

1.544 MHz Input to 1.544 MHz Output Jitter Transfer

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Jitter attenuation for 1 Hz@20 UIpp input	0		6	dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 1 Hz@104 UIpp input	6		16	dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 10 Hz@20 UIpp input	17		22	dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 60 Hz@20 UIpp input	33		38	dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 300 Hz@20 UIpp input	45			dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 10 kHz@0.3 UIpp input	48			dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 40 kHz@0.3 UIpp input	50			dB	1-3, 7, 9-14, 21-22, 24, 29, 35

† See “Notes” in page 17.

2.048 MHz Input to 2.048 MHz Output Jitter Transfer

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Jitter at output for 1 Hz@3.00 UIpp input			2.5	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 35
Jitter at output for 1 Hz@3.00 UIpp input with 40 Hz to 100 Hz filter			0.07	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 36
Jitter at output for 3 Hz@2.33 UIpp input			1.4	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 35
Jitter at output for 3 Hz@2.33 UIpp input with 40 Hz to 100 Hz filter			0.10	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 36
Jitter at output for 5 Hz@2.07 UIpp input			0.90	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 35
Jitter at output for 5 Hz@2.07 UIpp input with 40 Hz to 100 Hz filter			0.10	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 36
Jitter at output for 10 Hz@1.76 UIpp input			0.40	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 35
Jitter at output for 10 Hz@1.76 UIpp input with 40 Hz to 100 Hz filter			0.10	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 36
Jitter at output for 100 Hz@1.50 UIpp input			0.06	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 35
Jitter at output for 100 Hz@1.50 UIpp input with 40 Hz to 100 Hz filter			0.05	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 36
Jitter at output for 2400 Hz@1.50 UIpp input			0.04	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 35
Jitter at output for 2400 Hz@1.50 UIpp input with 40 Hz to 100 Hz filter			0.03	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 36
Jitter at output for 100 kHz@0.20 UIpp input			0.04	UIpp	1-3, 8, 9-14, 21-22, 24, 30, 35
Jitter at output for 100 kHz@0.20 UIpp input with 40 Hz to 100 Hz filter			0.02	UIpp	1-3, 8, 9-14, 21-22, 24, 30

8 kHz Input Jitter Tolerance

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Jitter tolerance for 1 Hz input	0.80			UIpp	1-3, 6, 9-14, 21-22, 24-26, 28
Jitter tolerance for 5 Hz input	0.70			UIpp	1-3, 6, 9-14, 21-22, 24-26, 28
Jitter tolerance for 20 Hz input	0.60			UIpp	1-3, 6, 9-14, 21-22, 24-26, 28
Jitter tolerance for 300 Hz input	0.16			UIpp	1-3, 6, 9-14, 21-22, 24-26, 28
Jitter tolerance for 400 Hz input	0.14			UIpp	1-3, 6, 9-14, 21-22, 24-26, 28
Jitter tolerance for 700 Hz input	0.07			UIpp	1-3, 6, 9-14, 21-22, 24-26, 28
Jitter tolerance for 2400 Hz input	0.02			UIpp	1-3, 6, 9-14, 21-22, 24-26, 28
Jitter tolerance for 3600 Hz input	0.01			UIpp	1-3, 6, 9-14, 21-22, 24-26, 28

1.544 MHz Input Jitter Tolerance

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Jitter tolerance for 1 Hz input	150			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29
Jitter tolerance for 5 Hz input	140			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29
Jitter tolerance for 20 Hz input	130			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29
Jitter tolerance for 300 Hz input	38			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29
Jitter tolerance for 400 Hz input	25			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29
Jitter tolerance for 700 Hz input	15			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29
Jitter tolerance for 2400 Hz input	5			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29
Jitter tolerance for 10 kHz input	1.2			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29
Jitter tolerance for 40 kHz input	0.5			UIpp	1-3, 7, 9-14, 21-22, 24-26, 29

2.048 MHz Input Jitter Tolerance

Description	Min	Typ	Max	Units	Test Conditions / Notes†
Jitter tolerance for 1 Hz input	150			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30
Jitter tolerance for 5 Hz input	140			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30
Jitter tolerance for 20 Hz input	130			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30
Jitter tolerance for 300 Hz input	40			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30
Jitter tolerance for 400 Hz input	33			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30
Jitter tolerance for 700 Hz input	18			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30
Jitter tolerance for 2400 Hz input	5.5			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30
Jitter tolerance for 10 kHz input	1.3			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30
Jitter tolerance for 100 kHz input	0.4			UIpp	1-3, 8, 9-14, 21-22, 24-26, 30

† See “Notes” in page 17.

† Notes:

Voltages are with respect to ground (V_{SS}) unless otherwise stated.
Supply voltage and operating temperature are as per Recommended Operating Conditions.
Timing parameters are as per AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

1. Fref0 reference input selected.
2. Fref1 reference input selected.
3. Normal Mode selected.
4. Holdover Mode selected.
5. Freerun Mode selected.
6. 8 kHz Frequency Mode selected.
7. 1.544 MHz Frequency Mode selected.
8. 2.048 MHz Frequency Mode selected.
9. Master clock input OSCi at 20 MHz ±0 ppm.
10. Master clock input OSCi at 20 MHz ±32 ppm.
11. Master clock input OSCi at 20 MHz ±100 ppm.
12. Selected reference input at ±0 ppm.
13. Selected reference input at ±32 ppm.
14. Selected reference input at ±100 ppm.
15. For Freerun Mode of ±0 ppm.
16. For Freerun Mode of ±32 ppm.
17. For Freerun Mode of ±100 ppm.
18. For capture range of ±230 ppm.
19. For capture range of ±198 ppm.
20. For capture range of ±130 ppm.
21. 25 pF capacitive load.
22. OSCi Master Clock jitter is less than 2 nspp, or 0.04 UIpp where 1 UIpp = 1/20 MHz.
23. Jitter on reference input is obtained at slightly higher input jitter amplitudes.
24. Applied jitter is sinusoidal.
25. Minimum applied input jitter magnitude to regain synchronization.
26. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
27. Within 10 ms of the state, reference or input change.
28. 1 UIpp = 125 µs for 8 kHz signals.
29. 1 UIpp = 648 ns for 1.544 MHz signals.
30. 1 UIpp = 488 ns for 2.048 MHz signals.
31. 1 UIpp = 323 ns for 3.088 MHz signals.
32. 1 UIpp = 244 ns for 4.096 MHz signals.
33. 1 UIpp = 122 ns for 8.192 MHz signals.
34. 1 UIpp = 61 ns for 16.484 MHz signals.
35. 1 UIpp = 30 ns for 32.968 MHz signals.
36. No filter.
37. 40 Hz to 100 kHz bandpass filter.
38. With respect to reference input signal frequency.
39. After a $\overline{RST}$ or $\overline{TCLR}$.
40. Master clock duty 40% to 60%.
41. Prior to Holdover Mode, device as in Normal Mode and phase locked.
42. With input frequency offset of 100 ppm.

TIMING CHARACTERISTICS

Timing Parameter Measurement Voltage Levels*

Parameter	Description	CMOS	Units
V_T	Threshold Voltage	$0.5V_{DD}$	V
V_{HM}	Rise and Fall Threshold Voltage High	$0.7V_{DD}$	V
V_{LM}	Rise and Fall Threshold Voltage Low	$0.3V_{DD}$	V

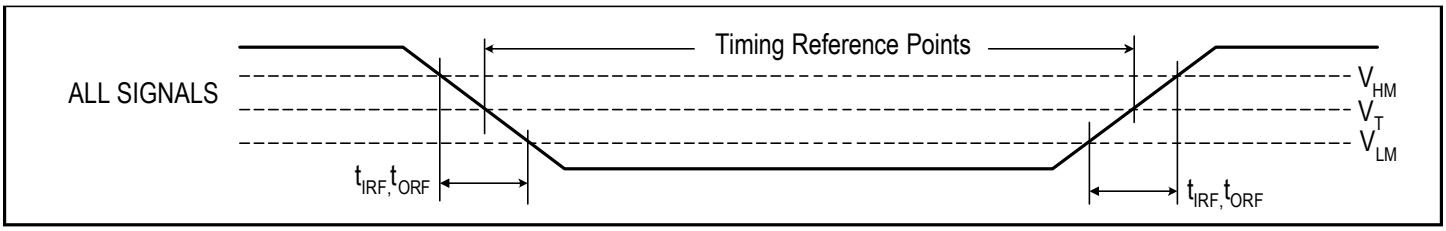


Figure 10. Timing Parameter Measurement Voltage Levels

*Note: 1. Voltages are with respect to ground (V_{SS}) unless otherwise stated.
2. Supply voltage and operating temperature are as per Recommended Operating Conditions.
3. Timing for input and output signals is based on the worst case result of the CMOS thresholds.

Input / Output Timing

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{RW}	Reference input pulse width high or low	100			ns	
t_{IRF}	Reference input rise or fall time			10	ns	
t_{R8D}	8 kHz reference input to F8o delay	0		25	ns	
t_{R15D}	1.544 MHz reference input to F8o delay	326		342	ns	
t_{R2D}	2.048 MHz reference input to F8o delay	248		264	ns	
t_{FOD}	F8o to $\overline{F0o}$ delay	111		130	ns	
t_{F16S}	$\overline{F16o}$ setup to $\overline{C16o}$ falling	25		40	ns	
t_{F16H}	$\overline{F16o}$ hold to $\overline{C16o}$ falling	25		40	ns	
t_{C15D}	F8o to C1.5o delay	-10		10	ns	
t_{C3D}	F8o to $\overline{C3o}$ delay	-10		10	ns	
t_{C6D}	F8o to C6o delay	-10		10	ns	
t_{C2D}	F8o to C2o	-11		5	ns	
t_{C4D}	F8o to $\overline{C4o}$	-11		5	ns	
t_{C8D}	F8o to C8o delay	-11		5	ns	
t_{C16D}	F8o to $\overline{C16o}$ delay	-11		5	ns	
t_{C32D}	F8o to $\overline{C32o}$ delay	-11		5	ns	
t_{TSPD}	F8o to TSP delay	-6		10	ns	
t_{RSPD}	F8o to RSP delay	-8		8	ns	
t_{C15W}	C1.5o pulse width high or low	309		339	ns	
t_{C3W}	$\overline{C3o}$ pulse width high or low	154		169	ns	
t_{C6W}	C6o pulse width high or low	70		86	ns	
t_{C2W}	C2o pulse width high or low	232		258	ns	
t_{C4W}	$\overline{C4o}$ pulse width high or low	111		133	ns	
t_{C8W}	C8o pulse width high or low	52		70	ns	
t_{C16WL}	$\overline{C16o}$ pulse width high or low	24		35	ns	
t_{C32W}	$\overline{C32o}$ pulse width high or low	14		16.78	ns	
t_{TSPW}	TSP pulse width high	478		494	ns	
t_{RSPW}	RSP pulse width high	474		491	ns	
t_{F0WL}	$\overline{F0o}$ pulse width low	234		254	ns	
t_{F8WH}	F8o pulse width high	109		135	ns	
t_{F16WL}	$\overline{F16o}$ pulse width low	47		72	ns	
t_{0RF}	Output clock and frame pulse rise or fall time			9	ns	
t_S	Input Controls Setup Time	100			ns	
t_H	Input Controls Hold Time	100			ns	
t_{F16D}	F8o to $\overline{F16o}$ delay	24		38	ns	
t_{F32D}	F8o to $\overline{F32o}$ delay	12		19	ns	
t_{F32S}	$\overline{F32o}$ setup to $\overline{C32o}$ falling	11			ns	
t_{F32H}	$\overline{F32o}$ hold to $\overline{C32o}$ falling	11			ns	
t_{F32WL}	$\overline{F32o}$ pulse width low	15		31	ns	

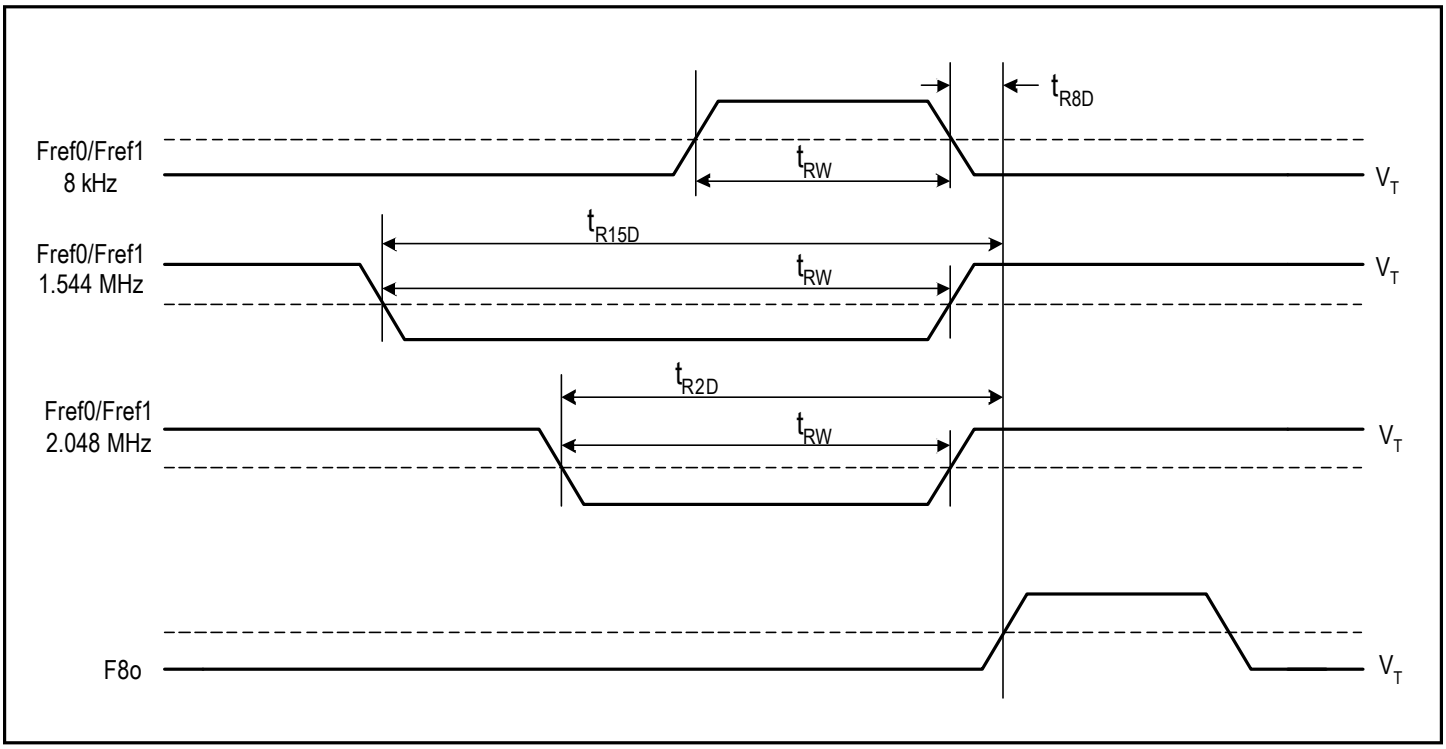


Figure 11. Input to Output Timing (Normal Mode)

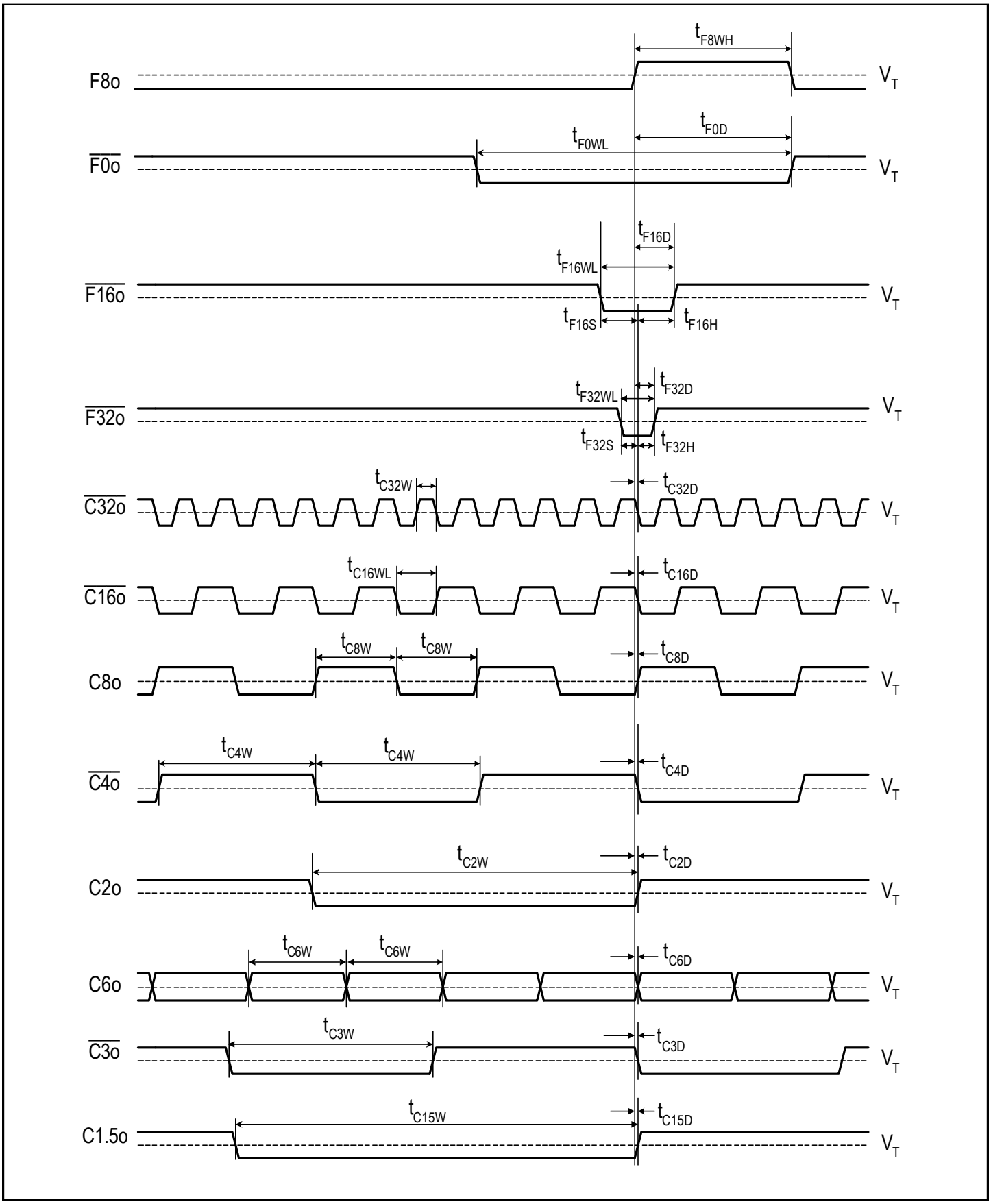


Figure 12. Output Timing 1

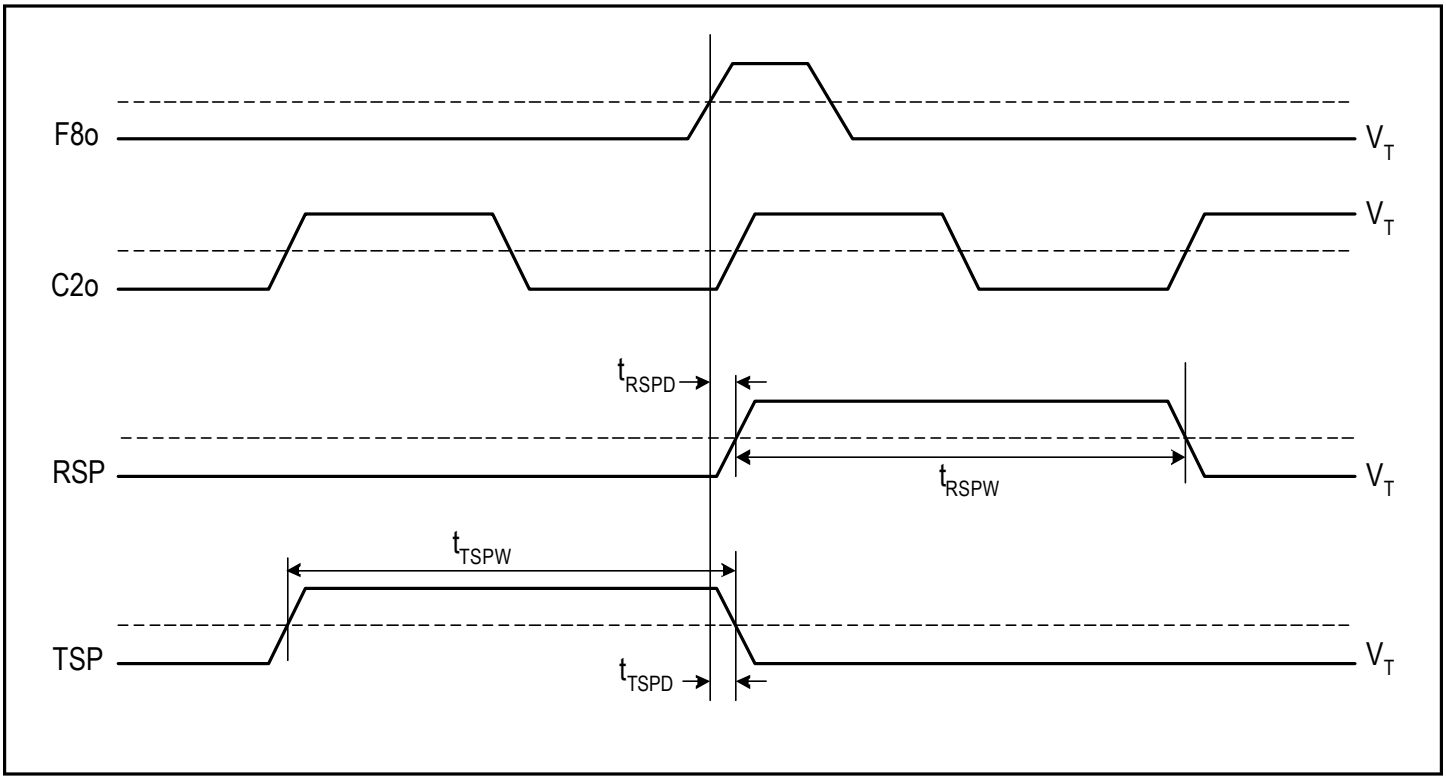


Figure 13. Output Timing 2

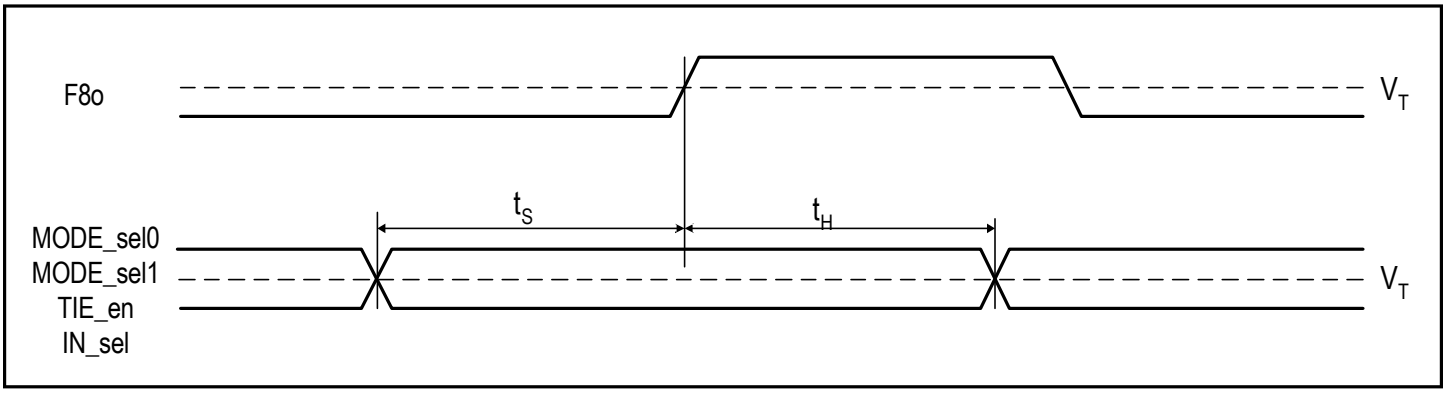
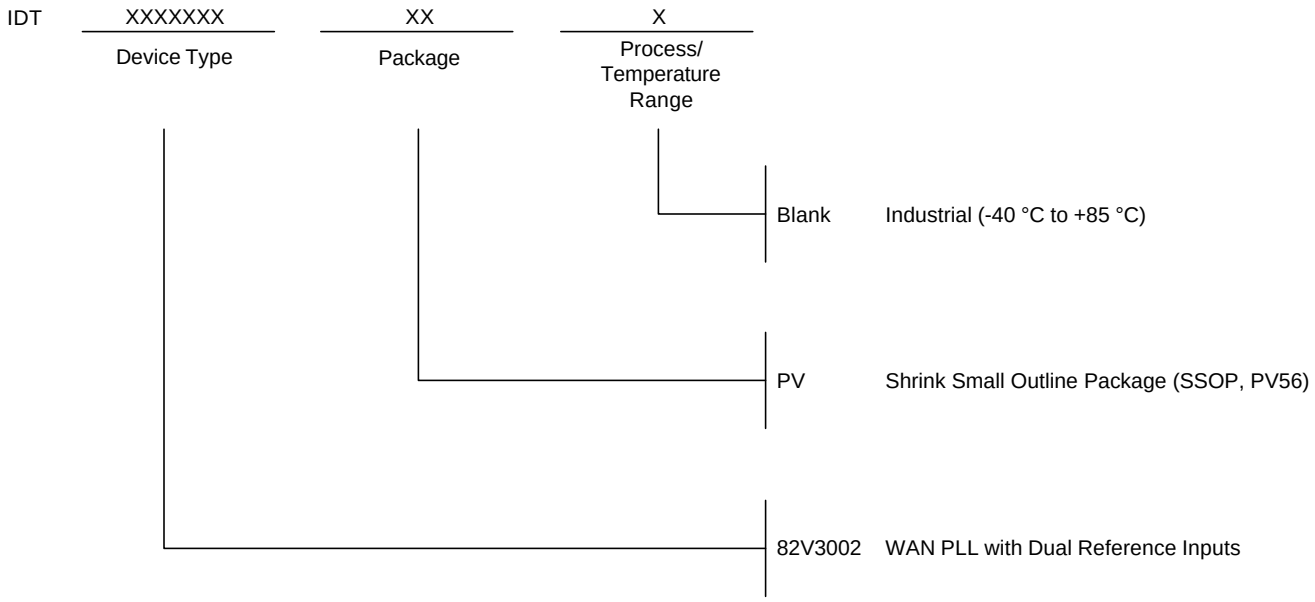


Figure 14. Input Control Setup and Hold Timing

ORDERING INFORMATION



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