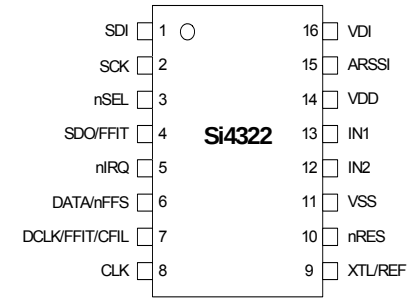
Si4322

Si4322 Universal ISM Band FSK Receiver

Features

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
- Direct differential antenna input
- Programmable baseband bandwidth (135 to 400 kHz)
- Analog and digital RSSI
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery
- RX pattern recognition
- SPI compatible serial control interface
- Clock and reset signals for microcontroller
- 64-bit RX data FIFO
- Autonomous low duty-cycle mode down to 0.006%
- Standard 10 MHz crystal reference
- Wake-up timer
- Low battery detector
- 2.2 to 3.8 V supply voltage
- Low power consumption
- Low standby current (typical 0.3 µA)

Pin Assignments



Patents pending

This data sheet refers to version A1

Applications

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

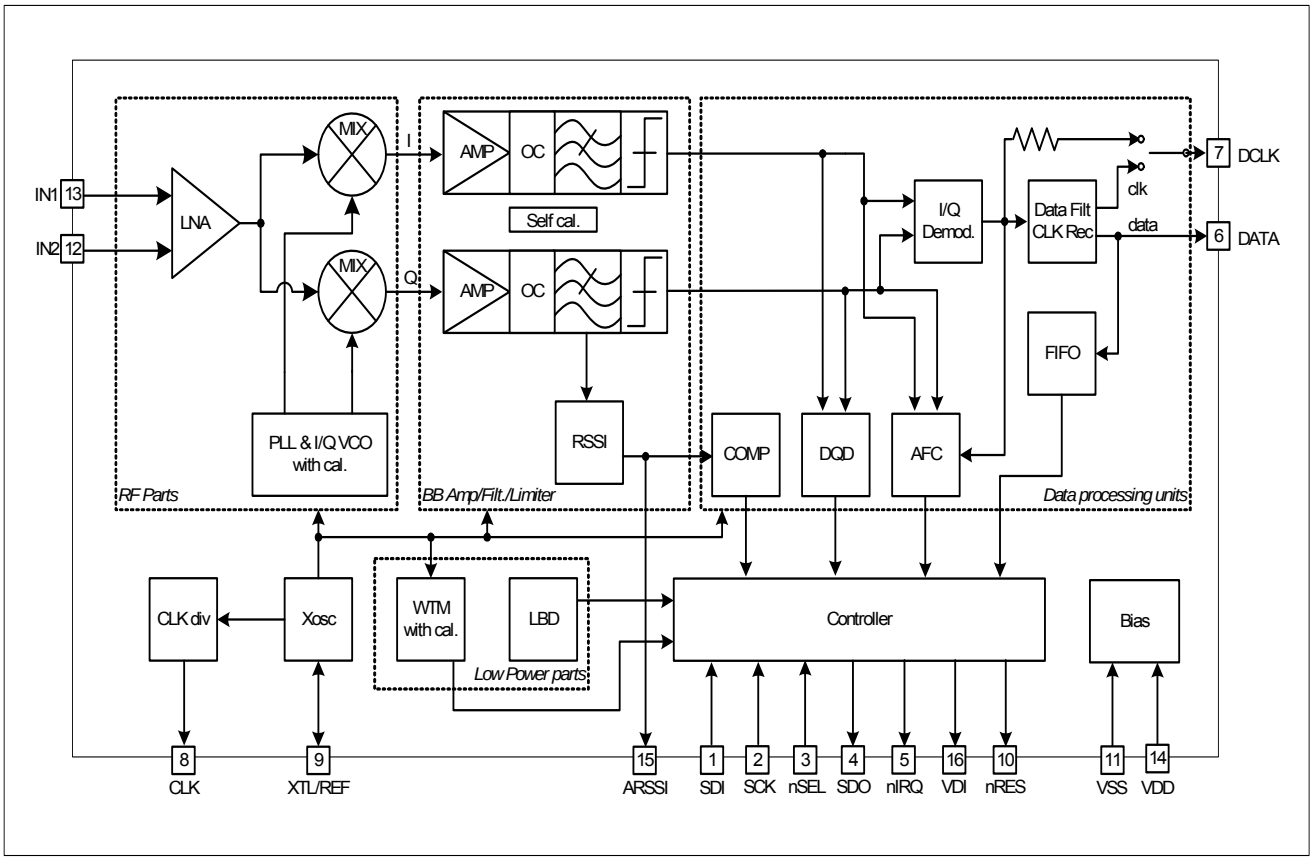
Description

Silicon Labs' Si4322 is a single chip, low power, multi-channel FSK receiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 433, 868, and 915 MHz bands. Used in conjunction with Silicon Labs' FSK transmitters, the Si4322 is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering capacitors are needed for operation.

The Si4322 is a complete analog RF and baseband receiver including a multi-band PLL synthesizer with an LNA, I/Q down converter mixers, baseband filters and amplifiers, and I/Q demodulator. The receiver employs zero-IF approach with I/Q demodulation, therefore no external components (except crystal and decoupling) are needed in a typical application. The Si4322 has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading, and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The baseband bandwidth (BW) is programmable to accommodate various deviation, data rate, and crystal tolerance requirements.

The chip dramatically reduces the load on the microcontroller with integrated digital data processing: data filtering, clock recovery, data pattern recognition and integrated FIFO. The automatic frequency control (AFC) feature allows using a low accuracy (low cost) crystal. To minimize the system cost, the chip can provide a clock signal for the microcontroller, avoiding the need for two crystals.

Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Characteristics
(Test conditions: T_{OP} = 25 °C; V_{DD} = 2.7 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	I_{dd}		—	12	14	mA
Standby Current	I_{pd}	all blocks disabled	—	0.3	—	µA
Low Battery Voltage Detector and Wake-Up Timer Current[1]	I_{lb}		—	—	5	µA
Idle Current	I_x	crystal oscillator is on[1]	—	0.5	—	mA
Low Battery Detection Threshold	V_{lb}	programmable in 0.1 V steps	2.0		3.5	V
Low Battery Detection Accuracy	V_{lba}		—	±2.5	—	%
V_{dd} Threshold Required to Generate a POR	V_{POR}		—	1.5	—	V
POR Hysteresis	$V_{PORhyst}$	larger glitches on the V_{dd} generate a POR even above the threshold V_{POR}[2]	—	—	0.6	V
V_{DD} Slew Rate	SR_{Vdd}	for proper POR generation	0.1	—	—	V/ms
Digital Input Low Level	V_{il}		—	—	0.3 x V_{DD}	V
Digital Input High Level	V_{ih}		0.7 x V_{DD}	—	—	V
Digital Input Current	I_{il}	V_{IL} = 0 V	–1	—	1	µA
Digital Input Current	I_{ih}	V_{IH} = V_{DD}, V_{DD} = 3.8 V	–1	—	1	µA
Digital Output Low Level	V_{ol}	I_{OL} = 2 mA		—	0.4	V
Digital Output High Level	V_{oh}	I_{oh} = –2 mA	V_{DD} – 0.4	—	—	V

Notes:
1. Measured with disabled clock output buffer.
2. For detailed information see "13. Reset modes" on page 34.

Table 2. AC Characteristics

(Test conditions: T_{OP} = 25 °C; V_{DD} = 2.7 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Receiver Frequency	f_{LO}	433 MHz band, 10 kHz resolution 868 MHz band, 20 kHz resolution 915 MHz band, 20 kHz resolution	400.96 801.92 881.92	— — —	439.03 878.06 958.06	MHz
Receiver Bandwidth	BW	Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	120 180 240 300 360	135 200 270 350 400	150 225 300 375 450	kHz
FSK Bit Rate	BR	With internal digital filters	—	—	115.2	kbps
FSK Bit Rate	BRA	With analog filter		—	256	kbps
Receiver Sensitivity	P_{min}	BER 10^{-3}, BW = 135 kHz, BR = 1.2 kbps, δf_{FSK} = 60 kHz	—	–109	—	dBm
AFC Locking Range	AFC_{range}	δf_{FSK}: FSK deviation in the received signal	—	0.8 x δf_{FSK}	—	
Input IP3	$IIP3_{inh}$	In band interferers	—	–21	—	dBm
Input IP3	$IIP3_{outh}$	Out of band interferers: f – f_{LO} > 4 MHz	—	–18	—	dBm
Co-Channel Rejection	CCR	BER = 10^{-2} with continuous wave interferer in the channel	—	–4	—	dB
Blocking Ratio with CW Interferer	BR_{2MHz}	BER = 10^{-2}, BW = 135 kHz, BR = 9.6 kbps, δf_{FSK} = 60 kHz, interferer offset 2 MHz	—	54	—	dB
	BR_{10MHz}	Same as above, interferer offset 10 MHz	—	59	—	dB
Maximum Input Power	P_{max}	LNA: maximum gain	0	—	—	dBm
RF Input Impedance Real Part (differential)[1]	R_{in}	LNA gain (0, –12 dB) LNA gain (–6, –18 dB)	— —	250 500	— —	Ω
RF Input Capacitance (differential)[1]	C_{in}		—	1	—	pF
RSSI Accuracy	RS_a		—	±5	—	dB
RSSI Range	RS_r		—	46	—	dB

Notes:

1. See matching circuit parameters and antenna design guide for information, and Application Notes available from http://www.silabs.com.
2. Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.
3. During the Power-On Reset period, commands are not accepted by the chip. In case of software reset, (see "13. Reset modes" on page 34) the reset timeout is 0.25 ms typical.
4. The crystal oscillator start up time strongly depends on the capacitance seen by the oscillator. Low capacitance and low ESR crystal is recommended with low parasitic PCB layout design.
5. Auto-calibration can be turned off.

Table 2. AC Characteristics (Continued)
(Test conditions: T_{OP} = 25 °C; V_{DD} = 2.7 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Filter Capacitance for ARSSI	C_{ARSSI}		1	—	—	nF
DRSSI Programmable Level Steps	RS_{step}		—	6	—	dB
DRSSI Response Time	RS_{resp}	Until the DRSSI goes high after the input signal exceeds the pre-programmed limit, C_{ARRSI} = 5 nF	—	500	—	µs
PLL Reference Frequency	f_{ref}	Note 2	9	10	11	MHz
PLL Lock Time	t_{lock}	Frequency error < 1 kHz after 1 MHz step	—	30	—	µs
PLL Startup Time	t_{st1P}	Initial calibration after power-up with running crystal oscillator	—	—	500	µs
PLL Startup Time	t_{st2P}	Recalibration after receiver chain enable with running crystal oscillator	—	—	60	µs
Crystal Load Capacitance, see Crystal Selection Guide	C_{xl}	Programmable in 0.5 pF steps, tolerance ±10%	8.5	—	16	pF
Internal POR Pulse Width[3]	t_{POR}	After V_{DD} has reached 90% of final value	—	50	100	ms
Crystal Oscillator Startup Time	t_{sx}	Crystal ESR < 50 Ω, C_L = 16pF[4]	—	—	5	ms
Wake-Up Timer Clock Period	t_{PBt}	Calibrated every 30 seconds[5]	0.995	1	1.005	ms
Programmable Wake-Up Time	$t_{wake-up}$		1	—	8.4×10^6	ms
Digital Input Capacitance	C_{inD}		—	—	2	pF
Digital Output Rise/Fall Time	t_r, t_f	15 pF pure capacitive load	—	—	10	ns
Clock Output Rise/Fall Time	t_{rckout}, t_{fckout}	10 pF pure capacitive load	—	—	15	ns
Slow Clock Frequency	$f_{ckoutslow}$	Tolerance ± 1 kHz	—	32	—	kHz

Notes:
1. See matching circuit parameters and antenna design guide for information, and Application Notes available from http://www.silabs.com.
2. Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.
3. During the Power-On Reset period, commands are not accepted by the chip. In case of software reset, (see "13. Reset modes" on page 34) the reset timeout is 0.25 ms typical.
4. The crystal oscillator start up time strongly depends on the capacitance seen by the oscillator. Low capacitance and low ESR crystal is recommended with low parasitic PCB layout design.
5. Auto-calibration can be turned off.

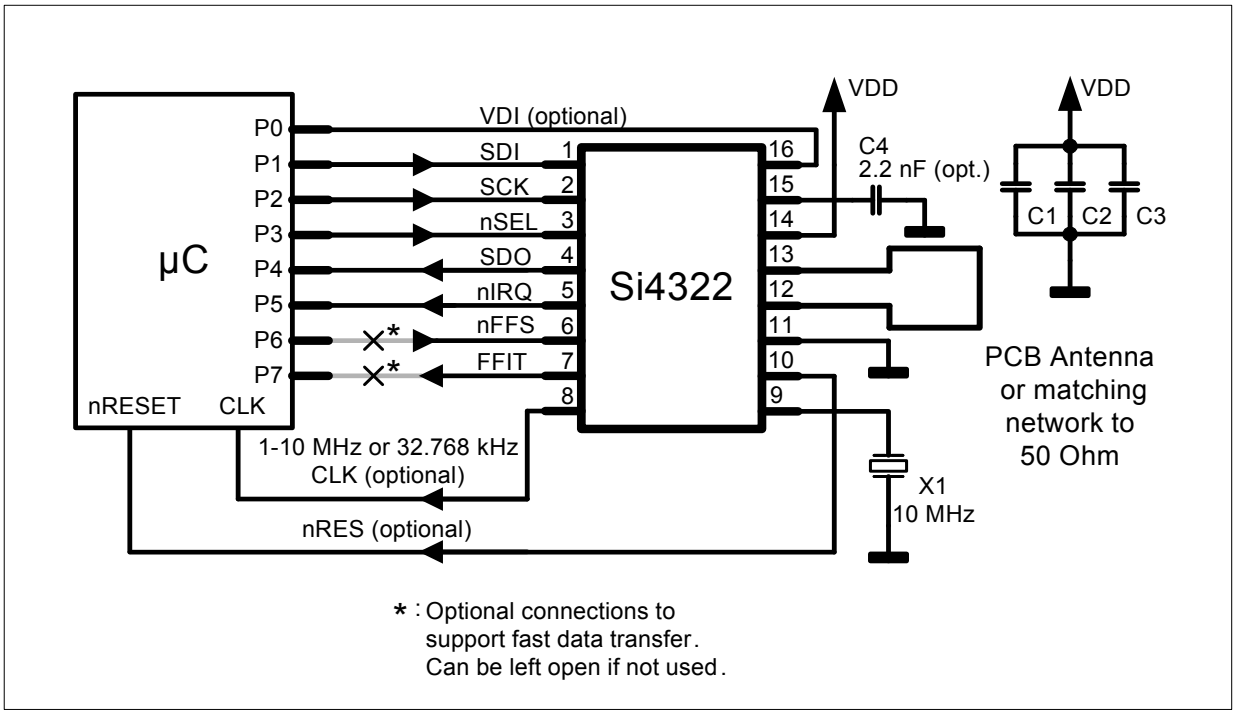
Table 3. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Supply Voltage	V_{DD}	2.2	—	3.8	V
Ambient Operating Temperature	T_{OP}	–40	—	+85	°C

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Positive Supply Voltage	V_{DD}	–0.5	6.0	V
Voltage on Any Pin	V_{IN}	–0.5	V_{dd}+0.5	V
Input Current into Any Pin Except VDD and VSS	I_{IN}	–25	25	mA
Electrostatic Discharge with Human Body Model	ESD	—	1000	V
Storage Temperature	T_{ST}	–55	125	°C
Lead Temperature (soldering, max 10 s)	T_{LD}	—	260	°C

2. Typical Application Schematic



2.1. Recommended Supply Decoupling Capacitor Values

C2 and C3 should be 0603 size ceramic capacitors to achieve the best supply decoupling.

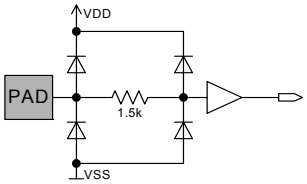
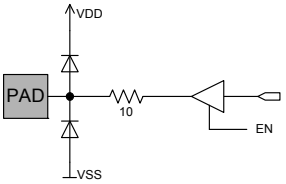
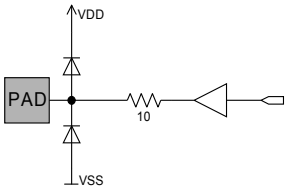
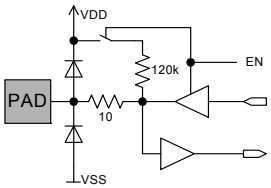
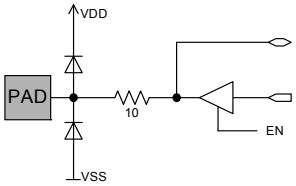
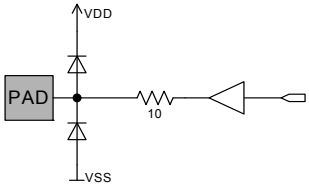
Band [MHz]	C1	C2	C3
433	2.2 µF	10 nF	220 pF
868	2.2 µF	10 nF	47 pF
915	2.2 µF	10 nF	33 pF

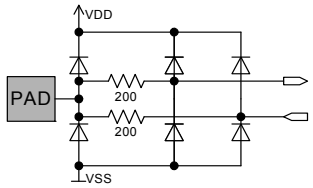
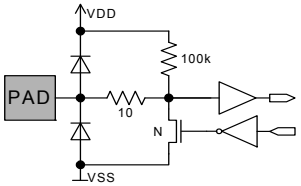
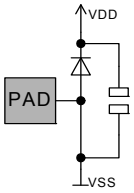
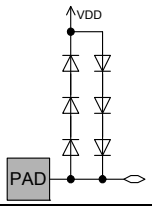
Property	C1	C2	C3
SMD size	A	0603	0603
Dielectric	Tantalum	Ceramic	Ceramic

Table 5. Pin Function vs. Operation Mode

Bit setting fe	Function	Pin 6	Pin 7
0	Receiver FIFO disabled	RX data output	RX data clock output
1	Receiver FIFO enabled	nFFS input (RX data FIFO can be accessed)	FFIT output
Note: The fe bit can be found in the "5.14. FIFO Settings Command" on page 25.			

3. Internal Pin Connections

Pin	Name	Internal Connection
1	SDI	
2	SCK	
3	nSEL	
4	SDO	
	FFIT	
5	nIRQ	
6	DATA	
	nFFS	
7	DCLK	
	FFIT	
	CFIL	
8	CLK	

Pin	Name	Internal Connection
9	XTL	
	REF	
10	nRES	
11	VSS	
12	IN2	
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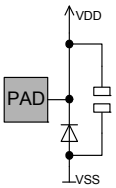
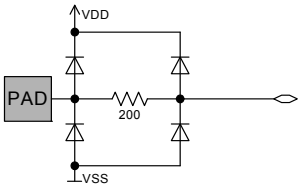
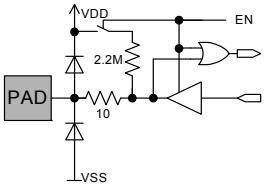
14	VDD	
15	ARSSI	
16	VDI	

4. Functional Description

The Si4322 FSK receiver is the counterpart of Silicon Labs' Si4022 FSK transmitter. It covers the unlicensed frequency bands at 433, 868 and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The receiver employs zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The Si4322 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

4.1. PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows for the use of multiple channels in any of the bands.

4.2. LNA

The LNA has 250 Ω input impedance, which suits to the recommended antennas. (See Application Notes available from www.silabs.com.)

If the RF input of the chip is connected to 50 Ω devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain can be selected (0, –6, –12, –18 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

4.3. Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements.

The filter structure is a 7th order Butterworth low-pass with 40 dB suppression at 2 x BW frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 15 kHz.

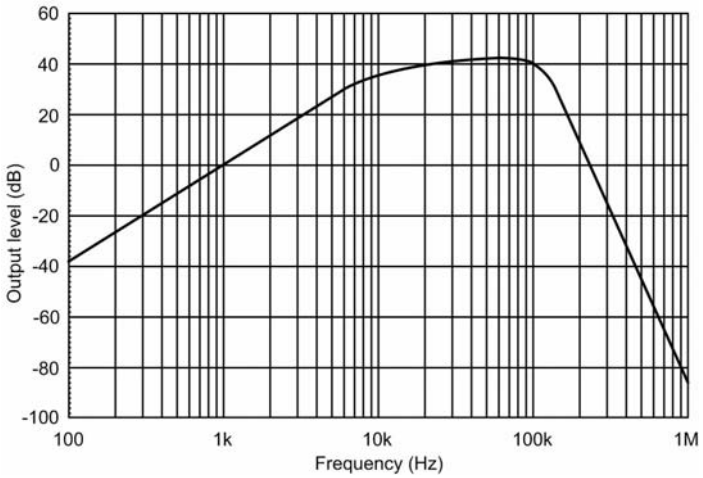


Figure 1. Full Baseband Amplifier Transfer Function, BW = 135 kHz

4.4. Data Filtering and Clock Recovery

The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation: The filter is an RC type low-pass filter followed by a Schmitt-trigger (St). The resistor (10k) and the Schmitt-trigger (St) are integrated on the chip. The filter capacitor should be connected externally, its value should be chosen according to the actual bit rate. In this mode, the receiver can handle up to 256 kbps data rate. When the analog filter is selected, the FIFO cannot be used and clock is not provided for the demodulated data.

Digital operation: The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode, there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock, the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, and then automatically switches to slow mode after locking.

Only the data filter and the clock recovery use the bit rate clock. Therefore, in analog mode, there is no need for setting the correct bit rate.

4.5. Data Validity Blocks

4.5.1. RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.

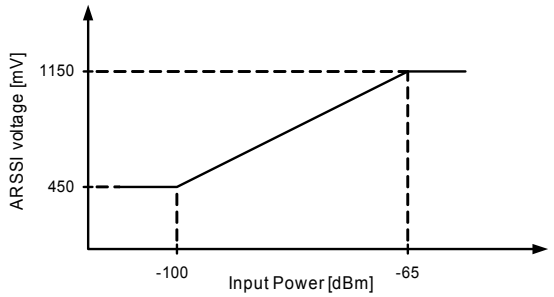


Figure 2. Typical Analog ARSSI Voltage vs. RF Input Power

4.5.2. DQD

The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive 0→1 and 1→0 transitions during a single bit period. The programmable DQD parameter defines a threshold for this counter. If the counter result exceeds this parameter, then DQD output indicates good FSK signal quality. Using this method, it is possible to "forecast" the probability of BER degradation. In cases when the deviation is close to the bit rate, there should be four transitions during a single one-bit period in the I/Q signals. As the bit rate decreases in comparison to the deviation, more and more transitions will happen during a bit period.

4.5.3. AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of the following:

- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e., increased sensitivity)
- higher data rate

4.6. Crystal Oscillator and Microcontroller Clock Output

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this data sheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. In normal operation, it is divided from the reference 10 MHz. During sleep mode, a low frequency (typical 32 kHz) output clock signal can be switched on, which is provided by a low-power RC oscillator.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the "5.3. Configuration Setting Command" on page 16, the chip provides a programmable number (default is 512) of further clock pulses (“clock tail”) for the microcontroller to let it go to idle or sleep mode.

4.7. Low Battery Voltage Detector

The low battery detector circuit periodically monitors (typ. 8 ms) the supply voltage and generates an interrupt if it falls below a programmable threshold level.

4.8. Wake-Up Timer

The wake-up timer has very low current consumption (5 µA max) and can be programmed from 1 ms to several hours.

It calibrates itself to the crystal oscillator at every startup and then at every 30 seconds with an accuracy of ±0.5%. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing. The periodic auto-calibration feature can be turned off.

4.9. Event Handling

In order to minimize current consumption, the receiver supports sleep mode. Active mode can be initiated by setting the *ex* or *en* bits (in "5.3. Configuration Setting Command" on page 16 or "5.5. Receiver Setting Command" on page 18).

The Si4322 generates an interrupt signal on several events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up). This signal can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

4.10. Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 64-bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the *fe* bit to 1 in the "5.14. FIFO Settings Command" on page 25. During FIFO read the crystal oscillator must be ON.

5. Control Interface

Commands to the receiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g., bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. Special care must be taken when the microcontroller's built-in hardware serial port is used. If the port cannot be switched to 16-bit mode then a separate I/O line should be used to control the nSEL pin to ensure the low level during the whole duration of the command or a software serial control interface should be implemented. The Power On Reset (POR) circuit sets default values in all control registers.

The receiver will generate an interrupt request (IRQ) for the microcontroller on the following events:

- Supply voltage below the preprogrammed value is detected (LBD)
- Wake-up timer timeout (WK-UP)
- FIFO received the preprogrammed amount of bits (FFIT)
- FIFO overflow (FFOV)

FFIT and FFOV are applicable only when the FIFO is enabled. To find out why the nIRQ was issued, the status bits should be read out.

5.1. Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

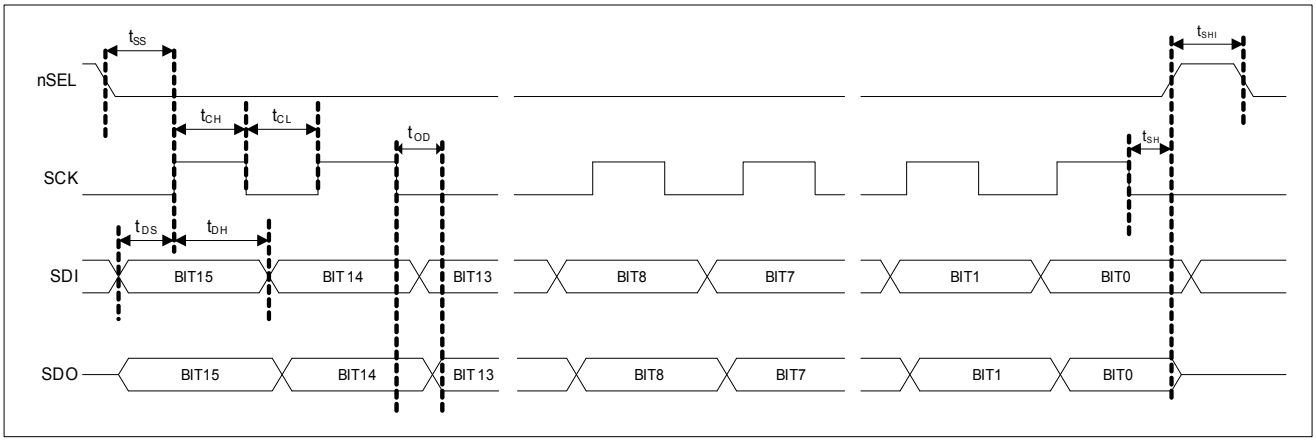


Figure 3. Timing Diagram

5.2. Control Commands

	Control Word	Related Parameters/Functions	Related Control Bits
1	Configuration Setting Command	Receiving band, low battery detector, wake-up timer, crystal oscillator, load capacitance, baseband filter bandwidth, clock output buffer	*b1* to *b0*, *eb*, *et*, *ex*, *x3* to *x0*, *i2* to *i0*, *dc*
2	Frequency Setting Command	Frequency of the local oscillator	*f11* to *f0*
3	Receiver Setting Command	VDI source, LNA gain, RSSI threshold, enable receiver	*d1* to *d0*, *g1* to *g0*, *r2* to *r0*, *en*
4	Synchron Pattern Command	Synchron pattern	*b7* to *b0*
5	Wake-up Timer Command	Wake-up time period	*r3* to *r0*, *m7* to *m0*
6	Extended Wake-up Timer Command	Wake-up time period extended adjustment	*c1* to *c0*, *m13* to *m8*
7	Low Duty-Cycle Command	Enable and set low duty-cycle mode	*d6* to *d0*, *enldc*
8	Low Battery Detector and Clock Divider Command	Microcontroller clock division ratio, low frequency oscillator enable, LBD threshold voltage	*cd2* to *cd0*, *elfc*, *t3* to *t0*
9	AFC Control Command	AFC parameters	*a1* to *a0*, *rl1* to *rl0*, *st*, *fi*, *oe*, *aen*
10	Data Filter Command	Clock recovery parameters, auto-sleep mode, data filter type, auto wake-up, DQD threshold	*al*, *ml*, *dsfi*, *sf*, *ewi*, *f2* to *f0*
11	Data Rate Command	Bit rate	*cs*, *r6* to *r0*
12	FIFO Settings Command	FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable	*f3* to *f0*, *s1* to *s0*, *ff*, *fe*
13	Extended Features Command	Clock tail, wake-up auto calibration, PLL bandwidth, long FIFO IT level	*ctls*, *dcal*, *bw1* to *bw0*, *f5* to *f4*
14	Status Read Command	Receiver status read	

Note: In the following tables the POR column shows the default values of the command registers after power-on.

Table 6. Control Register Default Values

	Control Register	Power-On Reset Value
1	Configuration Setting Command	928Ah
2	Frequency Setting Command	AD57h
3	Receiver Setting Command	C080h
4	Synchron Pattern Command	C1D4h
5	Wake-up Timer Command	E196h
6	Extended Wake-up Timer Command	C300h
7	Low Duty-Cycle Command	CC0Eh
8	Low Battery Detector and Clock Divider Command	C213h
9	AFC Control Command	C687h
10	Data Filter Command	C462h
11	Data Rate Command	C813h
12	FIFO Settings Command	CE87h
13	Extended Features Command	B0CAh
14	Status Register Read Command	0000h

5.3. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	eb	et	ex	x3	x2	x1	x0	i2	i1	i0	dc	928Ah

Bit 12-11 <*b1* : *b0*>:Receiving band selection:

b1	b0	Frequency Band [MHz]
0	0	reserved
0	1	433
1	0	868
1	1	915

Bit 10 <*eb*>: Enables the low battery detector circuit

Bit 9 <*et*>: When set, enables the operation of the wake-up timer

Bit 8 <*ex*>: If *ex* is set the crystal oscillator remains turned on during the inactive periods of the chip

Bit 7:4 <*x3* : *x0*>: Crystal load capacitance. Set according to the crystal's specified load capacitance.

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
……				….
1	1	1	0	15.5
1	1	1	1	16.0

Bit 3:1 <*i2* : *i0*>: Baseband filter bandwidth

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	Reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	135
1	1	0	Reserved
1	1	1	Reserved

Bit 0 <*dc*>: When *dc* bit is set it disables the clock output.

Note: The internal 32 kHz oscillator is turned on by setting the *elfc* bit in the "5.10. Low Battery Detector and Microcontroller Clock Divider Command" on page 21 or the *enldc* bit in the "5.9. Low Duty Cycle Command" on page 20 or by enabling the low battery detector using *eb* bit or by turning on the wake-up timer (*et* bit) in this command.
Clock tail feature: When the clock output (pin 8) used to provide clock signal for the microcontroller (*dc* bit is set to 0), it is possible to use the clock tail feature. This means that the crystal oscillator turn off is delayed, after issuing the command (clearing the *ex* bit) 512 more clock pulses are provided. This ensures that the microcontroller can switch itself to low power consumption mode. It is possible to decrease the clock tail length to 128 pulses by clearing the *ctls* bit in "5.15. Extended Features Command" on page 26.

5.4. Frequency Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	AD57h

The 12-bit parameter F (bits *f11* to *f0*) should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as follows:

$f_0 = 10 \times N \times (C + F/4000)$ [MHz]

The constants N and C are determined by the selected band:

Band [MHz]	N	C
433	4	10
868	8	10
915	8	11

Band	Min Frequency	Max Frequency	PLL Frequency Step
433 MHz	400.96 MHz	439.03 MHz	10 kHz
868 MHz	801.92 MHz	878.06 MHZ	20 kHz
915 MHz	881.92 MHz	958.06 MHz	20 kHz

5.5. Receiver Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d1	d0	g1	g0	r2	r1	r0	en	C080h

Bit 7:6 <*d1 : d0*>: Select the VDI (valid data indicator) signal:

d1	*d0*	VDI output
0	0	Digital RSSI Out (DRSSI)
0	1	Data Quality Detector Output (DQD)
1	0	Clock Recovery Lock
1	1	Always High

Bit 5:4 <*g1 : g0*>: Set the LNA gain:

g1	g0	G_{LNA} (dB relative to maximum gain)
0	0	0
0	1	–6
1	0	–12
1	1	–18

Bit 3:1 <*r2 : r0*>: Control the threshold of the RSSI detector:

r2	r1	r0	$RSSI_{setth}$ [dBm]
0	0	0	–103
0	0	1	–97
0	1	0	–91
0	1	1	–85
1	0	0	–79
1	0	1	–73
1	1	0	–67
1	1	1	–61

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

$$RSSI_{th} = RSSI_{setth} + G_{LNA}$$

Bit 0 <*en*>: Enables the whole receiver chain and crystal oscillator when set. Enable/disable of the wake-up timer and the low battery detect or are not affected by this setting.

5.6. Synchron Pattern Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	1	b7	b6	b5	b4	b3	b2	b1	b0	C1D4h

The synchron pattern consists of two bytes. Byte 1 is fixed 2Dh, Byte 0 is programmable (default D4h) by B <*b7* : *b0*>. For more details, see"5.14. FIFO Settings Command" on page 25.

5.7. Wake-Up Timer Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	0	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by M <*m13* : *m0*> , R <*r3* : *r0*> and C <*c1* : *c0*>:

$$T_{wake\text{-}up} = M \times 2^{R-C} \text{ ms}$$

The upper six bits of M <*m13* : *m8*> and the C <*c1* : *c0*> parameter can be found in the *Extended Wake-Up Timer Command*, see below.

Note: The wake-up timer generates interrupts continuously at the programmed interval while the *et* bit ("5.3. Configuration Setting Command" on page 16) is set.

5.8. Extended Wake-Up Timer Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	1	c1	c0	m13	m12	m11	m10	m9	m8	C300h

These bits can be used to extend the range of the wake-up timer. The explanation of the bits can be found under the Wake-Up Timer Command description (see above).

5.9. Low Duty Cycle Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	d6	d5	d4	d3	d2	d1	d0	enldc	CC0Eh

With this command, autonomous low duty cycle operation can be set up in order to decrease the average power consumption in receive mode.

Bit 7-1 <*d6* : *d0*>: The duty cycle can be calculated by using D <*d6* to *d0*> and M. (M is parameter in a *Wake-Up Timer Command*, see above). The time cycle is determined by the *Wake-Up Timer Command*. duty cycle= (D x 2 +1) / M x 100%

Bit 0 <*enldc*>: Enables the low duty cycle mode. Wake-up timer interrupt is not generated in this mode.

Note: For this operating mode, bit *en* must be cleared in the "5.5. Receiver Setting Command" on page 18 and bit *et* must be set in the "5.3. Configuration Setting Command" on page 16.
In low duty cycle mode the receiver periodically wakes up for a short period of time and checks if there is a valid FSK transmission is in progress. FSK transmission is detected in the frequency range determined by "5.4. Frequency Setting Command" on page 18 plus and minus the baseband filter bandwidth set by the "5.3. Configuration Setting Command" on page 16. This on-time is automatically extended while DQD indicates good received signal condition.

When calculating the on-time take into account the crystal oscillator, the synthesizer, and the PLL need time to start, see the "Table 2. AC Characteristics" on page 6 depending on the DQD parameter, the chip needs to receive a few valid data bits before the DQD signal indicates good signal condition "5.12. Data Filter Command" on page 23. Choosing too short on-cycle can prevent the crystal oscillator from starting or the DQD signal may not go high even when the received signal has good quality.

There is an application proposal shown below. The Si4322 is configured to work in FIFO mode. The chip periodically wakes up and switches to receiving mode. If valid FSK data received, the chip sends an interrupt to the microcontroller and continues filling the RX FIFO. After the transmission is over and the FIFO is read out completely and all other interrupts are cleared, the chip goes back to low power consumption mode.

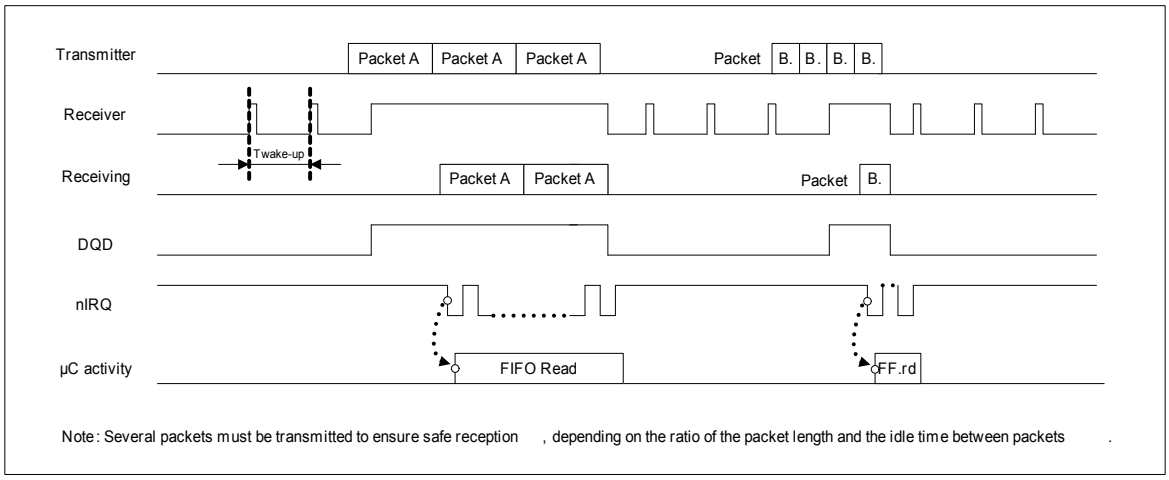


Figure 4. Application Proposal for LPDM (Low Power Duty-Cycle Mode) Receivers

5.10. Low Battery Detector and Microcontroller Clock Divider Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	cd2	cd1	cd0	elfc	t3	t2	t1	t0	C213h

Bit 7:5 <*cd2* : *cd0*>:Clock divider configuration (valid only if the crystal oscillator is on):

cd2	cd1	cd0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

Bit 4 <*elfc*>: Enables the low frequency (32 kHz) clock during sleep mode. The clock signal is present on the CLK pin regardless to the state of the *dc* bit ("5.3. Configuration Setting Command" on page 16).

Bit 3:0 <*t3* : *t0*>: The 4-bit value T of <*t3* : *t0*> determines the threshold voltage of the threshold voltage V_{lb} of the detector:

$$V_{lb} = 2.0\ V + T \times 0.1\ V$$

5.11. AFC Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	a1	a0	rl1	rl0	st	fi	oe	aen	C687h

Bit 0 <*aen*>: Enables the calculation of the offset frequency by the AFC circuit (it allows the addition of the content of the output register to the frequency control word of the PLL).

Bit 1 <*oe*>: Enables the output (frequency offset) register

Bit 2 <*fi*>: Switches the circuit to high accuracy (fine) mode. In this case the processing time is about four times longer, but the measurement uncertainty is less than half.

Bit 3 <*st*>: Strobe edge. When *st* goes to high, the actual latest calculated frequency error is stored into the output registers of the AFC block.

Bit 5:4 <*rl1* : *rl0*>: Limit the value of the frequency offset register to the following values:

rl1	rl0	Max dev [f_{res}]
0	0	No restriction
0	1	±4
1	0	±2
1	1	±1

f_{res}:

434MHz band: 10 kHz

868MHz band: 20 kHz

915MHz band: 20 kHz

Bit 7:6 <*a1* : *a0*>: Automatic operation mode selector:

a1	a0	Operation mode
0	0	Auto mode off (Strobe is controlled by µC)
0	1	Runs only once after each power-up
1	0	Keep the f_{offset} only during receiving (VDI=high).
1	1	Keep the f_{offset} value

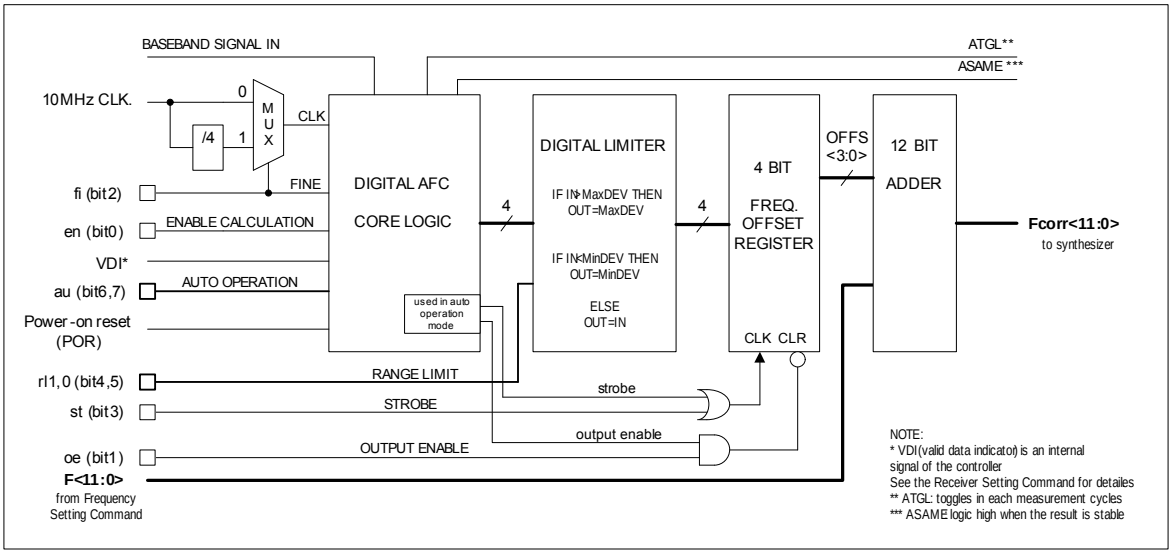


Figure 5. AFC Operation Block Diagram

In manual mode, the strobe signal is provided by the microcontroller. One measurement cycle can compensate about 50-60% of the actual frequency offset. Two measurement cycles can compensate 80%, and three measurement cycles can compensate 92%. The ATGL bit in the status register can be used to determine when the actual measurement cycle is finished.

In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register) the AFC circuit is automatically enabled when the VDI indicates potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

Without AFC the transmitter and the receiver needs to be tuned precisely to the same frequency. RX/TX frequency offset can lower the range. The units must be adjusted carefully during production, stable, expensive crystal must be used to avoid drift or the output power needs to be increased to compensate range loss.

The AFC block will calculate the TX-RX offset. This value will be used to pull the RX synthesizer close to the frequency of the transmitter. The main benefits of the automatic frequency control: low cost crystal can be used, the temperature or aging drift will not cause range loss and no production alignment needed.

There are four operation modes:

1. (*a1*=0, *a0*=0) Automatic operation of the AFC is off. Strobe bit can be controlled by the microcontroller.

2. (*a1*=0, *a0*=1) The circuit measures the frequency offset only once after power up. This way, extended TX-RX distance can be achieved. In the final application, during the first receiving cycle, the circuit measures and compensates for the frequency offset caused by the crystal tolerances. This method allows the use of lower cost crystal in the application and provides protection against tracking an interferer.
3. (*a1*=1, *a0*=0) The frequency offset is calculated automatically and the center frequency is corrected when the VDI is high. The calculated value is dropped when the VDI goes low. To improve the efficiency of the AFC calculation two methods are recommended:
   a. The transmit package should start with a low effective baud rate pattern (i.e.: 00110011) because it is easier to receive. The circuit automatically measures the frequency offset during this initial pattern and changes the receiving frequency accordingly. The further part of the package will be received by the corrected frequency settings.
   b. The transmitter sends the first part of the packet with a step higher deviation than required during normal operation to ease the receiving. After the frequency shift was corrected, the deviation can be reduced.

   In both cases (3a and 3b), when the VDI indicates poor receiving conditions (VDI goes low), the output register is automatically cleared. Use this "drop offset" mode when the receiver communicates with more than one transmitter.
4. (*a1*=1, *a0*=1) It is similar mode 3, but suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is kept independently of the state of the VDI signal. When the receiver is paired with only one transmitter, it is possible to use this "keep offset" mode. In this case, the DRSSI limit should be selected carefully to minimize the range hysteresis.

5.12. Data Filter Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	al	ml	dsfi	sf	ewi	f2	f1	f0	C462h

Bit 7 <*al*>: Clock recovery (CR) auto lock control
1: auto mode: the CR starts in fast mode and after locking it switches to slow mode. The *ml* bit (Bit 6) has no effect.
0: manual mode: the clock recovery mode is set by Bit 6 <*ml*>

Bit 6 <*ml*>: Clock recovery lock control
1: fast mode, fast attack and fast release (4 to 8-bit preamble (1010...) is recommended)
0: slow mode, slow attack and slow release (12 to 16-bit preamble is recommended)
Using the slow mode requires more accurate bit timing (see "5.13. Data Rate Command" on page 24).

Bit 5 <*dsfi*>: Disables auto-sleep on FIFO interrupt if set to 1.

This mode helps to decrease the average current consumption of the receiver. In normal mode (auto-sleep is disabled) the receiver remains active after receiving a given number of bits (set by the FIFO IT level, see the "5.14. FIFO Settings Command" on page 25). If the auto-sleep is enabled the part goes to stand-by mode when FIFO interrupt occurs – increasing this way the battery life. Use this mode when the transmitted data length is known and set the FIFO IT level to this value.

Bit 4 <*sf*>: Selects the type of the data filter

sf	Filter Type
0	Digital filter
1	Analog RC filter

Digital Filter: This is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the "5.13. Data Rate Command" on page 24.

Note: Bit rate cannot exceed 115 kbps in this mode.

Analog RC filter: The demodulator output is fed to pin 7 over a 10 kΩ resistor. The filter cut-off frequency is set by the external capacitor connected to this pin and VSS.

The table shows the optimal filter capacitor values for different data rates.

Data Rate [kbps]	1.2	2.4	4.8	9.6	19.2	38.4	57.6	115.2	256
Filter Capacitor Value	12 nF	8.2 nF	6.8 nF	3.3 nF	1.5 nF	680 pF	270 pF	150 pF	100 pF

Note: If analog RC filter is selected the internal clock recovery circuit and the FIFO cannot be used.

Bit 3 <*ewi*>: Enables the automatic wake-up on any interrupt event. When the *ewi* bit is set, the crystal oscillator turns on automatically when an interrupt occurs. This time the crystal oscillator stays active until all the active interrupts cleared. Clearing the *ex* bit in the "5.3. Configuration Setting Command" on page 16 will not stop the oscillator.

Bit 2:0 <*f2 : f0*>: DQD threshold parameter. The Data Quality Detector is a digital processing part of the radio, connected to the demodulator—it is an indicator reporting the quality of an FSK modulated RF signal. It works every time when the receiver is on. Setting its parameter defines how clean should be the incoming data stream to be qualified as good data (valid FSK signal).

If the internally calculated data quality value exceeds the DQD threshold parameter for five consecutive data bits for both the high and low periods, then the DQD signal goes high.

The DQD parameter in the Data Filter Command should be chosen according to the following rules:

- The DQD parameter can be calculated with the following formula:
  DQD_{par} = 4 x (deviation – $TX\text{-}RX_{offset}$) / bit rate
- It should be larger than 4 because otherwise noise might be treated as a valid FSK signal.
- The maximum value is 7.

5.13. Data Rate Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C813h

Bit 7 <*cs*>: Enables the prescaler in the data rate clock generation circuit (1/8 divider)

Bit 6:0 <*r6* : *r0*>: The seven bit value of R <*r6* : *r0*> sets the divider ratio of the data rate clock generation circuit

The expected bit rate of the received data stream is determined by the R value and the *cs* bit. Set R according the next function:

R = (10 MHz / 29 / (1 + *cs* x 7) / BR) – 1, where BR is the bit rate

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Data rate accuracy requirements:

Clock recovery in slow mode: $\Delta BR/BR < 1 / (29 \times N_{bit})$ Clock recovery in fast mode: $\Delta BR/BR < 3 / (29 \times N_{bit})$

BR is the bit rate set in the receiver and ΔBR is bit rate difference between the transmitter and the receiver. N_{bit} is the maximal number of consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1→0 and 0→1 transitions, and be careful to use the same division ratio in the receiver and in the transmitter.

ΔBR is a theoretical limit for the clock recovery circuit. Clock recovery will not work above this limit. The clock recovery circuit will always operate below this limit independently from process, temperature, or V_{DD} condition.

Supposing that the maximum length of consecutive zeros or ones in the data stream is less than 5 bits, the necessary relative accuracy is 0.68% in slow mode and 2.1% in fast mode.

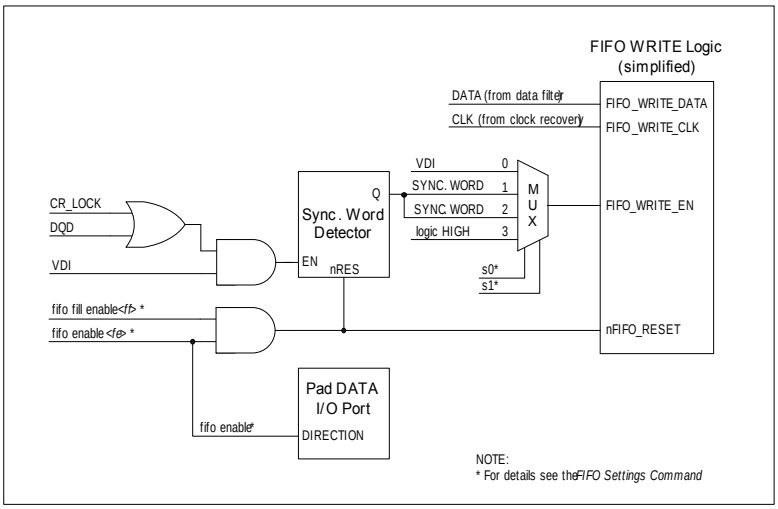
5.14. FIFO Settings Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	s1	s0	ff	fe	CE87h

Bit 7:4 <*f3* : *f0*>: Together with bits <*f5* : *f4*> of the *Extended Features Command* (see below) determines the FIFO IT level. The FIFO generates IT when the number of the received data bits reaches this level.

Bit 3:2 <*s1* : *s0*>: Select the input of the FIFO fill start condition:

s1	s0	FIFO Start Condition
0	0	VDI
0	1	Synchron Pattern
1	0	
1	1	Always



Note: For details of the VDI (Valid Data Indicator) signal see the "5.5. Receiver Setting Command" on page 18.

The synchron pattern consists of two bytes. Byte 1 is fixed 2Dh, Byte 0 is programmable (default D4h) in the "5.6. Synchron Pattern Command" on page 19.

Bit 1 <*ff*>: Enables FIFO fill after synchron word reception. FIFO fill stops when this bit is cleared.

Bit 0 <*fe*>: Enables the 64-bit deep FIFO mode. To clear the counter of the FIFO, it has to be set to zero.

Note: To restart the synchron word reception, the *ff* bit should be cleared and set. This action will initialize the FIFO and clear its content.

The *fe* bit modifies the function of DATA (pin 6) and DCLK (pin 7) outputs. The DATA pin becomes FIFO select input (nFFS). If the chip is used in FIFO mode, do not allow this to be a floating input. The DCLK pin changes to FIFO interrupt output (FFIT) if this bit is set to 1.

5.15. Extended Features Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	1	ctls	0	dcal	bw1	bw0	f5	f4	B0CAh

Bit 6 <*ctls*>: Clock tail selection bit. Clearing this bit selects 128-bit long clock tail instead of the default 512-bit length.

Bit 4 <*dcal*>: Disables the wake-up timer auto-calibration.

Bit 3:2 <*bw1:bw0*>: Select the bandwidth of the PLL

bw1	bw0	PLL bandwidth
0	0	15 kHz
0	1	30 kHz
1	0	60 kHz
1	1	120 kHz

Bit 1:0 <*f5* : *f4*>: Upper two bits for selecting the 64-bit FIFO IT level together with the *f3-f0* bits in "5.14. FIFO Settings Command" on page 25.

5.16. Status Register Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h

The read command starts with a zero, whereas all other control commands start with a one. Therefore, after receiving the first bit of the control command the Si4322 identifies it as a read command. Therefore, as the first bit of the command is received, the receiver starts to clock out the status bits on the SDO output as follows:

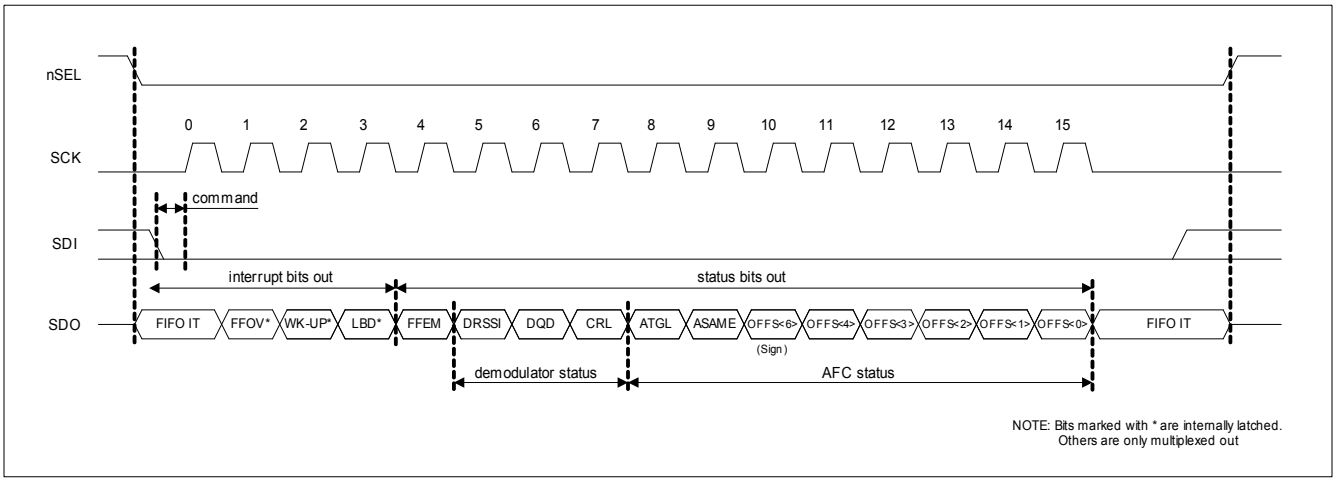


Figure 6. Status Register Read Sequence

Note: The FIFO IT bit behaves like a status bit, but generates nIRQ pulse if active. To check whether there is a sufficient amount of data in the FIFO, the SDO output can be tested. In extreme speed critical applications, it can be useful to read only the first four bits (FIFO IT to LBD) to clear the FFOV, WK-UP, and LBD bits.

Table 7. Status Register Read Timing Diagram Bits Definitions

Bit Name	Function
FFIT	The number of data bits in the FIFO has reached the preprogrammed limit
FFOV	FIFO overflow
WK-UP	Wake-up timer overflow
LBD	Low battery detect, the power supply voltage is below the preprogrammed limit
FFEM	FIFO is empty
DRSSI	The strength of the incoming signal is above the preprogrammed limit
DQD	Data Quality Detector detected a good quality signal
CRL	Clock recovery lock
ATGL	Toggling in each AFC cycle
ASAME	AFC measured twice the same result
OFFS(6)	MSB of the measured frequency offset (sign of the offset value)
OFFS(4)–OFFS(0)	Offset value to be added to the value of the selected center frequency

6. Interrupt Handling

In order to achieve low power consumption there is an advanced event handling circuit implemented. The device has a very low power consumption mode, so called sleep mode. In this mode only a few parts of the circuit are working. In case of an event, an interrupt signal generated on the nIRQ pin to indicate the changed state to the microcontroller. If the *ewi* bit was set in the "5.13. Data Rate Command" on page 24 the device wakes up and switches into idle mode. The cause of the interrupt can be determined by reading the status word of the device (see "5.16. Status Register Read Command" on page 26).

Several interrupt sources are available:

FFIT—The number of the received bits in the RX FIFO reached the preprogrammed level: When the number of received data bits in the receiver FIFO reaches the threshold set by the *f5…f0* bits of the "5.14. FIFO Settings Command" on page 25 and the "5.15. Extended Features Command" on page 26 an interrupt is generated. Valid only when the *fe* (enable FIFO mode) bit is set in the FIFO settings command and the receiver is enabled in the "5.5. Receiver Setting Command" on page 18.

FFOV—FIFO overflow: There are more bits received than the capacity of the FIFO (64 bits). Valid only when the *fe* (enable FIFO mode) bit is set in the FIFO settings command and the receiver is enabled in the receiver setting command.

WKUP—Wake-up timer interrupt: This interrupt event occurs when the time specified by the "5.7. Wake-Up Timer Command" on page 19 has elapsed. Valid only when the *et* bit is set in the configuration setting command.

LBD—Low battery detector interrupt: Occurs when the V_{DD} goes below the programmable low battery detector threshold level (*t3…t0* bits in the "5.10. Low Battery Detector and Microcontroller Clock Divider Command" on page 21). Valid only when the eb (enable low battery detector) bit is set in the configuration setting command.

If an interrupt occurs the nIRQ pin will change to logic low level, and the corresponding bit in the status byte will be 1.

Clearing an interrupt actually implies two things:

- Releasing the nIRQ pin to return to logic high
- Clearing the corresponding bit in the status byte

To clear an interrupt requires different procedure depending on the interrupt type:

FFIT—Both the nIRQ pin and the status bit remain active until the FIFO is read (a FIFO IT threshold number of bits have been read), the receiver is switched off, or the RX FIFO is switched off.

FFOV—This bit is always set together with FFIT; it can be cleared by the status read command, but the FFIT bit and hence the nIRQ pin will remain active until the FIFO is read fully or the RX FIFO is switched off.

WKUP—Both the nIRQ pin and the status bit can be cleared by the *Status Read Command*

LBD—The nIRQ pin can be released by the reading the status, but the status bit will remain active while the V_{DD} is below the threshold.

The best practice in interrupt handling is to start with a status read when interrupt occurs, and then make a decision based on the status byte. It is very important to mention that any interrupt can “wake up” the EZradio chip from sleep mode if the ewi bit is set in the "5.12. Data Filter Command" on page 23. In this case the crystal oscillator will start and the Si4322 will not go to low current sleep mode if any interrupt remains active regardless to the state of the ex (enable crystal oscillator) bit in the "5.3. Configuration Setting Command" on page 16. This way the microcontroller always can have clock signal to process the interrupt. To prevent high current consumption and this way short battery life, it is strongly advised to process and clear every interrupt before turning off the crystal oscillator. All unnecessary functions should be turned off to avoid unwanted interrupts. Before freezing the microcontroller code, a thorough testing must be performed in order to make sure that all interrupt sources are handled properly and the part goes to low power consumption (sleep) mode when the crystal oscillator turned off.

7. FIFO Buffered Data Read

In this operating mode, incoming data are clocked into a 64-bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and/or the synchron word recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

For further details see "5.5. Receiver Setting Command" on page 18 and "5.14. FIFO Settings Command" on page 25.

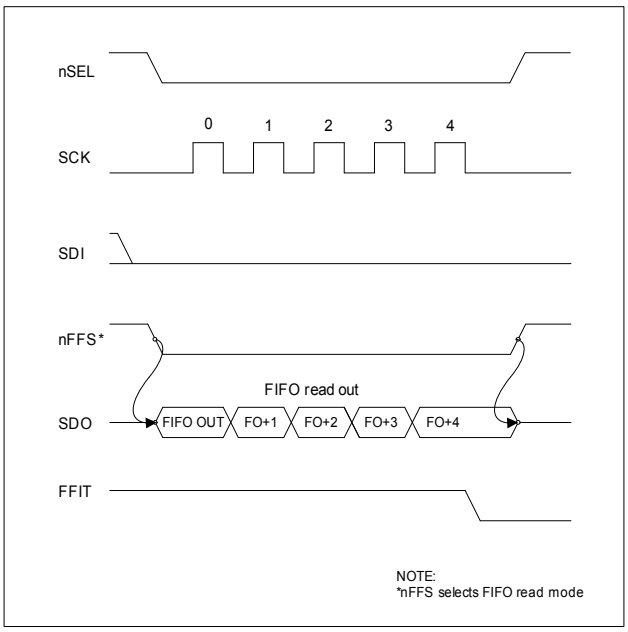
7.1. Polling Mode

The nFFS signal selects the buffer directly and its content could be clocked out through pin SDO by SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken. An SPI read command is also available.

7.2. Interrupt Controlled Mode

The user can define the FIFO level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.

7.3. FIFO Read Example with FFIT Polling



Note: During FIFO access f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency. When the duty-cycle of the clock signal is not 50% the shorter period of the clock pulse should be at least $2/f_{ref}$.

8. Power Saving Modes

The different operating modes of the chip depend on the following control bits:

Operating Mode	*eb* or *et* or *elfc*	en	ex	I_{DD} (typ)
Active	X	1	X	12 mA
Idle	X	0	1	0.5 mA
Sleep	1	0	0	5 µA*
Standby	0	0	0	0.3 µA
***Note:** Maximum value.				

eb, *et*, *ex* bits—"5.3. Configuration Setting Command" on page 16

elfc bit—"5.10. Low Battery Detector and Microcontroller Clock Divider Command" on page 21

en bit—"5.5. Receiver Setting Command" on page 18

Active mode—The whole receiver chain and the crystal oscillator both turned on.

Idle mode—The receiver is not active, only the crystal oscillator is running.

Sleep mode—Only the low frequency (32 kHz) RC oscillator is running. This oscillator also runs when the wake-up timer or the low battery detector is enabled, providing them a timing signal.

Stand-by mode—All circuits are turned off.

9. Dual Clock Output

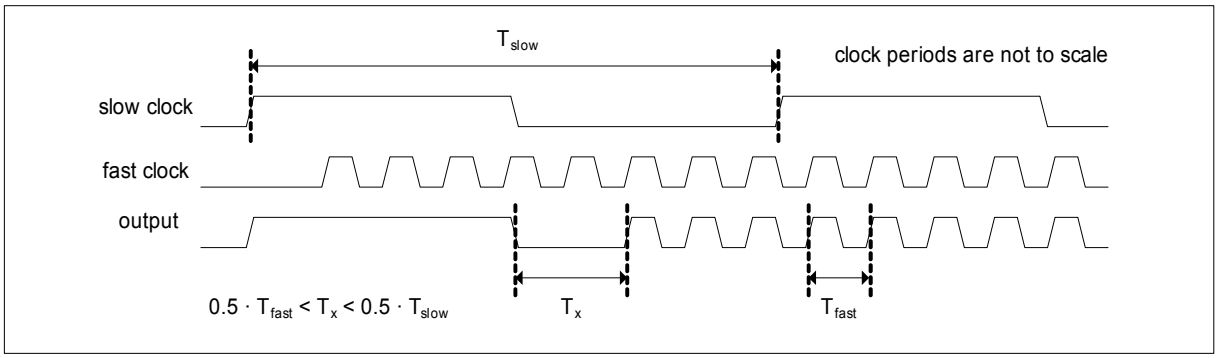
When the chip is switched into idle mode, the 10 MHz crystal oscillator starts. After oscillation ramp-up a 1 MHz clock signal is available on the CLK pin. This (fast) clock frequency can be reprogrammed during operation with the "5.10. Low Battery Detector and Microcontroller Clock Divider Command" on page 21. During startup and in sleep or standby mode (crystal oscillator disabled), the CLK output is pulled to logic low.

On the same pin a low frequency clock signal can be obtained if the *elfc* bit is set in the low battery and microcontroller clock divider command. The clock frequency is 32 kHz, which is derived from the low-power RC oscillator. The clock signal is present on the CLK pin regardless the state of the *dc* bit in the "5.3. Configuration Setting Command" on page 16.

Slow clock feature can be enabled by entering into sleep mode (clearing the *en* and *ex* bits and setting the *elfc* bit). Driving the output will increase the sleep mode supply current. Actual worst-case value can be determined when the exact load and min/max operating conditions are defined. After power-on reset the chip goes into sleep mode and the slow frequency clock appears on the CLK pin.

Switching back into fast clock mode can be done by setting the *ex* bit in the configuration setting command or the *en* bit in the "5.5. Receiver Setting Command" on page 18. It is important to leave bit *dc* in the Configuration Setting Command at its default state (0) otherwise there will be no clock signal on the CLK pin.

Switching between the fast and slow clock modes is glitch-free in a sense that either state of the clock lasts for at least a half cycle of the fast clock. During switching the clock can be logic low once for an intermediate period i.e. for any time between the half cycle of the fast and the slow clock.



The clock switching synchronization circuit detects the falling edges of the clocks. One consequence is a latency of 0 to T_{slow} + T_{fast} from the occurrence of a clock change request (entering into sleep mode or interrupt) until the beginning of the intermediate length (T_x) half cycle. The other is that both clocks should be up and running for the change to occur. Changing from fast to slow clock, it is automatically ensured by entering into the sleep mode if the *elfc* bit is enabled. As the crystal oscillator is normally stopped while the slow clock is used, when changing back to fast clock the crystal oscillator startup time has to pass first before the above mentioned latency period starts. The startup condition is detected internally, so no software timing is necessary.

10. Wake-Up Timer Calibration

By default, the wake-up timer is calibrated every time it is enabled by setting the *et* bit in the "5.3. Configuration Setting Command" on page 16. After timeout the timer restarts automatically and can be stopped by resetting the *et* bit. If the timer is programmed to run for longer periods, at approximately every 30 seconds it performs additional self-calibration.

This feature can be disabled to avoid sudden changes in the actual wake-up time period. A suitable software algorithm can then compensate for the gradual shift caused by temperature change.

Bit *dcal* in the "5.15. Extended Features Command" on page 26 controls the automatic calibration feature. It is reset to 0 at power-on and the automatic calibration is enabled. This is necessary to compensate for process tolerances. After one calibration cycle further (re)calibration can be disabled by setting this bit to 1.

11. RX-TX Alignment Procedures

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver, the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the *aen* bit in the "5.11. AFC Command" on page 21.

12. Crystal Selection Guidelines

The crystal oscillator of the Si4322 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 100 Ω ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (f_{LO}). Therefore, f_{LO} is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C_0.

The on chip AFC is capable to correct TX/RX carrier offsets as much as 80% of the deviation of the received FSK modulated signal.

12.1. Maximum Crystal Tolerances Including Temperature and Aging [ppm]

Table 8. Bit Rate: 2.4 kbps

	Transmitter Deviation [± kHz]							
	20	**40**	**60**	**80**	**100**	**120**	**140**	**160**
433 MHz	3	25	50	70	80	100	100	100
868 MHz	2	12	25	30	40	50	70	80
915 MHz	2	12	20	30	40	50	60	70

Table 9. Bit Rate: 9.6 kbps

	Transmitter Deviation [± kHz]							
	20	**40**	**60**	**80**	**100**	**120**	**140**	**160**
433 MHz	don't use	15	40	50	70	100	133	156
868 MHz	don't use	8	20	30	40	50	60	70
915 MHz	don't use	8	15	30	40	50	60	70

Table 10. Bit Rate: 38.4 kbps

	Transmitter Deviation [± kHz]							
	20	**40**	**60**	**80**	**100**	**120**	**140**	**160**
433 MHz	don't use	don't use	20	40	50	70	100	100
868 MHz	don't use	don't use	10	20	30	40	50	70
915 MHz	don't use	don't use	10	20	30	40	50	60

Table 11. Bit Rate: 115.2 kbps

	Transmitter Deviation [± kHz]							
	20	**40**	**60**	**80**	**100**	**120**	**140**	**160**
433 MHz	don't use	don't use	don't use	don't use	don't use	3	25	50
868 MHz	don't use	don't use	don't use	don't use	don't use	2	12	25
915 MHz	don't use	don't use	don't use	don't use	don't use	2	12	20

13. Reset modes

The chip will enter into reset mode if any of the following conditions are met:

- Power-on reset: During a power up sequence until the V_{dd} has reached the correct level and stabilized
- Power glitch reset: Transients present on the V_{DD} line
- Software reset: Special control command received by the chip

13.1. Power-On Reset

After power up the supply voltage starts to rise from 0 V. The reset block has an internal ramping voltage reference (reset-ramp signal), which is rising at 100 mV/ms (typical) rate. The chip remains in reset state while the voltage difference between the actual V_{DD} and the internal reset-ramp signal is higher than the reset threshold voltage, which is 600 mV (typical). As long as the V_{DD} voltage is less than 1.6 V (typical) the chip stays in reset mode regardless the voltage difference between the V_{DD} and the internal ramp signal.

The reset event can last up to 100 ms supposing that the V_{DD} reaches 90% its final value within 1 ms. During this period, the chip does not accept control commands via the serial control interface.

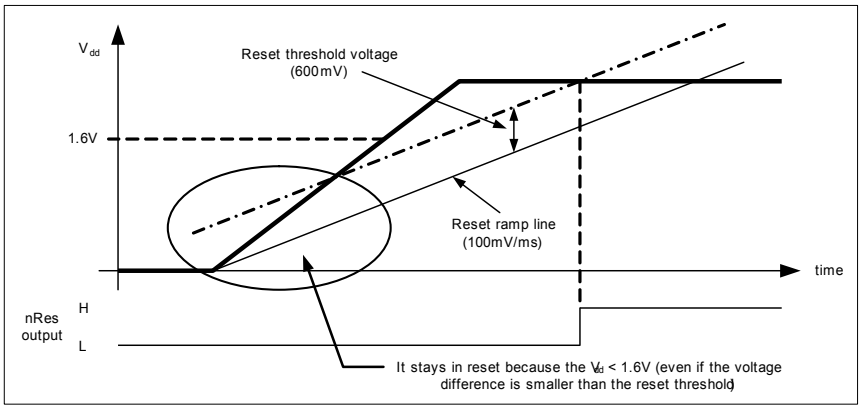


Figure 7. Power-On Reset Example

13.2. Power Glitch Reset

The internal reset block has two basic mode of operation: normal and sensitive reset. The default mode is sensitive, which can be changed by the appropriate control command (see related control commands at the end of this section). In normal mode the power glitch detection circuit is disabled.

There can be spikes or glitches on the V_{DD} line if the supply filtering is not satisfactory or the internal resistance of the power supply is too high. In such cases if the sensitive reset is enabled an (unwanted) reset will be generated if the positive going edge of the V_{DD} has a rising rate greater than 100 mV/ms and the voltage difference between the internal ramp signal and the V_{DD} reaches the reset threshold voltage (600 mV). Typical case when the battery is weak and due to its increased internal resistance a sudden decrease of the current consumption (for example turning off the power amplifier) might lead to an increase in supply voltage. If for some reason the sensitive reset cannot be disabled step-by-step decrease of the current consumption (by turning off the different stages one by one) can help to avoid this problem.

Any negative change in the supply voltage will not cause reset event unless the V_{DD} level reaches the reset threshold voltage (250 mV in normal mode, 1.6V in sensitive reset mode).

If the sensitive mode is disabled and the power supply turned off the V_{DD} must drop below 250 mV in order to trigger a power-on reset event when the supply voltage is turned back on. If the decoupling capacitors keep their charges for a long time it could happen that no reset will be generated upon power-up because the power glitch detector circuit is disabled.

Note that the reset event reinitializes the internal registers, so the sensitive mode will be enabled again.

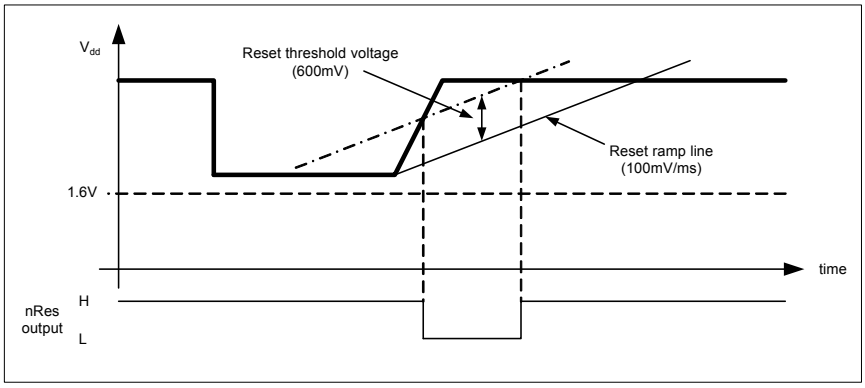


Figure 8. Sensitive Reset Enabled, Ripple on V_{DD}

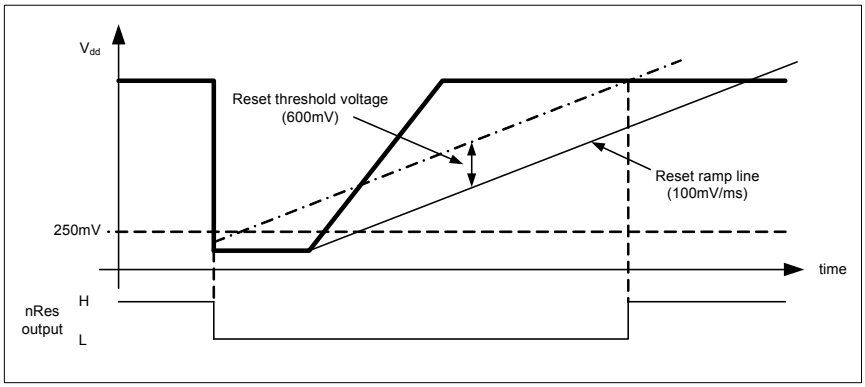


Figure 9. Sensitive Reset Disabled

13.2.1. Software Reset

Software reset can be issued by sending the appropriate control command to the chip. The result of the command is the same as if power-on reset was occurred but the length of the reset event is much less, 0.25 ms typical. The software reset works only when the sensitive reset mode is selected.

13.2.2. V_{DD} Line Filtering

During the reset event (caused by power-on, fast positive spike on the supply line or software reset command), it is very important to keep the V_{DD} line as smooth as possible. Noise or periodic disturbing signal superimposed the supply voltage may prevent the part getting out from reset state. To avoid this phenomenon use adequate filtering on the power supply line to keep the level of the disturbing signal below 100 mV_{PP} in the DC – 50 kHz range for 200 ms from V_{DD} ramp start. Typical example when a switch-mode regulator is used to supply the radio, switching noise may be present on the V_{dd} line. Follow the manufacturer's recommendations how to decrease the ripple of the regulator IC and/or how to shift the switching frequency.

13.2.3. Related Control Commands

Reset Mode Command—Sending D540h command to the chip will change the reset mode to normal from the default sensitive. Write D500h to the control interface in order to switch back to the sensitive mode.

SW Reset Command—Issuing FF00h command will trigger software reset (sensitive reset mode must be enabled).

14. Typical Performance Characteristics

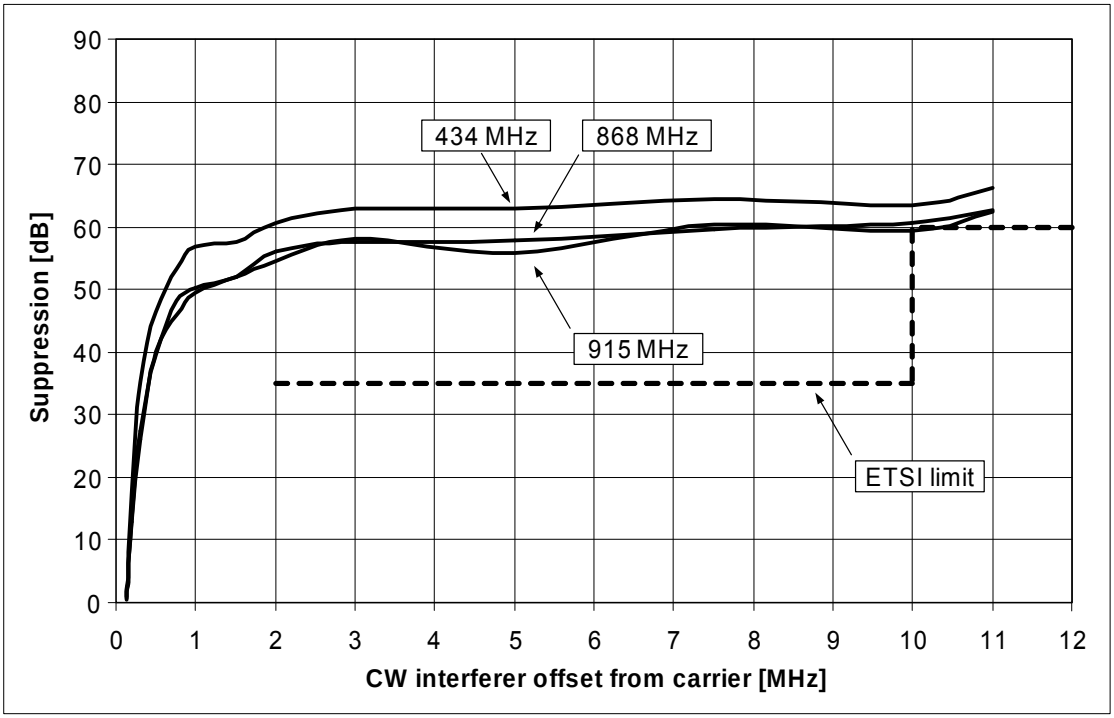


Figure 10. Channel Selectivity and Blocking

Notes:

- LNA gain: maximum, filter bandwidth: 135 kHz, data rate: 9.6 kbps, AFC: switched off, FSK deviation: ±60 kHz, V_{DD} = 2.7 V
- The measurement was done according to the descriptions in the ETSI Standard EN 300 220-2 v.2.1.2 (2007-06), section 4.3.3. and 4.3.4., referring to EN 300 220-1 v2.1.1 (2006-04), section 9.
- The ETSI limit given in the figure is drawn by taking –104 dBm at 9.6 kbps typical sensitivity into account, and corresponds to receiver class 2 requirements (section 4.1.1).

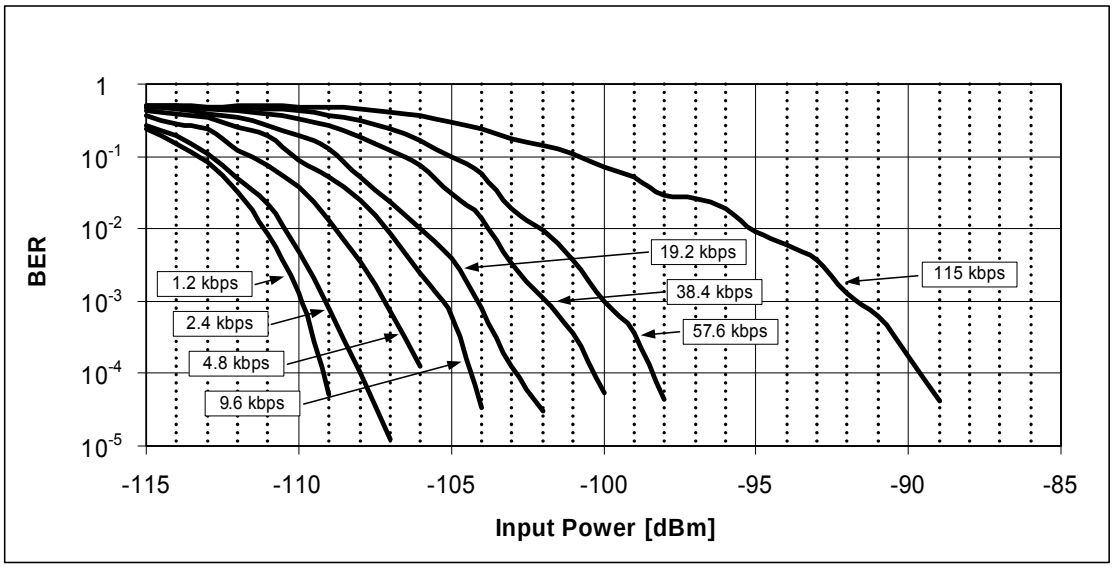


Figure 11. BER Curves in 433 MHz Band

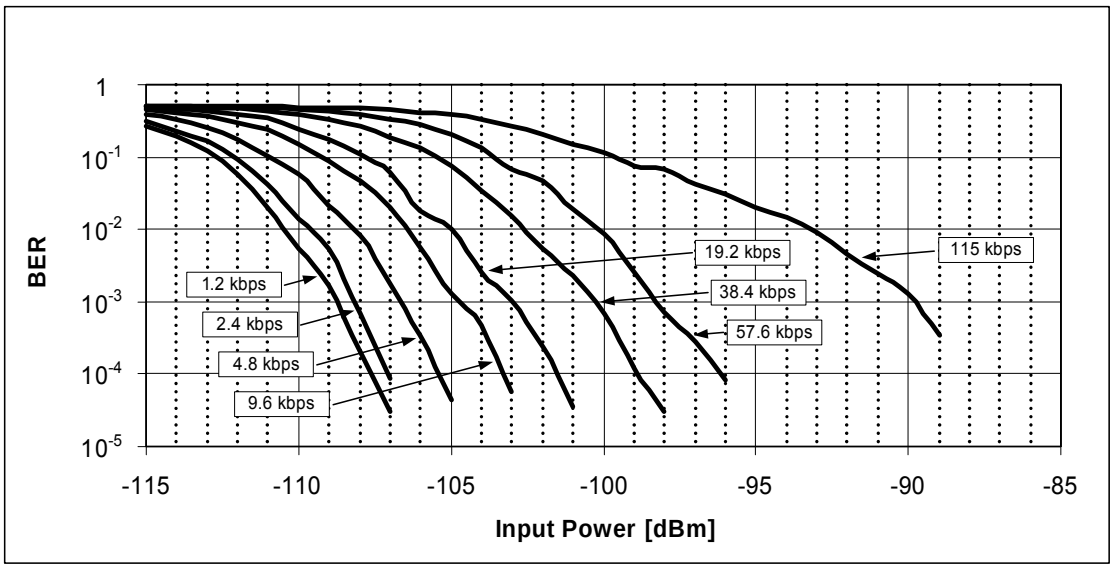


Figure 12. BER Curves in 868 MHz Band

Note: LNA gain: maximum, V_{DD} = 3.0 V

The table below shows the optimal receiver baseband bandwidth (BW) and transmitter deviation frequency (δf_{FSK}) settings for different data-rates supposing no transmit receive offset frequency. If TX/RX offset (for example due to crystal tolerances) have to be taken into account, increase the BW accordingly.

1.2 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115.2 kbps
BW=135 kHz δf_{FSK} =60 kHz	BW=135 kHz δf_{FSK} =60 kHz	BW=135 kHz δf_{FSK} =60 kHz	BW=135 kHz δf_{FSK} =60 kHz	BW=135 kHz δf_{FSK} =60 kHz	BW=135 kHz δf_{FSK} =100 kHz	BW=200 kHz δf_{FSK} =120 kHz	BW=270 kHz δf_{FSK} =140 kHz

15. Reference Design: Evaluation Board with 50 Ω Matching Network

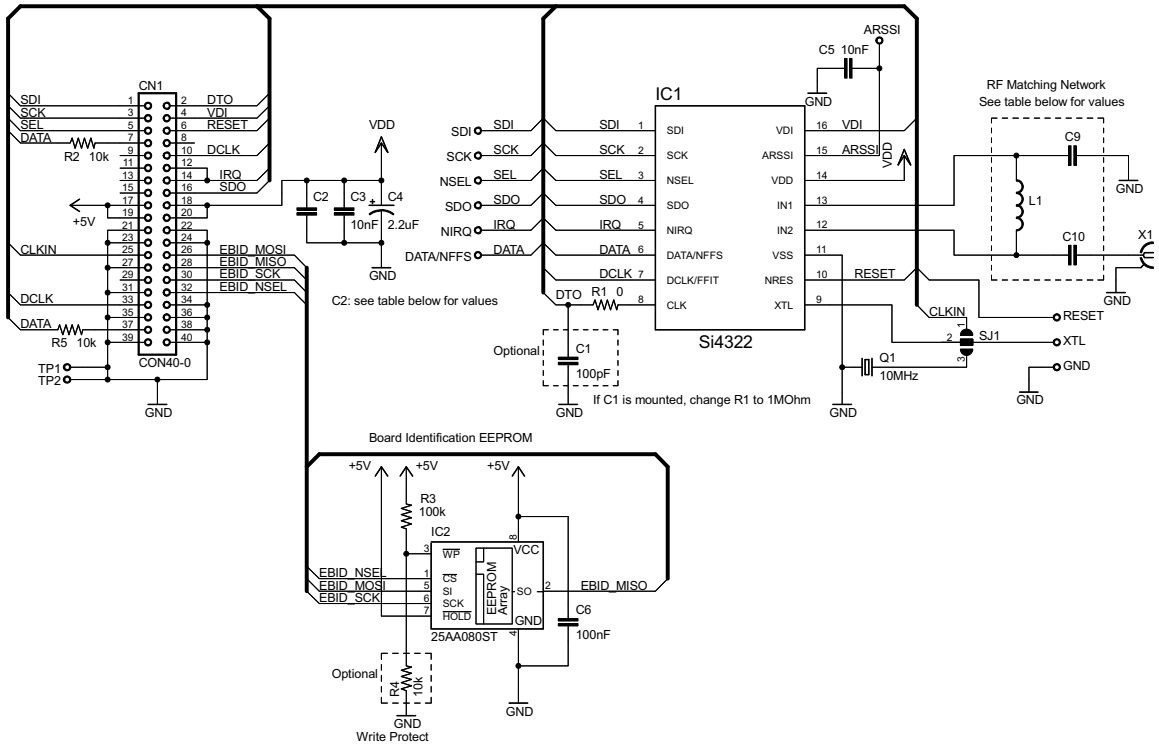


Figure 13. Schematic

Table 12. Frequency Dependent Component Values

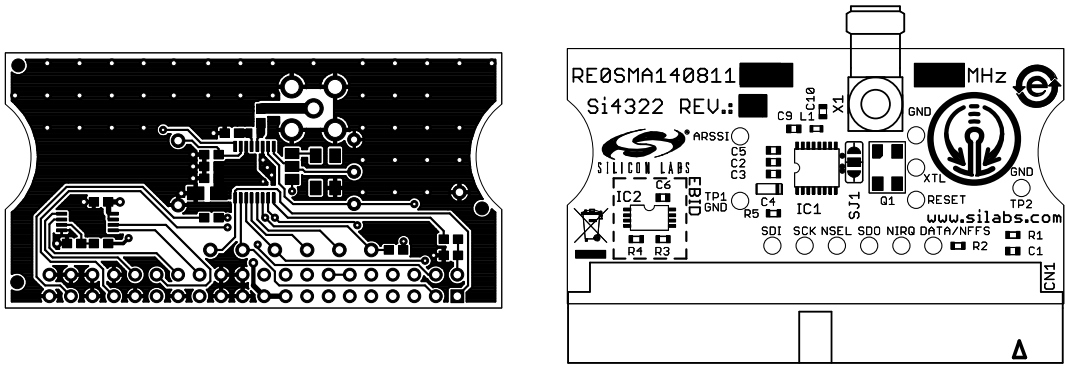
f [MHz]	L1 [nH]	C2 [pF]	C9 [pF]	C10 [pF]
434	33	220	6.8	6.8
868	15	39	2.2	3
915	15	39	2.2	3

Table 13. Recommended Component Types

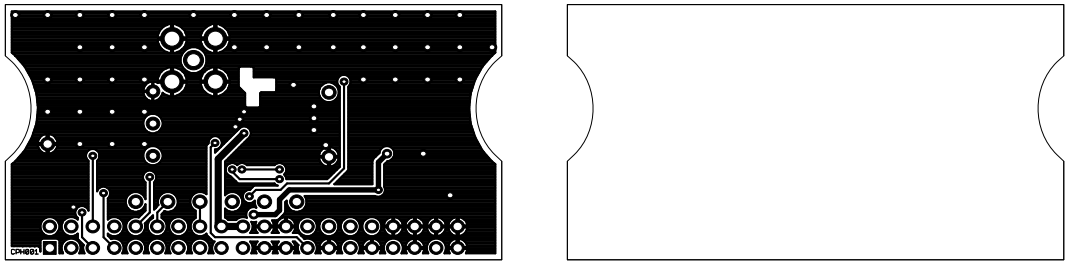
Component	Manufacturer	Part Number			Note
		434 MHz	868 MHz	915 MHz	
L1	Coilcraft	0603CS-33NX	0603CS-15NX	0603CS-15NX	1
C2	Murata	GRM1885C1H221JA01B	GRM1885C1H390JZ01B	GRM1885C1H390JZ01B	2
C9	Murata	GRM1885C1H6R8DZ01B	GRM1885C1H2R2CZ01B	GRM1885C1H2R2CZ01B	2
C10	Murata	GRM1885C1H6R8DZ01B	GRM1885C1H3R0CZ01B	GRM1885C1H3R0CZ01B	2

Notes:
1. SRF, DCR and Q should be similar if components from other manufacturer used.
2. The dielectric type should be C0G and the resonant frequency should be similar if components from alternative vendor used.

16. PCB Layout



Top View



Bottom View

17. Pin Descriptions—Si4322

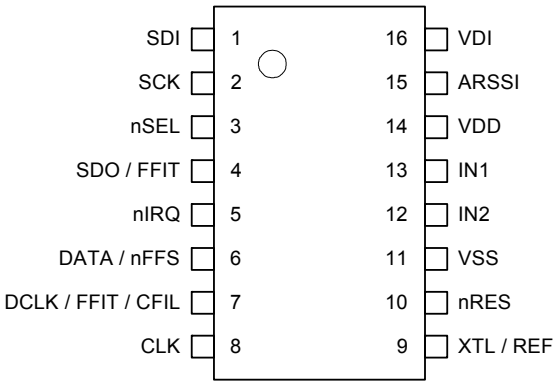


Figure 14. Pin Configurations

Table 14. Pin Descriptions

Pin	Name	Type	Description
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of serial control interface (active low)
4	SDO	DO	Serial data output. Tristate with bus-hold cell if nSEL = H
	FFIT	DO	FIFO IT output. See "5.16. Status Register Read Command" on page 26 for details.
5	nIRQ	DO	Interrupt request output (active low)
6*	DATA	DO	Received data output (FIFO not used)
	nFFS	DI	FIFO select input (active low) with internal pull-up resistor (120 kΩ)
7*	DCLK	DO	Received data clock output (digital filter used, FIFO not used)
	FFIT	DO	FIFO IT output. FIFO empty function can be achieved if FIFO IT level is set to 1.
	CFIL	AIO	External data filter capacitor connection (if analog RC filter is used)
8	CLK	DO	Clock output for the microcontroller
9	XTL	AIO	Crystal connection (connect the other terminal of the crystal to VSS)
	REF	DI	External reference input
10	nRES	DO	Reset output (active low)
11	VSS	S	Negative supply voltage
12	IN2	AI	RF differential signal input
13	IN1	AI	RF differential signal input
14	VDD	S	Positive supply voltage
15	ARSSI	AO	Analog RSSI output
16	VDI	DO	Valid Data Indicator output
Note: For detailed information about the functions of pin 6 and pin 7 see Table 5 on page 9.			

18. Ordering Guide

Part Ordering #	Temperature	Package
Si4322-A1-FT	–40 to +85 °C	16-Pin TSSOP
Note: Add an “R” at the end of the device to denote tape and reel option; 2500 quantity per reel.		

19. Package Outline: 16-Pin TSSOP

Figure 15 illustrates the package details for the Si4322. Table 15 lists the values for the dimensions shown in the illustration.

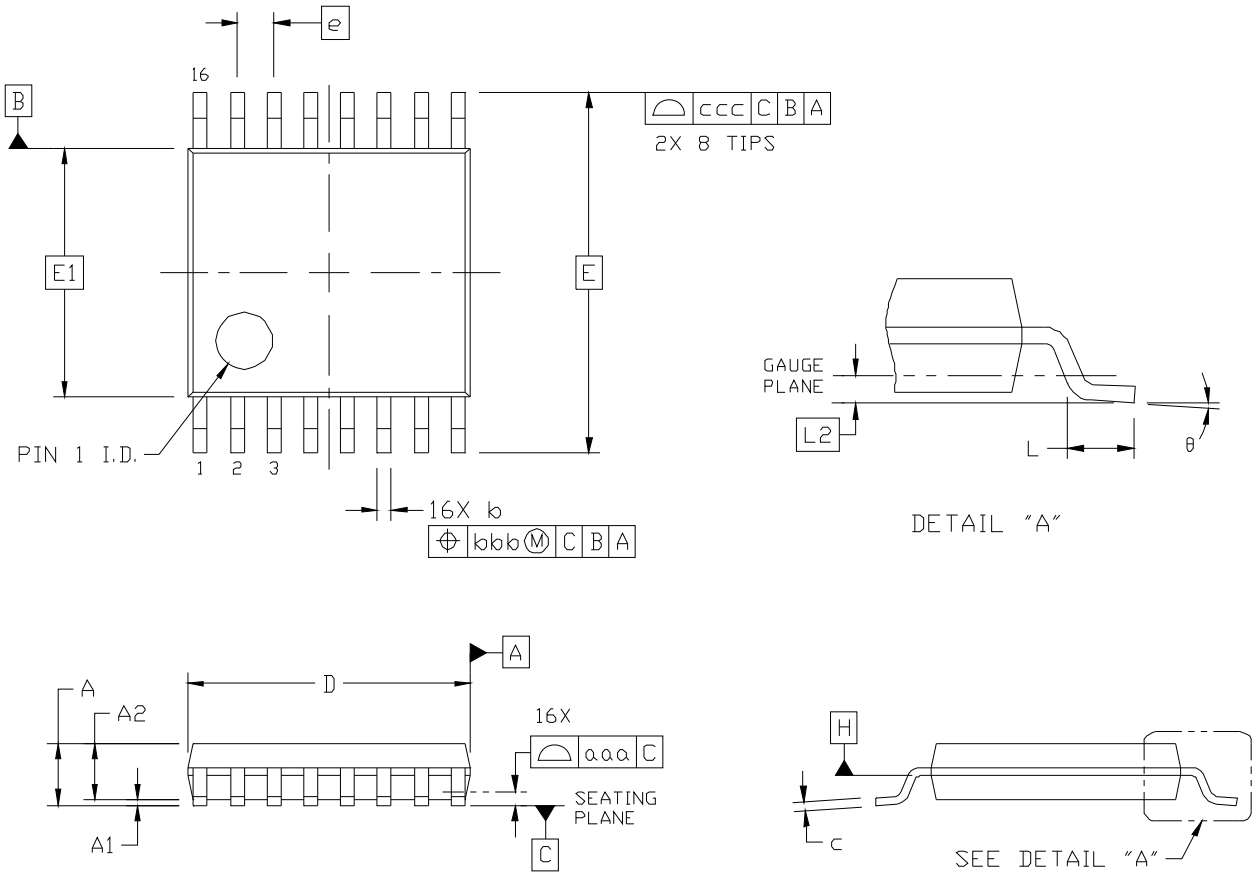


Figure 15. 16-Pin TSSOP

Table 15. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.20		

NOTES:

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