LPC3180/01

16/32-bit ARM microcontroller; hardware floating-point coprocessor, USB On-The-Go, and SDRAM memory interface

Rev. 00.08 — 20 November 2008 **Preliminary data sheet**

1. General description

The LPC3180/01 is an ARM9-based microcontroller for embedded applications designed for high performance and low power dissipation. To achieve these objectives, NXP uses state-of-the-art 90 nanometer technology to implement an ARM926EJ-S CPU core with a Vector Floating Point (VFP) coprocessor and a large array of standard peripherals including USB On-The-Go with

The microcontroller operates at frequencies up to 208 MHz CPU. The ARM926EJ-S processor Core implements a 5-stage pipeline in a Harvard architecture with separate 32 kB instruction and data caches, and a Memory Management Unit (MMU) . The core uses the ARM v5Te instruction set that includes DSP instruction extensions with a single cycle MAC, and Jazelle Java bytecode execution hardware. A block diagram of the microcontroller is shown in Figure 1.

The LPC3180/01 incorporates an SDRAM interface, two NAND flash interfaces, USB 2.0 full-speed interface, seven UARTs, two I^{2}C-bus interfaces, two SPI ports, a Secure Digital (SD) interface, and a 10-bit ADC in addition to many other features.

2. Features

2.1 Key features

- ARM926EJ-S processor with 32 kB instruction cache and 32 kB data cache, running at up to 208 MHz.
- 64 kB of SRAM.
- High-performance multi-layer AHB bus system provides a separate bus for CPU data and instruction fetch, two data buses for the DMA controller, and another for the USB controller.
- External memory interfaces: one supports DDR and SDR SDRAM, another supports single-level and multi-level NAND flash devices and can serve as an 8-bit parallel interface.
- General purpose DMA controller that can be used with the SD card and SPI interfaces, as well as for memory-to-memory transfers.
- USB 2.0 full-speed device, host (OHCI compliant), and OTG block. A dedicated PLL provides the 48 MHz USB clock.
- Multiple serial interfaces, including seven UARTs, two SPI controllers, and two master, multi-master, or slave I^{2}C-bus interfaces.
- SD memory card interface.
- Up to 55 GPI, GPO, and GPIO pins. Includes 12 GPI pins, 24 GPO pins, and six GPIO pins.

founded by Philips

- 10-bit ADC with input multiplexing from three pins.
- Real-Time Clock (RTC) with separate power supply and power domain, clocked by a dedicated 32 kHz oscillator. Includes a 128 byte scratch pad memory. The RTC may remain active when the rest of the chip is not powered.
- 32-bit general purpose high-speed timer with 16-bit pre-scaler with capture and compare capability.
- 32-bit millisecond timer driven from the RTC clock. Interrupts may be generated using two match registers.
- Watchdog timer.
- Two PWM blocks with an output rate up to 50 kHz.
- Keyboard scanner function provides automatic scanning of up to an 8 × 8 key matrix.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace buffer with 2 k × 24-bit RAM allows trace via JTAG.
- On-chip crystal oscillator.
- Stop mode saves power, while allowing many peripheral functions to restart CPU activity.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal.
- Boundary scan for simplified board testing.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC3180FEL320/01[1]	LFBGA320	plastic low profile fine-pitch ball grid array package; 320 balls; body 13 × 13 × 0.9 mm	SOT824-1

[1] F = –40 °C to +85 °C temperature range.

4. Block diagram

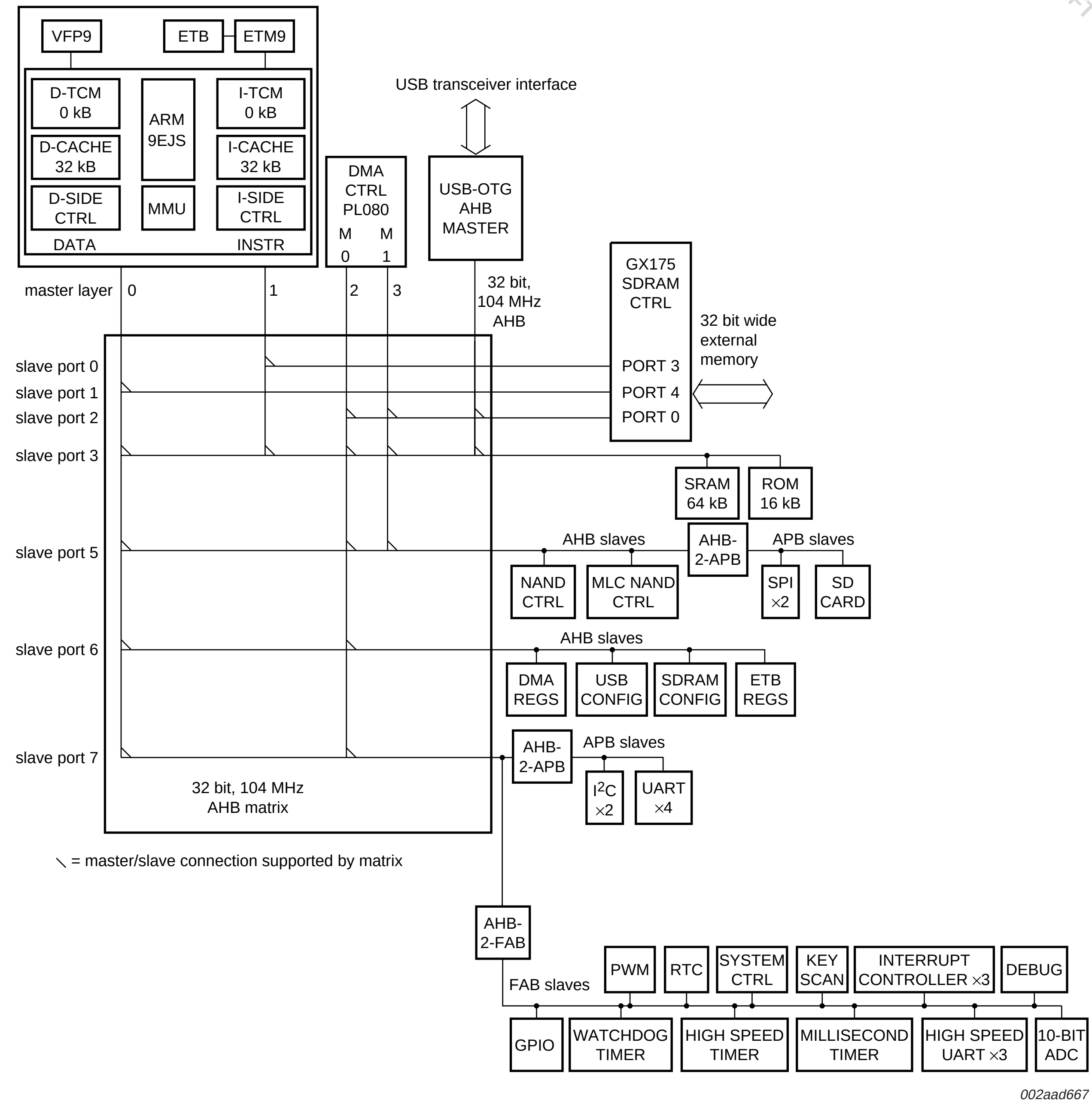


Fig 1. LPC3180/01 block diagram

5. Pinning information

5.1 Pinning

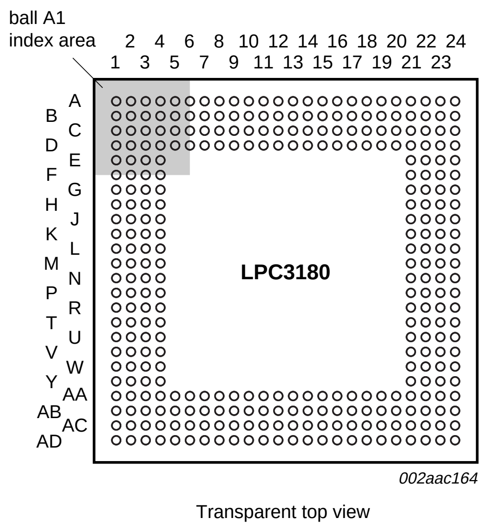


Fig 2. LPC3180/01 package

Table 2. LPC3180/01 Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	U6_IRRX/ PIO_INP[21]	2	U5_RX/PIO_INP[20]	3	HIGHCORE	4	JTAG1_TDO
5	JTAG1_TMS	6	JTAG1_RTCK	7	U3_TX	8	n.c.[1]
9	n.c.[1]	10	VSS_IOA	11	GPO_23/U2_HRTS	12	GPI_05
13	RTCX_OUT	14	RTCX_IN	15	n.c.[1]	16	n.c.[1]
17	n.c.[1]	18	n.c.[1]	19	n.c.[1]	20	n.c.[1]
21	n.c.[1]	22	VDD_PLLHCLK_12	23	SYSX_IN	24	n.c.[1]
Row B							
1	KEY_COL5	2	U7_HCTS/ PIO_INP[22]	3	U7_TX	4	VDD_IOA
5	JTAG1_TCK	6	JTAG1_TDI	7	VDD_IOA	8	U2_HCTS/ PIO_INP[16]
9	U1_RX/PIO_INP[15]	10	U1_TX	11	n.c.[1]	12	GPO_17
13	VSS_RTCCORE	14	VDD12	15	n.c.[1]	16	n.c.[1]
17	n.c.[1]	18	n.c.[1]	19	n.c.[1]	20	VSS_PLLUSB
21	VSS_OSC	22	VDD_PLLUSB_12	23	SYSX_OUT	24	n.c.[1]
Row C							
1	KEY_COL2	2	KEY_COL3	3	U7_RX/PIO_INP[23]	4	U5_TX
5	SYSCLKEN	6	U3_RX/PIO_INP[18]	7	U2_RX/PIO_INP[17]	8	n.c.[1]
9	n.c.[1]	10	VDD_COREFXD12_01	11	VDD_RTCCORE12	12	VDD_RTC12

Table 2. LPC3180/01 Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
13	VSS_RTCOSC	14	VDD_RTCOSC12	15	n.c.[1]	16	n.c.[1]
17	n.c.[1]	18	n.c.[1]	19	VSS_RAM[1]	20	VSS_CORE_01
21	PLL397_LOOP	22	VDD_PLL397_12	23	VSS_PLL397	24	ADIN0
Row D							
1	KEY_ROW4	2	KEY_COL0	3	TEST	4	VSS_IOD
5	U6_IRTX	6	VDD_CORE12_02	7	JTAG1_NTRST	8	VSS_CORE_02
9	U2_TX	10	GPI_11	11	n.c.[1]	12	ONSW
13	RESET_N	14	n.c.[1]	15	n.c.[1]	16	VSS_CORE_03
17	n.c.[1]	18	VDD_COREFXD12_02	19	VSS_PLLHCLK	20	VDD_OSC12
21	n.c.[1]	22	VSS_AD	23	ADIN2	24	VDD_AD28
Row E							
1	KEY_ROW2	2	KEY_ROW5	3	VSS_IOD	4	KEY_COL4
21	VDD_AD28	22	ADIN1	23	RAM_D[30]/ PIO_SD[11]	24	RAM_D[31]/ PIO_SD[12]
Row F							
1	VSS_IOD	2	KEY_ROW1	3	KEY_ROW3	4	KEY_COL1
21	RAM_D[29]/ PIO_SD[10]	22	VDD_RAM	23	VSS_RAM	24	RAM_D[28]/ PIO_SD[09]
Row G							
1	n.c.[1]	2	n.c.[1]	3	KEY_ROW0	4	VDD_IOD
21	VDD_RAM	22	VSS_RAM	23	RAM_D[24]/ PIO_SD[05]	24	RAM_D[27]/ PIO_SD[08]
Row H							
1	GPI_00	2	n.c.[1]	3	PWM_OUT2	4	n.c.[1]
21	RAM_D[19]/ PIO_SD[00]	22	RAM_D[23]/ PIO_SD[04]	23	RAM_D[26]/ PIO_SD[07]	24	RAM_D[21]/ PIO_SD[02]
Row J							
1	GPI_07	2	PWM_OUT1	3	GPI_02	4	VSS_CORE_04
21	RAM_D[25]/ PIO_SD[06]	22	VDD_RAM	23	VSS_RAM	24	RAM_D[20]/ PIO_SD[01]
Row K							
1	GPI_10/U4_RX	2	GPI_08/KEY_COL6/ SPI2_BUSY	3	GPI_01/SERVICE_N	4	GPI_04/SPI1_BUSY
21	VDD_CORE12_03	22	VDD_RAM	23	RAM_D[22]/ PIO_SD[03]	24	RAM_D[18]/ DDR_NCLK
Row L							
1	GPO_03	2	GPI_09/KEY_COL7	3	VDD_CORE12_05	4	GPO_02
21	RAM_D[17]/ DDR_DQS1	22	RAM_D[13]	23	RAM_D[16]/ DDR_DQS0	24	RAM_D[15]
Row M							
1	GPO_08	2	GPO_10	3	GPO_07	4	GPO_06
21	VSS_RAM	22	RAM_D[10]	23	RAM_D[14]	24	RAM_D[12]
Row N							

Table 2. LPC3180/01 Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	GPO_13	2	GPO_16	3	VSS_IOD	4	GPO_09
21	RAM_D[07]	22	VSS_RAM	23	RAM_D[11]	24	RAM_D[09]
Row P							
1	GPO_18	2	GPO_22/U7_HRTS	3	GPO_12	4	GPO_21/U4_TX
21	RAM_D[04]	22	VDD_RAM	23	RAM_D[08]	24	RAM_D[06]
Row R							
1	GPIO_01	2	GPIO_05	3	VSS_CORE_05	4	GPO_15
21	VSS_CORE_06	22	VSS_RAM	23	RAM_D[05]	24	RAM_D[03]
Row T							
1	GPIO_03/ KEY_ROW7	2	GPIO_04	3	GPIO_00	4	SPI2_DATIN
21	RAM_CLKIN	22	RAM_D[01]	23	RAM_D[00]	24	RAM_D[02]
Row U							
1	n.c.[1]	2	MS_DIO1	3	GPIO_02/ KEY_ROW6	4	VDD_IOD
21	RAM_RAS_N	22	VDD_RAM	23	RAM_CLK	24	RAM_CKE
Row V							
1	SPI1_DATIN	2	SPI2_DATIO	3	SPI2_CLK	4	MS_DIO3
21	RAM_DQM[2]	22	RAM_WR_N	23	RAM_CAS_N	24	RAM_CS_N
Row W							
1	SPI1_DATIO	2	MS_DIO0	3	SPI1_CLK	4	n.c.[1]
21	RAM_A[14]	22	VSS_RAM	23	RAM_DQM[1]	24	RAM_DQM[3]
Row Y							
1	MS_BS	2	MS_DIO2	3	GPO_04	4	I2C1_SCL
21	VDD_RAM	22	RAM_A[10]	23	RAM_A[12]	24	RAM_DQM[0]
Row AA							
1	MS_SCLK	2	VDD_CORE12_01	3	GPI_06/ HSTIM_CAP	4	VDD_IOB
5	VSS_CORE_07	6	n.c.[1]	7	USB_ATX_INT_N	8	USB_DAT_VP/ U5_RX
9	I2C2_SDA	10	VSS_CORE_08	11	GPI_03	12	VDD_CORE12_06
13	n.c.[1]	14	n.c.[1]	15	VDD_IOC	16	FLASH_ALE
17	FLASH_RD_N	18	n.c.[1]	19	VDD_IOC	20	VDD_RAM
21	RAM_A[05]	22	VSS_RAM	23	RAM_A[09]	24	RAM_A[13]
Row AB							
1	GPO_11	2	n.c.[1]	3	TST_CLK2	4	n.c.[1]
5	VSS_IOB	6	VDD_CORE12_07	7	USB_SE0_VM/ U5_TX	8	VSS_IOC
9	GPO_00/TST_CLK1	10	GPO_05	11	VDD_IOC	12	RESOUT_N
13	n.c.[1]	14	n.c.[1]	15	n.c.[1]	16	n.c.[1]
17	VSS_CORE_09	18	VDD_CORE12_08	19	FLASH_IO[04]	20	RAM_A[01]
21	VSS_RAM	22	RAM_A[07]	23	RAM_A[08]	24	RAM_A[11]

Table 2. LPC3180/01 Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row AC							
1	I2C1_SDA	2	VSS	3	VSS	4	VSS
5	n.c.[1]	6	n.c.[1]	7	VDD_IOC	8	USB_I2C_SCL
9	GPO_01	10	GPO_19	11	n.c.[1]	12	n.c.[1]
13	n.c.[1]	14	n.c.[1]	15	FLASH_CLE	16	VSS_IOC
17	FLASH_IO[06]	18	FLASH_RDY	19	FLASH_IO[02]	20	FLASH_IO[03]
21	FLASH_CE_N	22	RAM_A[04]	23	RAM_A[06]	24	VDD_RAM
Row AD							
1	n.c.[1]	2	n.c.[1]	3	n.c.[1]	4	n.c.[1]
5	n.c.[1]	6	USB_OE_TP_N	7	USB_I2C_SDA	8	I2C2_SCL
9	GPO_14	10	GPO_20	11	VSS_RAM	12	n.c.[1]
13	n.c.[1]	14	n.c.[1]	15	VSS_IOC	16	n.c.[1]
17	FLASH_WR_N	18	FLASH_IO[07]	19	FLASH_IO[05]	20	FLASH_IO[01]
21	FLASH_IO[00]	22	RAM_A[00]	23	RAM_A[02]	24	RAM_A[03]

[1] n.c. = not connected.

5.2 Pin description

Table 3. LPC 3180/01 Pin description

Symbol	Pin	Type	Description
ADIN0	C24	I	input 0 to the ADC
ADIN1	E22	I	input 1 to the ADC
ADIN2	D23	I	input 2 to the ADC
FLASH_ALE	AA16	O	address latch enable for NAND flash
FLASH_CE_N	AC21	O	chip enable for NAND flash
FLASH_CLE	AC15	O	command latch enable for NAND flash
FLASH_IO[07:00]	AD18, AC17, AD19, AB19, AC20, AC19, AD20, AD21	I/O	NAND flash data bus
FLASH_RD_N	AA17	O	read strobe for NAND flash
FLASH_RDY	AC18	I	ready status from NAND flash
FLASH_WR_N	AD17	O	write strobe for NAND flash
GPI_00	H1	I	general purpose input 00
GPI_01/SERVICE_N	K3	I	**GPI_01 —** general purpose input 01
		I	**SERVICE_N —** boot select input
GPI_02	J3	I	general purpose input 02
GPI_03	AA11	I	general purpose input 03
GPI_04/SPI1_BUSY	K4	I	**GPI_04 —** general purpose input 04
		I	**SPI1_BUSY —** busy input for SPI1
GPI_05	A12	I	general purpose input 05
GPI_06/HSTIM_CAP	AA3	I	**GPI_06 —** general purpose input 06
		I	**HSTIM_CAP —** capture input trigger for the high-speed timer

Table 3. LPC 3180/01 Pin description *...continued*

Symbol	Pin	Type	Description
GPI_07	J1	I	general purpose input 07
GPI_08/KEY_COL6/ SPI2_BUSY	K2	I	**GPI_08 —** general purpose input 08
		I	**KEY_COL6 —** keyboard scan column input 6
		I	**SPI2_BUSY —** busy input for SPI2
GPI_09/KEY_COL7	L2	I	**GPI_09 —** general purpose input 09
		I	**KEY_COL7 —** keyboard scan column input 7
GPI_10/U4_RX	K1	I	**GPI_10 —** general purpose input 10
		I	**U4_RX —** UART 4 receive data input
GPI_11	D10	I	general purpose input 11
GPIO_00	T3	I/O	general purpose input/output 00
GPIO_01	R1	I/O	general purpose input/output 01
GPIO_02/KEY_ROW6	U3	I/O	**GPIO_02 —** general purpose input/output 02
		O	**KEY_ROW6 —** keyboard scan row output 6
GPIO_03/KEY_ROW7	T1	I/O	**GPIO_03 —** general purpose input/output 03
		O	**KEY_ROW7 —** keyboard scan row output 7
GPIO_04	T2	I/O	general purpose input/output 04
GPIO_05	R2	I/O	general purpose input/output 05
GPO_00/ TST_CLK1	AB9	O	**GPO_00 —** general purpose output 00
		O	**TST_CLK1 —** Clock test output 1, controlled by the TEST_CLK register
GPO_01	AC9	O	general purpose output 01
GPO_02	L4	O	general purpose output 02
GPO_03	L1	O	general purpose output 03
GPO_04	Y3	O	general purpose output 04
GPO_05	AB10	O	general purpose output 05
GPO_06	M4	O	general purpose output 06
GPO_07	M3	O	general purpose output 07
GPO_08	M1	O	general purpose output 08
GPO_09	N4	O	general purpose output 09
GPO_10	M2	O	general purpose output 10
GPO_11	AB1	O	general purpose output 11
GPO_12	P3	O	general purpose output 12
GPO_13	N1	O	general purpose output 13
GPO_14	AD9	O	general purpose output 14
GPO_15	R4	O	general purpose output 15
GPO_16	N2	O	general purpose output 16
GPO_17	B12	O	general purpose output 17
GPO_18	P1	O	general purpose output 18
GPO_19	AC10	O	general purpose output 19
GPO_20	AD10	O	general purpose output 20

Table 3. LPC 3180/01 Pin description *...continued*

Symbol	Pin	Type	Description
GPO_21/U4_TX	P4	O	**GPO_21 —** general purpose output 21
		O	**U4_TX —** UART 4 transmit data output
GPO_22/U7_HRTS	P2	O	**GPO_22 —** general purpose output 22
		O	**U7_HRTS —** UART 7 hardware flow control (RTS) output
GPO_23/U2_HRTS	A11	O	**GPO_23 —** general purpose output 23
		O	**U2_HRTS —** UART 2 hardware flow control (RTS) output
HIGHCORE	A3	O	core voltage select output
I2C1_SCL	Y4	I/O	serial clock for I^2C1
I2C1_SDA	AC1	I/O	serial data for I^2C1
I2C2_SCL	AD8	I/O	serial clock for I^2C2
I2C2_SDA	AA9	I/O	serial data for I^2C2
JTAG1_NTRST	D7	I	JTAG reset input
JTAG1_RTCK	A6	O	JTAG return clock output
JTAG1_TCK	B5	I	JTAG clock input
JTAG1_TDI	B6	I	JTAG data input
JTAG1_TDO	A4	O	JTAG data output
JTAG1_TMS	A5	I	JTAG test mode select input
KEY_COL0 to KEY_COL5	D2, F4, C1, C2, E4, B1	I	keyboard scan column inputs
KEY_ROW0 to KEY_ROW5	G3, F2, E1, F3, D1, E2	O	keyboard scan row outputs 0 through 5
MS_BS	Y1	I/O	SD card command input/output (SD_CMD)
MS_DIO0 to MS_DIO3	W2, U2, Y2, V4	I/O	SD card data bus (SD_D0 to SD_D3)
MS_SCLK	AA1	O	SD card clock output (SD_CLK)
ONSW	D12	O	VCCon output signal
PLL397_LOOP	C21	I/O	loop filter pin for PLL397; requires external components if PLL397 is used
PWM_OUT1	J2	O	output of Pulse Width Modulator 1
PWM_OUT2	H3	O	output of Pulse Width Modulator 2
RAM_A[14:00]	W21, AA24, Y23, AB24, Y22, AA23, AB23, AB22, AC23, AA21, AC22, AD24, AD23, AB20, AD22	O	SDRAM address bus, pins 14 to 00
RAM_CAS_N	V23	O	SDRAM column address strobe output
RAM_CKE	U24	O	SDRAM clock enable output
RAM_CLK	U23	O	SDRAM clock output
RAM_CLKIN	T21	I	SDRAM clock return input
RAM_CS_N	V24	O	SDRAM chip select output
RAM_D[15:00]	L24, M23, L22, M24, N23, M22, N24, P23, N21, P24, R23, P21, R24, T24, T22, T23	I/O	SDRAM data bus, pins 15 to 00

Table 3. LPC 3180/01 Pin description *...continued*

Symbol	Pin	Type	Description
RAM_D[16]/ DDR_DQS0	L23	I/O	**RAM_D[16] —** SDRAM data bus, pin 16
		O	**DDR_DQS0 —** SDRAM data strobe output for lower byte
RAM_D[17]/ DDR_DQS1	L21	I/O	**RAM_D[17] —** SDRAM data bus, pin 17
		O	**DDR_DQS1 —** SDRAM data strobe output for upper byte
RAM_D[18]/ DDR_NCLK	K24	I/O	**RAM_D[18] —** SDRAM data bus, pin 18
		O	**DDR_NCLK —** inverted SDRAM clock output for DDR
RAM_D[31:19]/ PIO_SD[12:00]	E24, E23, F21, F24, G24, H23, J21, G23, H22, K23, H24, J24, H21	I/O	**RAM_D[31:19] —** SDRAM data bus, pins 31 to 19
		I/O	**PIO_SD[12:00] —** general purpose input/output, pins 12 to 00; details may be found in Section 6.10
RAM_DQM[3:0]	W24, V21, W23, Y24	O	SDRAM byte write mask outputs
RAM_RAS_N	U21	O	SDRAM row address strobe output
RAM_WR_N	V22	O	SDRAM write strobe output
RESET_N	D13	I	system reset input
RESOUT_N	AB12	O	reset output signal
RTCX_IN	A14	I	RTC oscillator input
RTCX_OUT	A13	O	RTC oscillator output
SPI1_CLK	W3	O	clock output for SPI1
SPI1_DATIN	V1	I	data input for SPI1
SPI1_DATIO	W1	I/O	data input/output for SPI1
SPI2_CLK	V3	O	clock output for SPI2
SPI2_DATIN	T4	I	data input for SPI2
SPI2_DATIO	V2	I/O	data input/output for SPI2
SYSCLKEN	C5	I/O	system clock request
SYSX_IN	A23	I	main oscillator input
SYSX_OUT	B23	O	main oscillator output
TEST (DBGEN)	D3	I	test input; internally pulled down, should be left floating in an application
TST_CLK2	AB3	O	clock test output 2, controlled by the TEST_CLK
U1_RX/ PIO_INP[15]	B9	I	**U1_RX —** UART 1 receive data input
		I	**PIO_INP[15] —** general purpose input to PIO_INP_STATE register
U1_TX	B10	O	UART 1 transmit data output
U2_HCTS/ PIO_INP[16]	B8	I	**U2_HCTS —** UART 2 hardware flow control (CTS) input
		I	**PIO_INP[16] —** general purpose input to PIO_INP_STATE register
U2_RX/ PIO_INP[17]	C7	I	**U2_RX —** UART 2 receive data input
		I	**PIO_INP[17] —** general purpose input to PIO_INP_STATE register
U2_TX	D9	O	UART 2 transmit data output
U3_RX/ PIO_INP[18]	C6	I	**U3_RX —** UART 3 receive data input
		I	**PIO_INP[18] —** general purpose input to PIO_INP_STATE register
U3_TX	A7	O	UART 3 transmit data output
U5_RX/PIO_INP[20]	A2	I	**U5_RX —** UART 5 receive data input
		I	**PIO_INP[20] —** general purpose input to PIO_INP_STATE register

Table 3. LPC 3180/01 Pin description *...continued*

Symbol	Pin	Type	Description
U5_TX	C4	O	UART 5 transmit data output
U6_IRRX/ PIO_INP[21]	A1	I/O	**U6_IRRX —** UART 6 receive data input; can be IrDA data
		I	**PIO_INP[21] —** general purpose input to PIO_INP_STATE register
U6_IRTX	D5	O	UART 6 transmit data output; can be IrDA data
U7_HCTS/ PIO_INP[22]	B2	I	**U7_HCTS —** UART 7 hardware flow control (CTS) input
		I	**PIO_INP[22] —** general purpose input to PIO_INP_STATE register
U7_RX/ PIO_INP[23]	C3	I	**U7_RX —** UART 7 receive data input
		I	**PIO_INP[23] —** general purpose input to PIO_INP_STATE register
U7_TX	B3	O	UART 7 transmit data output
USB_ATX_INT_N	AA7	I	USB interrupt from external transceiver
USB_DAT_VP/ U5_RX	AA8	I/O	**USB_DAT_VP —** USB transmit data
		I	**U5_RX —** UART 5 receive data input
USB_I2C_SCL	AC8	I/O	serial clock for USB I^2C-bus
USB_I2C_SDA	AD7	I/O	serial data for USB I^2C-bus
USB_OE_TP_N	AD6	I/O	USB transmit enable for DAT/SE0
USB_SE0_VM/ U5_TX	AB7	I/O	**USB_SE0_VM —** USB single ended zero transmit
		O	**U5_TX —** UART 5 transmit data output
VDD12	B14	I	1.2 V power supply for various internal functional blocks that are not included with VDD_CORE or VDD_COREFXD
VDD_AD28	D24, E21	I	3.0 V power supply and positive reference voltage for the ADC
VDD_CORE12_01 to VDD_CORE12_03, VDD_CORE12_05 to VDD_CORE12_08	AA2, D6, K21, L3, AA12, AB6, AB18	I	1.2 V core main power supply for the CPU and other core logic; this voltage may be reduced to 0.9 V when the core is running at or below 13 MHz; the HIGHCORE pin may be used to signal this condition to an external voltage switch
VDD_COREFXD12_01, VDD_COREFXD12_02	C10, D18	I	1.2 V core secondary power supply voltage for the CPU and other core logic; this supply cannot be reduced in the same manner as the VDD_CORE12 supply
VDD_IOA	B7, B4	I	1.8 V or 3.0 V power supply for I/O pins that may operate from either a 1.8 V range or a 3 V range
VDD_IOB	AA4	I	1.8 V or 3.0 V power supply for I/O pins that may operate from either a 1.8 V range or a 3 V range
VDD_IOC	AA19, AA15, AB11, AC7	I	1.8 V or 3.0 V power supply for I/O pins that may operate from either a 1.8 V range or a 3 V range
VDD_IOD	U4, G4,	I	1.8 V or 3.0 V power supply for I/O pins that may operate from either a 1.8 V range or a 3 V range
VDD_OSC12	D20	I	1.2 V power supply for the main oscillator
VDD_PLL397_12	C22	I	1.2 V power supply for the 397x PLL
VDD_PLLHCLK_12	A22	I	1.2 V power supply for the HCLK PLL
VDD_PLLUSB_12	B22	I	1.2 V power supply for the USB PLL
VDD_RTC12	C12	I	1.2 V power supply for the RTC block
VDD_RTCCORE12	C11	I	1.2 V power supply for the RTC block
VDD_RTCOSC12	C14	I	1.2 V power supply for the 32 kHz RTC oscillator

Table 3. LPC 3180/01 Pin description *...continued*

Symbol	Pin	Type	Description
VDD_RAM	G21, F22, J22, K22, P22, U22, Y21, AC24, AA20	I	power supply for the SDRAM that may operate in either a 1.8 V range or a 2.8/3.0 V range
VSS	AC2, AC3, AC4	I	ground for various internal logic blocks that are not included with VDD_CORE or VDD_COREFXD.
VSS_AD	D22	I	ground for the ADC; this should nominally be the same voltage as VSS, but should be isolated to minimize noise and conversion error
VSS_CORE_01 to VSS_CORE_09	C20, D8, D16, J4, R3, R21, AA5, AA10, AB17	I	ground for the core logic functions
VSS_IOA	A10	I	ground for I/O pins that may operate from either a 1.8 V range or a 3 V range
VSS_IOB	AB5	I	ground for various internal logic blocks that are not included with VDD_CORE or VDD_COREFXD.
VSS_IOC	AC16, AD15, AB8	I	ground for I/O pins that may operate from either a 1.8 V range or a 3 V range
VSS_IOD	D4, E3, F1, N3	I	ground for I/O pins that may operate from either a 1.8 V range or a 3 V range
VSS_OSC	B21	I	ground for the main oscillator
VSS_PLL397	C23	I	ground for the 397x PLL
VSS_PLLHCLK	D19	I	ground for the HCLK PLL
VSS_PLLUSB	B20	I	ground for the USB PLL
VSS_RTCCORE	B13	I	ground for the RTC block
VSS_RTCOSC	C13	I	ground for the 32 kHz RTC oscillator
VSS_RAM	AD11, C19, F23, G22, J23, M21, N22, R22, W22, AA22, AB21	I	ground for the SDRAM controller block
VSS_RAM		I	
n.c.	A8, A9, A15, A16, A17, A18, A19, A20, A21, A24, B11, B17, B18, B15, B16, B19, B24, C9, C8, C15, C16, C17, C18, D11, D14, D15, D17, D21, G1, G2, H2, H4, U1, W4, AA6, AA13, AA14, AA18, AB2, AB4, AB13, AB14, AB15, AB16, AC5, AC6, AC11, AC12, AC13, AC14, AD1, AD2, AD3, AD4, AD5, AD12, AD13, AD14, AD16,		not connected;

6. Functional description

6.1 Architectural overview

The microcontroller is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISCs. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

A 5-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. At any one point in time, several operations are typically in progress: subsequent instruction fetch, next instruction decode, instruction execution, memory access, and write-back. The combination of architectural enhancements gives the ARM9 about 30 % better performance than an ARM7 running at the same clock rate:

- Approximately 1.3 clocks per instruction (1.9 clocks per instruction for ARM7).
- Approximately 1.1 Dhrystone MIPS/MHz (0.9 Dhrystone MIPS/MHz for ARM7).

The ARM926EJ-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM926EJ-S processor has two instruction sets:

1. The standard 32-bit ARM set.
2. A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

In addition, the ARM9 includes enhanced DSP instructions and multiplier, as well as an enhanced 32-bit MAC block.

6.2 Vector Floating Point (VFP) coprocessor

This CPU coprocessor provides full support for single-precision and double-precision add, subtract, multiply, divide, and multiply-accumulate operations at CPU clock speeds. It is compliant with the IEEE 754 standard, and enables advanced Motor control and DSP applications. The VFP has three separate pipelines for floating-point MAC operations, divide or square root operations, and load/store operations. These pipelines can operate in parallel and can complete execution out of order. All single-precision instructions, except divide and square root, take one cycle and double-precision multiply and multiply-accumulate instructions take two cycles. The VFP also provides format conversions between floating-point and integer word formats.

6.3 AHB matrix

The microcontroller has a multi-layer AHB matrix for inter-block communication. AHB is the ARM high-speed bus, which is part of the ARM bus architecture. AHB is a high-bandwidth low-latency bus that supports multi-master arbitration and a bus grant/request mechanism. For systems where there is only one bus master (the CPU), or where there are two masters (CPU and DMA) and the CPU does not generally need to contend with the DMA for program memory access (because the CPU has access to memory on its local bus or has caches or another AHB bus etc.), this arrangement works well. However, if there are multiple bus masters and the CPU needs access to external memory, a single AHB bus can cause a bottleneck. ARM's solution to this was to invent a multi-layer AHB which replaces the request/grant and arbitration mechanism with a multiplexer fabric that pushes arbitration to the level of the devices. Thus, if a CPU and a DMA controller want access to the same memory, the multi-layer fabric will arbitrate between the two on granting access to that memory. This allows simultaneous access by bus masters to different resources at the cost of increased arbitration complexity. As with all trade-offs, the pros and cons must be analyzed, for a microcontroller operating at 200 MHz, removing guaranteed central arbitration in case more than one bus master is active in favor of occasional local arbitration gives better performance.

The blocks outside the CPU can be roughly split into memory controllers, serial communication, I/O, timers/counters and RTC, system control, and debug and trace blocks. These are described as follows.

6.4 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8/16/32 bit. The LPC3180/01 provides 64 kB of SRAM.

6.5 Memory map

The LPC3180/01 memory map incorporates several distinct regions, as shown in Figure 3. When an application is running, the CPU interrupt vectors are re-mapped to allow them to reside in on-chip SRAM.

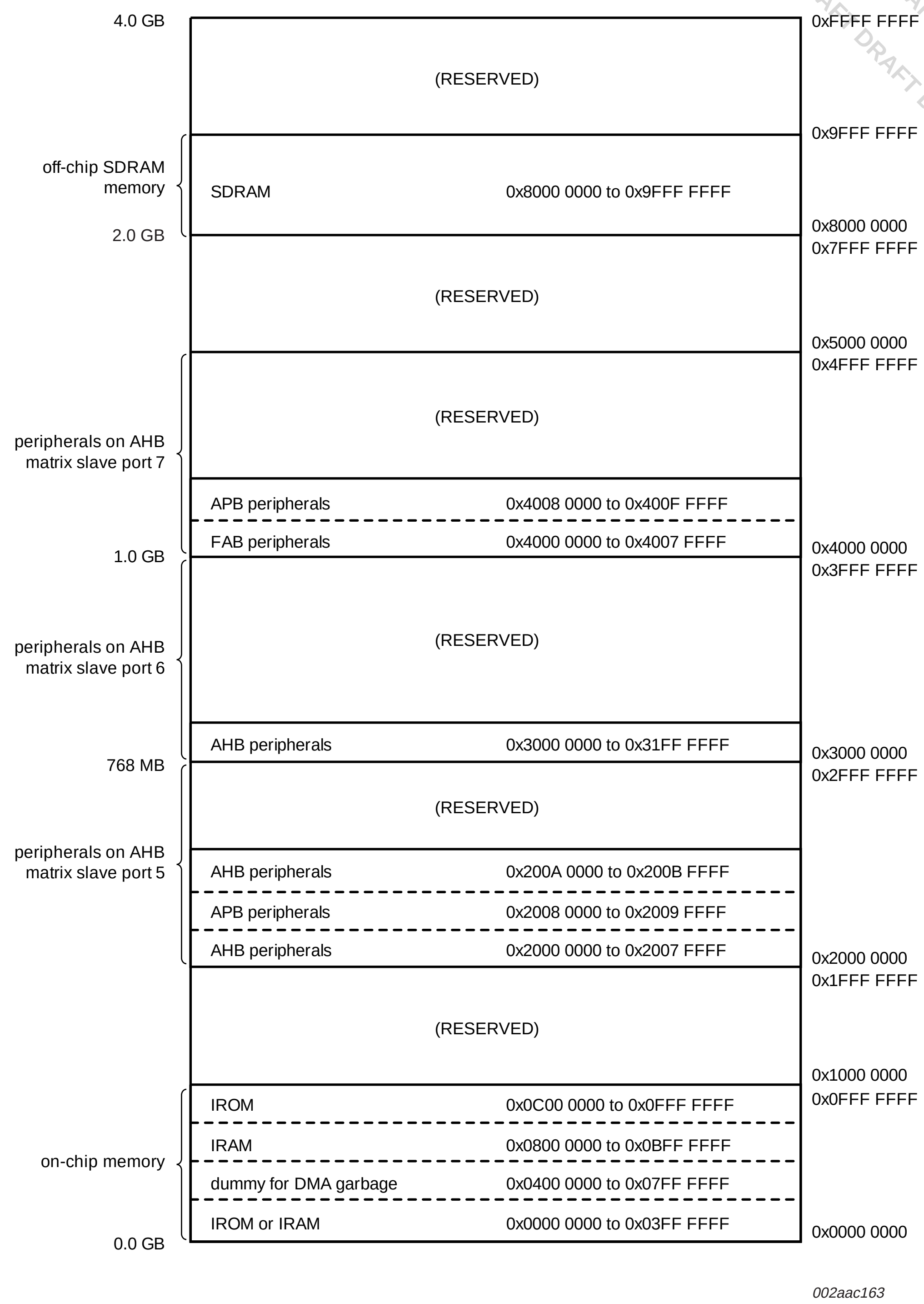


Fig 3. LPC3180/01 memory map

6.6 SDRAM memory controller

The SDRAM memory controller provides an interface between the system bus and external (off-chip) memory devices. A single chip select is supplied, supporting one group of SDRAM in the same address range. The SDRAM controller supports SDR SDRAM

devices of 64/128/256/512 Mbit in size, as well as DDR SDRAM devices of 64/128/256/512 Mbit in size. The SDRAM controller uses four data ports to allow simultaneous requests from multiple on-chip AHB bus masters.

6.7 NAND flash controllers

The LPC3180/01 includes two NAND flash controllers, one for multi-level NAND flash devices and one for single-level NAND flash devices. The two NAND flash controllers use the same pins to interface to external NAND flash devices, so only one interface is active at a time.

6.7.1 Multi-Level Cell (MLC) NAND flash controller

The MLC NAND flash controller interfaces to either multi-level or single-level NAND flash devices. An external NAND flash device is used to allow the bootloader to automatically load a portion of the application code into internal SRAM for execution following reset.

The MLC NAND flash controller supports up to 2 Gbit devices with small (528 byte) or large (2114 byte) pages. Programmable NAND timing parameters allow support for a variety of NAND flash devices. A built-in Reed-Solomon encoder/decoder provides error detection and correction capability. A 528 byte data buffer reduces the need for CPU supervision during loading. The MLC NAND flash controller also provides DMA support.

6.7.2 Single-Level Cell (SLC) NAND flash controller

The SLC NAND flash controller interfaces to single-level NAND flash devices up to 2 Gbit in size. DMA page transfers are supported, including a 20 byte DMA read and write FIFO. Hardware support for ECC (Error Checking and Correction) is included for the main data area. Software can correct a single bit error.

6.8 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the same AHB master or one area by each master.

The DMA controls eight DMA channels with hardware prioritization. The DMA controller interfaces to the system via two AHB bus masters, each with a full 32-bit data bus width. DMA operations may be set up for 8-bit, 16-bit, and 32-bit data widths, and can be either big-endian or little-endian. Incrementing or non-incrementing addressing for source and destination are supported, as well as programmable DMA burst size. Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.

6.9 Interrupt controller

The interrupt controller is comprised of three basic interrupt controller blocks, supporting a total of 59 interrupt sources. Each interrupt source can be individually enabled/disabled and configured for high or low level triggering, or rising or falling edge triggering. Each interrupt may also be steered to either the FIQ or IRQ input of the ARM9. Raw interrupt

status and masked interrupt status registers allow versatile condition evaluation. In addition to peripheral functions, each of the six general purpose input/output pins and 11 general purpose input pins are connected directly to the interrupt controller.

6.10 General purpose parallel I/O

Some device pins that are not dedicated to a specific peripheral function have been designed to be general purpose inputs, outputs, or I/Os. Also, some pins may be configured either as a specific peripheral function or a general purpose input, output, or I/O. A total of 55 pins can potentially be used as general purpose input/outputs, general purpose outputs, and general purpose inputs.

GPIO pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of GPIO and GPO outputs controlled by that register simultaneously. The value of the output register for standard GPIOs and GPO pins may be read back, as well as the current actual state of the port pins.

There are 12 GPI, 24 GPO, and six GPIO pins. When the SDRAM bus is configured for 16 data bits, 13 of the remaining SDRAM data pins may be used as GPIOs.

6.10.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- A single register selects direction for pins that support both input and output modes.
- Direction control of individual bits.
- For input/output pins, both the programmed output state and the actual pin state can be read.
- There are a total of 12 general purpose inputs, 24 general purpose outputs, and six general purpose input/outputs.
- Additionally, 13 SDRAM data lines may be used as GPIOs if a 16-bit SDRAM interface is used (rather than a 32-bit interface).

6.11 10-bit ADC

The ADC is a three channel, 10-bit successive approximation ADC. The ADC may be configured to produce results with a resolution anywhere from 10 bits to 3 bits. When high resolution is not needed, lowering the resolution can substantially reduce conversion time.

The analog portion of the ADC has its own power supply to enhance the low noise characteristics of the converter. This voltage is only supplied internally when the core has voltage. However, the ADC block is not affected by any difference in ramp-up time for VDD_AD and VDD_CORE voltage supplies.

6.11.1 Features

- Measurement range of 0 V to VDD_AD28 (nominally 3 V).
- Low noise ADC.
- Maximum 10-bit resolution, resolution can be reduced to any amount down to 3 bits for faster conversion.
- Three input channels.

- Uses 32 kHz RTC clock

6.12 USB interface

The LPC3180/01 supports USB in either device, host, or OTG configuration.

6.12.1 USB device controller

The USB device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. The DMA controller when enabled transfers data between the endpoint buffer and the USB RAM.

6.12.1.1 Features

- Fully compliant with USB 2.0 full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints.
- One duplex DMA channel serves all endpoints.
- Allows dynamic switching between CPU controlled and DMA modes.
- Double buffer implementation for bulk and isochronous endpoints.

6.12.2 USB host controller

The host controller enables data exchange with various USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies to the OHCI specification.

6.12.2.1 Features

- OHCI compliant.
- OHCI specifies the operation and interface of the USB host controller and SW driver.
- The host controller has four USB states visible to the SW driver:
  - USBOperational: Process lists and generate SOF tokens.
  - USBReset: Forces reset signaling on the bus, SOF disabled.
  - USBSuspend: Monitor USB for wake-up activity.
  - USBResume: Forces resume signaling on the bus.
- HCCA register points to interrupt and isochronous descriptors list.
- ControlHeadED and BulkHeadED registers point to control and bulk descriptors list.

6.12.3 USB OTG Controller

USB OTG (On-The-Go) is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

6.12.3.1 Features

- Fully compliant with On-The-Go supplement to the USB Specification 2.0 Revision 1.0.
- Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices under software control. HNP is partially implemented in hardware.
- Provides programmable timers required for HNP and SRP.
- Supports slave mode operation through AHB slave interface.
- Supports the OTG ATX from NXP (ISP 1301) or any external CEA-2011OTG specification compliant ATX.

6.13 UARTs

The LPC3180/01 contains seven UARTs. Four are standard UARTs, and three are special purpose high-speed UARTs.

6.13.1 Standard UARTs

The four standard UARTs are downwards compatible with the INS16Cx50. These UARTs support rates up to 460800 bit/s from a 13 MHz peripheral clock.

6.13.1.1 Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16 B, 32 B, 48 B, and 60 B.
- Transmitter FIFO trigger points at 0 B, 4 B, 8 B, and 16 B.
- Register locations conform to 16C550 industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800) bit/s.
- Each UART includes an internal loopback mode.

6.13.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bit/s from a 13 MHz peripheral clock, for on-board communication in low noise conditions. This is accomplished by changing the oversampling from 16× to 14×, and altering the rate generation logic.

6.13.2.1 Features

- Each high-speed UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, 16 B, 32 B, and 48 B.
- Transmitter FIFO trigger points at 0 B, 4 B, and 8 B.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600) bit/s.
- Each UART includes an internal loopback mode.

6.14 I^{2}C-bus serial I/O controller

The I^{2}C serial bus controller in the LPC3180/01 includes multimaster and slave support. A short description of the interface is described in the next paragraph.

There are two I^{2}C-bus interfaces in the LPC3180/01. The I^{2}C blocks are standard I^{2}C-bus compliant interfaces and can be configured as a master, multimaster or slave supporting the 400 kHz I^{2}C-bus mode and lower rates. The I^{2}C blocks also support 7 or 10 bit addressing. Each has a four word FIFO for both transmit and receive. An interrupt signal is available from each block.

There is a separate slave transmit FIFO. The slave transmit FIFO (TXS) and its level are only available when the controller is configured as a Master/Slave device and is operating in a multi-master environment. Separate TX FIFOs are needed in a multi-master because a controller might have a message queued for transmission when an external master addresses it to be come a slave-transmitter, a second source of data is needed.

6.14.1 Features

- Programmable clock to allow adjustment of I^{2}C-bus transfer rates.
- Bidirectional data transfer.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

6.15 SPI serial I/O controller

The LPC3180/01 has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master. The SPI implementation on the LPC3180/01 does not support operation as a slave.

6.15.1 Features

- Supports slaves compatible with SPI modes 0 to 3.
- Half duplex synchronous transfers.

- DMA support for data transmit and receive.
- 1-bit to 16-bit word length.
- Choice of LSB or MSB first data transmission.
- 64×16-bit input or output FIFO.
- Bit rates up to 52 Mbit/s.
- Busy input function.
- DMA time out interrupt to allow detection of end of reception when using DMA.
- Timed interrupt to facilitate emptying the FIFO at the end of a transmission.
- SPI clock and data pins may be used as general purpose pins if the SPI is not used.

6.16 SD card controller

The SD interface allows access to external SD memory cards. The SD card interface conforms to the SD Memory Card Specification Version 1.01.

6.16.1 Features

- Conformance to the SD Memory Card Specification Version 1.01.
- DMA is supported through the system DMA controller.
- Provides all functions specific to the SD memory card. These include the clock generation unit, power management control, command and data transfer.

6.17 Keyboard scan

The keyboard scan function can automatically scan a keyboard of up to 64 keys in an 8×8 matrix. In operation, the keyboard scanner's internal state machine will normally be in an idle state, with all KEY_ROW[n] pins set high, waiting for a change in the column inputs to indicate that one or more keys have been pressed.

When a keypress is detected, the matrix is scanned by setting one output pin high at a time and reading the column inputs. After de-bouncing, the keypad state is stored and an interrupt is generated. The keypad is then continuously scanned waiting for 'extra key pressed' or 'key released'. Any new keypad state is scanned and stored into the matrix registers followed by a new interrupt request to the interrupt controller. It is possible to detect and separate up to 64 multiple keys pressed.

6.17.1 Features

- Supports up to 64 keys in 8×8 matrix.
- Programmable debounce period.
- A key press can wake up the CPU from Stop mode.

6.18 High-speed timer

The high-speed timer block is clocked by the main peripheral clock. The clock is first divided down in a 16-bit programmable prescale counter which clocks a 32-bit Timer/Counter.

The high-speed timer includes three match registers that are compared to the Timer/Counter value. A match can generate an interrupt and cause the Timer/Counter to either continue to run, stop, or be reset. The high-speed timer also includes two capture registers that can take a snapshot of the Timer/Counter value when an input signal transitions. A capture event may also generate an interrupt.

6.18.1 Features

- 32-bit Timer/Counter with programmable 16-bit prescaler.
- Counter or Timer operation.
- Two 32-bit capture registers.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

6.19 Millisecond timer

The millisecond timer is clocked by 32 kHz RTC clock, so a prescaler is not needed to obtain a lower count rate.

The millisecond timer includes three match registers that are compared to the Timer/Counter value. A match can generate an interrupt and the cause the Timer/Counter either continue to run, stop, or be reset.

6.19.1 Features

- 32-bit Timer/Counter, running from the 32 kHz RTC clock.
- Counter or Timer operation.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

6.20 Watchdog timer

The watchdog timer block is clocked by the main peripheral clock, which clocks a 32-bit counter. A match register is compared to the Timer. When configured for watchdog functionality, a match drives the match output low. The match output is gated with an enable signal that can generate two different reset signals: one that resets the chip internally, and another that goes through a programmable pulse generator before it goes to the external pin RESOUT_N and to the internal chip reset.

6.20.1 Features

- Programmable 32-bit timer.
- Internally resets the device if not periodically reloaded.

- Flag to indicate that a watchdog reset has occurred.
- Programmable watchdog pulse output on RESOUT_N pin.
- Can be used as a standard timer if watchdog is not used.
- Pause control to stop counting when core is in debug state.

6.21 Real-Time Clock (RTC) and battery RAM

The RTC runs at 32768 Hz using a very low power oscillator. The RTC counts seconds and can generate alarm interrupts that can wake up the device from Stop mode. The RTCCLK can also clock the 397x PLL, the Millisecond Timer, the ADC, the Keyboard Scanner and the PWMs. The RTC up-counter value represents a number of seconds elapsed since second 0, which is an application determined time. The RTC counter will reach maximum value after about 136 years. The RTC down-counter is initiated with all 1's.

Two 32-bit Match registers are readable and writable by the processor. A match will result in an interrupt provided that the interrupt is enabled. The ONSW output pin can also be triggered by a match event, and cause an external power supply to turn on all of the operating voltages, as a way to startup after power has been removed.

The RTC block is implemented in a separate voltage domain. The block is supplied via a separate supply pin from a battery or other power source.

The RTC block also contains 32 words (128 B) of very low voltage SRAM. This SRAM is able to hold its contents down to the minimum RTC operating voltage.

6.21.1 Features

- Measures the passage of time in seconds.
- 32-bit up and down seconds counters.
- Ultra low power design to support battery powered systems.
- Dedicated 32 kHz oscillator.
- An output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC.
- Two 32-bit match registers with interrupt option.
- 32 words (128 B) of very low voltage SRAM.
- The RTC and battery RAM power have an independent power domain and dedicated supply pins, which can be powered from a battery or power supply.

6.22 Pulse width modulators

The LPC3180/01 provides two PWMs. They are clocked separately by either the main peripheral clock or the 32 kHz RTC clock. Both PWMs have a duty cycle programmable in 255 steps.

6.22.1 Features

- Clocked by the main peripheral clock or the 32 kHz RTC clock.
- Programmable 4-bit prescaler.
- Duty cycle programmable in 255 steps.

- Output frequency up to 50 kHz when using a 13 MHz peripheral clock.

6.23 Reset

Reset is accomplished by an active low signal on the RESET_N input pin. A reset pulse with a minimum width of 10 main oscillator clocks after the oscillator is stable is required to guarantee a valid chip reset. At power-up, 10 milliseconds should be allowed for the oscillator to start up and stabilize after V_{DD} reaches operational voltage. An internal reset with a minimum duration of 10 clock pulses will also be applied if the watchdog timer generates an internal device reset.

The RESET_N pin is located in the RTC power domain. This means that the RTC power must be present for an external reset to have any effect. The RTC power domain nominally runs from 1.2 V, but the RESET_N pin can be driven as high as 1.95 V.

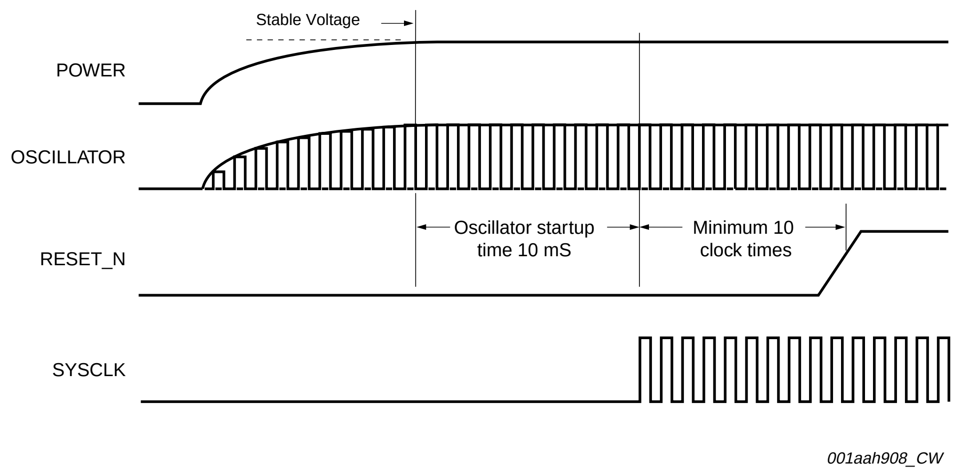


Fig 4. Power-up reset

6.24 Clocking and power control

Clocking in the LPC3180/01 is designed to be versatile, so that system and peripheral requirements may be met, while allowing optimization of power consumption. Clocks to most functions may be turned off if not needed, some peripherals do this automatically.

The LPC3180/01 includes three operational modes that give control over processing speed and power consumption. In addition, clock rates to different functional blocks may be controlled by changing clock sources, reconfiguring PLL values, or altering clock divider configurations. This allows a trade-off of power versus processing speed based on application requirements.

6.24.1 Crystal oscillator

The main oscillator is the basis for the clocks most chip functions use by default. Optionally, many functions can be clocked instead by the output of a PLL (with a fixed 397x rate multiplication) which runs from the RTC oscillator. In this mode, the main oscillator may be turned off unless the USB interface is enabled. If a SYSCLK frequency other than 13 MHz is required in the application, or if the USB block is not used, the main oscillator may be used with a frequency of between 1 MHz and 20 MHz.

6.24.2 PLLs

The LPC3180/01 includes three PLLs: one allows boosting the RTC frequency to 13.008896 MHz for use as the primary system clock; one provides the 48 MHz clock required by the USB block; and one provides the basis for the CPU clock, the AHB bus clock, and the main peripheral clock.

The first PLL multiplies the 32768 Hz RTC clock by 397 to obtain a 13.008896 MHz clock. The 397x PLL is designed for low power operation and low jitter. This PLL requires an external RC loop filter for proper operation.

The other two PLLs accept an input clock from either the main oscillator or the output of the 397x PLL. The input frequency is multiplied up to a higher frequency, then divided down to provide the output clock.

The PLL input may initially be divided down by a pre-divider value ‘N’, which may have the values 1, 2, 3, or 4. This pre-divider can allow a greater number of possibilities for the output frequency.

Following the PLL input divider is the PLL multiplier. This can multiply the pre-divider output by a value ‘M’, in the range of 1 through 256. The resulting frequency must be in the range of 156 MHz to 320 MHz. The multiplier works by dividing the output of a Current Controlled Oscillator (CCO) by the value of M, then using a phase detector to compare the divided CCO output to the pre-divider output. The error value is used to adjust the CCO frequency.

At the PLL output, there is a post-divider that can be used to bring the CCO frequency down to the desired PLL output frequency. The post-divider value ‘P’, can divide the CCO output by 1, 2, 4, 8, or 16. The post-divider can also be bypassed, allowing the PLL CCO output to be used directly. The maximum PLL output frequency that is supported by the CPU is 208 MHz.

6.24.3 Power control and modes

The LPC3180/01 supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: Run mode, Direct Run mode, and Stop mode.

Run mode is the normal operating mode for applications that require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. In Run mode, the CPU can run at up to 208 MHz and the AHB bus can run at up to 104 MHz.

Direct Run mode allows reducing the CPU and AHB bus rates in order to save power. Direct Run mode can also be the normal operating mode for applications that do not require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. Direct Run mode is the default mode following chip reset.

Stop mode causes all CPU and AHB operation to cease, and stops clocks to peripherals other than the USB block.

6.24.4 APB bus

Many peripheral functions are accessed by on-chip APB busses that are attached to the higher speed AHB bus. The APB bus performs reads and writes to peripheral registers in three peripheral clocks.

6.24.5 FAB bus

Some peripherals are placed on a special bus called FAB that allows faster CPU access to those peripheral functions. Write access to FAB peripherals takes a single AHB clock. Read access to FAB peripherals takes two AHB clocks.

6.25 Emulation and debugging

The LPC3180/01 supports emulation and debugging via a dedicated JTAG serial port. An Embedded Trace Buffer allows tracing program execution. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

6.25.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. The EmbeddedICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or entering the debug state.

6.25.2 Embedded trace buffer

The Embedded Trace Module (ETM) is connected directly to the ARM core. It compresses the trace information and exports it through a narrow trace port. An internal Embedded Trace Buffer of 2 k $\times$ 24 bits captures the trace information under software debugger control. Data from the Embedded Trace Buffer is recovered by the debug software through the JTAG port.

The trace contains information about when the ARM core switches between states. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. For data accesses either data or address or both can be traced.

7. Limiting values

Table 4. Limiting values for LPC3180/01

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)		[2]	–0.5	+1.4	V
$V_{DD(1V8)}$	supply voltage (1.8 V)		[3]	–0.5	+2.4	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		[4]	–0.5	+4.6	V
V_{DD}	supply voltage		[5]	–0.5	+4.6	V
V_{IA}	analog input voltage			–0.5	+4.6	V
V_I	input voltage	1.8 V pins	[6]	–0.5	+2.4	V
		3.3 V pins	[6]	–0.5	+4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
T_{stg}	storage temperature			–40	+125	°C
$P_{tot(pack)}$	total power dissipation (per package)	Max. Junction Temp 125 °C Max. Ambient Temp 85 °C	[7]		0.94	W
V_{esd}	electrostatic discharge voltage	HBM	[8]		+2000	V
		CDM	[9]		+500	V

[1] The following applies to Table 4:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Core, PLL, oscillator, and RTC supplies; applies to pins VDD_CORE12_01 to VDD_CORE12_08, VDD_COREFXD12_01 to VDD_COREFXD12_02, VDD_OSC12, VDD_PLL397_12, VDD_PLLHCLK_12, VDD_PLLUSB_12, VDD_RTC12, VDD_RTCCORE12, VDD_RTCOSC12, and VDD12.

[3] I/O pad supply; applies to pins VDD_RAM.

[4] Applies to VDD_AD28 pins.

[5] Applies to pins VDD_IOA, VDD_IOB, VDD_IOC and VDD_IOD.

[6] Including voltage on outputs in 3-state mode.

[7] Based on package (LFBGA320) heat transfer, not device power consumption

- calculated Pkg Thermal Resistance ($Theta_{JA}$): 42.407 °C/W (with JEDEC Test Board (4.5" x 4.0") and 0 m/s airflow, ±15% accuracy)

[8] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[9] Charge device model per AEC-Q100-011.

8. Static characteristics

8.1 Static characteristics LPC3180/01

Table 5. Static characteristics for the LPC3180/01
T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)	core supply voltage for normal operation; full frequency range	[2]	1.1	1.2	1.3	V
		core supply voltage for reduced power; up to 14 MHz CPU	[2]	0.9	-	1.3	V
		RTC supply voltage	[3]	0.9	-	1.3	V
		PLL and oscillator supply voltage	[4]	1.1	1.2	1.3	V
$V_{DD(SDRAM)}$	SDRAM supply voltage	in 1.8 V range	[5]	1.7	1.8	1.95	V
		in 3.3 V range		2.7	3.3	3.6	V
$V_{DD(IO)}$	I/O supply voltage	in 1.8 V range	[6]	1.7	1.8	1.95	V
		in 3.3 V range		2.7	3.3	3.6	V
$V_{DDA(3V0)}$	analog supply voltage (3 V)	applies to VDD_AD28 pins		2.7	3.3	3.6	V
Run, Direct Run and Stop modes							
$I_{DD(run)}$	Run mode supply current	VDD_CORE12 = 1.2 V; T_{amb} = 25 °C; I-cache enabled; CPU clock = 208 MHz; all peripherals enabled		-	80	-	mA
$I_{DD(drun)}$	Direct Run mode supply current	VDD_CORE12 = 0.9 V; T_{amb} = 25 °C; CPU clock = 13 MHz		-	7	-	mA
$I_{DD(stop)}$	Stop mode supply current	VDD_CORE12 = 0.9 V; T_{amb} = 25 °C; CPU clock = stopped internally		-	500	-	µA
$I_{DD(rtc)}$	RTC supply current	VDD_RTCCORE12 = VDD_RTC12 = VDD_RTCOSC12 = 1.2 V; T_{amb} = 25 °C;		-	4	-	µA
Input pins and I/O pins configured as input							
V_I	input voltage		[7][9]	0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		$0.7 \times V_{DD(IO)}$	-	-	V
		3.3 V inputs		$0.7 \times V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage	1.8 V inputs		-	-	$0.3 \times V_{DD(IO)}$	V
		3.3 V inputs		-	-	$0.3 \times V_{DD(IO)}$	V
V_{hys}	hysteresis voltage	1.8 V inputs		$0.1 \times V_{DD(IO)}$			V
		3.3 V inputs		$0.1 \times V_{DD(IO)}$			V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; no pull-down	[7]	-	-	1	µA

Table 5. Static characteristics for the LPC3180/01 *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[7]	-	-	100	mA
I_{pu}	pull-up current	1.8 V inputs with pull-up; V_I = 0		6	12	22	µA
		3.3 V inputs with pull-up; V_I = 0		25	50	80	µA
I_{pd}	pull-down current	1.8 V inputs with pull-down; $V_I = V_{DD}$		5	12	22	µA
		3.3 V inputs with pull-down; $V_I = V_{DD}$		25	50	85	µA
C_i	input capacitance	excluding bonding pad capacitance		-	-	3.3	pF
Output pins and I/O pins configured as output							
V_O	output voltage		[7][8][9][10]	0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	1.8 V outputs; I_{OH} = −1 mA	[11]	$V_{DD(IO)} - 0.4$	-	-	V
		3.3 V outputs; I_{OH} = −4 mA	[11]	$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	1.8 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
		3.3 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{DD} = 1.8 V; $V_{OH} = V_{DD} - 0.4$ V	[7][11]	−3.3	-	-	mA
		V_{DD} = 3.3 V; $V_{OH} = V_{DD} - 0.4$ V		−6.5	-	-	mA
I_{OL}	LOW-level output current	V_{DD} = 1.8 V; V_{OL} = 0.4 V	[7][11]	1.5	-	-	mA
		V_{DD} = 3.3 V; V_{OL} = 0.4 V		3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down	[7]	-	-	1	µA
I_{OHS}	HIGH-level short-circuit output current	V_{DD} = 1.8 V; V_{OH} = 0 V	[12]	-	-	66	mA
		V_{DD} = 3.3 V; V_{OH} = 0 V		-	-	183	mA
I_{OLS}	LOW-level short-circuit output current	V_{DD} = 1.8 V; $V_{OL} = V_{DD}$	[7][12]	-	-	34	mA
		V_{DD} = 3.3 V; $V_{OL} = V_{DD}$		-	-	105	mA
Z_o	output impedance	V_{DD} = 1.8 V		40	-	60	ohm
		V_{DD} = 3.3 V		40	-	60	ohm
SDRAM pins							
V_I	input voltage		[7][9]	0	-	$V_{DD(SDRAM)}$	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		$0.7 \times V_{DD(SDRAM)}$	-	-	V
		3.3 V inputs		$0.7 \times V_{DD(SDRAM)}$	-	-	V
V_{IL}	LOW-level input voltage	1.8 V inputs		-	-	$0.3 \times V_{DD(SDRAM)}$	V
		3.3 V inputs		-	-	$0.3 \times V_{DD(SDRAM)}$	V
V_{hys}	hysteresis voltage	1.8 V inputs		0.4	-	0.6	V
		3.3 V inputs		0.55	-	0.85	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	0.3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(SDRAM)}$; no pull-down	[7]	-	-	0.3	µA

Table 5. Static characteristics for the LPC3180/01 *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[7]	-	-	100	mA
I_{pu}	pull-up current	1.8 V inputs with pull-up; V_I = 0		34	62	107	µA
		3.3 V inputs with pull-up; V_I = 0		97	169	271	µA
I_{pd}	pull-down current	1.8 V inputs with pull-down; $V_I = V_{DD(SDRAM)}$		23	51	93	µA
		3.3 V inputs with pull-down; $V_I = V_{DD(SDRAM)}$		73	155	266	µA
C_i	input capacitance	excluding bonding pad capacitance		-	-	2.1	pF
V_O	output voltage		[7][8] [9][10]	0	-	$V_{DD(SDRAM)}$	V
V_{OH}	HIGH-level output voltage	1.8 V outputs; I_{OH} = −1 mA	[11]	$V_{DD(SDRAM)} - 0.3$	-	-	V
		3.3 V outputs; I_{OH} = −4 mA	[11]	$V_{DD(SDRAM)} - 0.3$	-	-	V
V_{OL}	LOW-level output voltage	1.8 V outputs; I_{OL} = 4 mA	[11]	-	-	0.3	V
		3.3 V outputs; I_{OL} = 4 mA	[11]	-	-	0.3	V
I_{OH}	HIGH-level output current	V_{DD} = 1.8 V; $V_{OH} = V_{DD} - 0.4$ V	[7][11]	−6	-	-	mA
		V_{DD} = 3.3 V; $V_{OH} = V_{DD} - 0.4$ V		−6	-	-	mA
I_{OL}	LOW-level output current	V_{DD} = 1.8 V; V_{OL} = 0.4 V	[7][11]	6	-	-	mA
		V_{DD} = 3.3 V; V_{OL} = 0.4 V		6	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down	[7]	-	-	0.3	µA
I_{OHS}	HIGH-level short-circuit output current	V_{DD} = 1.8 V; V_{OH} = 0 V	[12]	-	-	−49	mA
		V_{DD} = 3.3 V; V_{OH} =0 V		-	-	−81	mA
I_{OLS}	LOW-level short-circuit output current	V_{DD} = 1.8 V; $V_{OL} = V_{DD}$	[7][11]	-	-	49	mA
		V_{DD} = 3.3 V; $V_{OL} = V_{DD}$		-	-	86	mA
Z_o	output impedance	V_{DD} = 1.8 V		35	40	58	ohm
		V_{DD} = 3.3 V		32	35	45	ohm
I^2C-bus pins							
V_I	input voltage		[7][9]	0	-	5.5	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		$0.7 \times V_{DD(IO)}$	-	-	V
		3.3 V inputs		$0.7 \times V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage	1.8 V inputs		-	-	$0.3 \times V_{DD(IO)}$	V
		3.3 V inputs		-	-	$0.3 \times V_{DD(IO)}$	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	10	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; no pull-down	[7]	-	-	10	µA
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[7]	-	-	100	mA
C_i	input capacitance	Excluding bonding pad capacitance		-	-	1.6	pF

Table 5. Static characteristics for the LPC3180/01 *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OL}	LOW-level output voltage	1.8 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
		3.3 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
I_{OL}	LOW-level output current	V_{DD} = 1.8 V; V_{OL} = 0.4V	[7][11]	3	-	-	mA
		V_{DD} = 3.3 V; V_{OL} = 0.4V		3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down	[7]	-	-	10	µA
I_{OLS}	LOW-level short-circuit output current	V_{DD} = 1.8 V; V_{OL} = V_{DD}	[7][12]	-	-	40	mA
		V_{DD} = 3.3 V; V_{OL} = V_{DD}		-	-	40	mA
ONSW pins							
V_O	output voltage		[8][9][10][11]	0	-	$V_{DD(1V2)}$	V
V_{OH}	HIGH-level output voltage	1.2 V outputs; I_{OH} = −1 mA	[11]	$V_{DD(1V2)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	1.2 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V	[7][11]	-4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7][11]	3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down	[7]	-	-	1.5	µA
I_{OHS}	HIGH-level short-circuit output current	V_{DD} = 1.8 V; V_{OH} = 0 V	[12]	-	-	−135	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[7][12]	-	-	135	mA
Z_o	output impedance	V_{DD} = 1.2 V		40	-	60	ohm
Reset pins							
V_I	input voltage		[7][9]	0	-	1.95	V
V_{IH}	HIGH-level input voltage	1.2 V inputs		0.7 × $V_{DD(1V2)}$	-	-	V
V_{IL}	LOW-level input voltage	1.2 V inputs		-	-	0.7 × $V_{DD(1V2)}$	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	1	µA
I_{IH}	HIGH-level input current	V_I = V_{DD}; no pull-down	[7]	-	-	1	µA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down	[7]	-	-	1	µA
I_{latch}	I/O latch-up current	−(1.5V_{DD}) < V_I < (1.5V_{DD})	[7]	-	-	100	mA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Applies to VDD_CORE12_01 to VDD_CORE12_08 pins.

[3] Applies to pins VDD_RTC12, VDD_RTCCORE12, and VDD_RTCOSC12.

[4] Applies to pins VDD_COREFXD12_01 to VDD_COREFXD12_02, VDD_OSC12, VDD_PLL397_12, VDD_PLLHCLK_12, VDD_PLLUSB_12, and VDD12.

[5] Applies to VDD_RAM, VDD_IOC pins.

[6] Applies to VDD_IOA, VDD_IOB, and VDD_IOD pins.

[7] Referenced to the applicable V_{DD} for the pin.

[8] Including voltage on outputs in 3-state mode.

[9] The applicable V_{DD} voltage for the pin must be present.

[10] 3-state outputs go into 3-state mode when $V_{DD(3V0)}$ is grounded.

[11] Accounts for 100 mV voltage drop in all supply lines.

[12] Only allowed for a short time period.

8.1.1 Power Supply Sequencing

The LPC32x0 has no power sequencing requirements, that is, VDD(1V2), VDD(SDRAM), VDD(IO), and VDDA(3V0) can be switched ‘On’ or ‘Off’ independent of each other. An internal circuit takes care that the system correctly powers up in the absence of core-power. During IO power-up this circuit takes care the system is powered in a defined mode, and during core power-down the same is valid.

8.2 Analog to digital Converter (ADC) static characteristics

Table 6. ADC static characteristics

V_{DDA} = 3.3 V; T_{amb} = 25 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	±0.5	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	±0.6	±1	LSB
E_O	offset error	[1][5]	-	±1	±3	LSB
E_G	gain error	[1][6]	-	±0.3	±0.6	%
E_T	absolute error	[1][7]	-		±4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

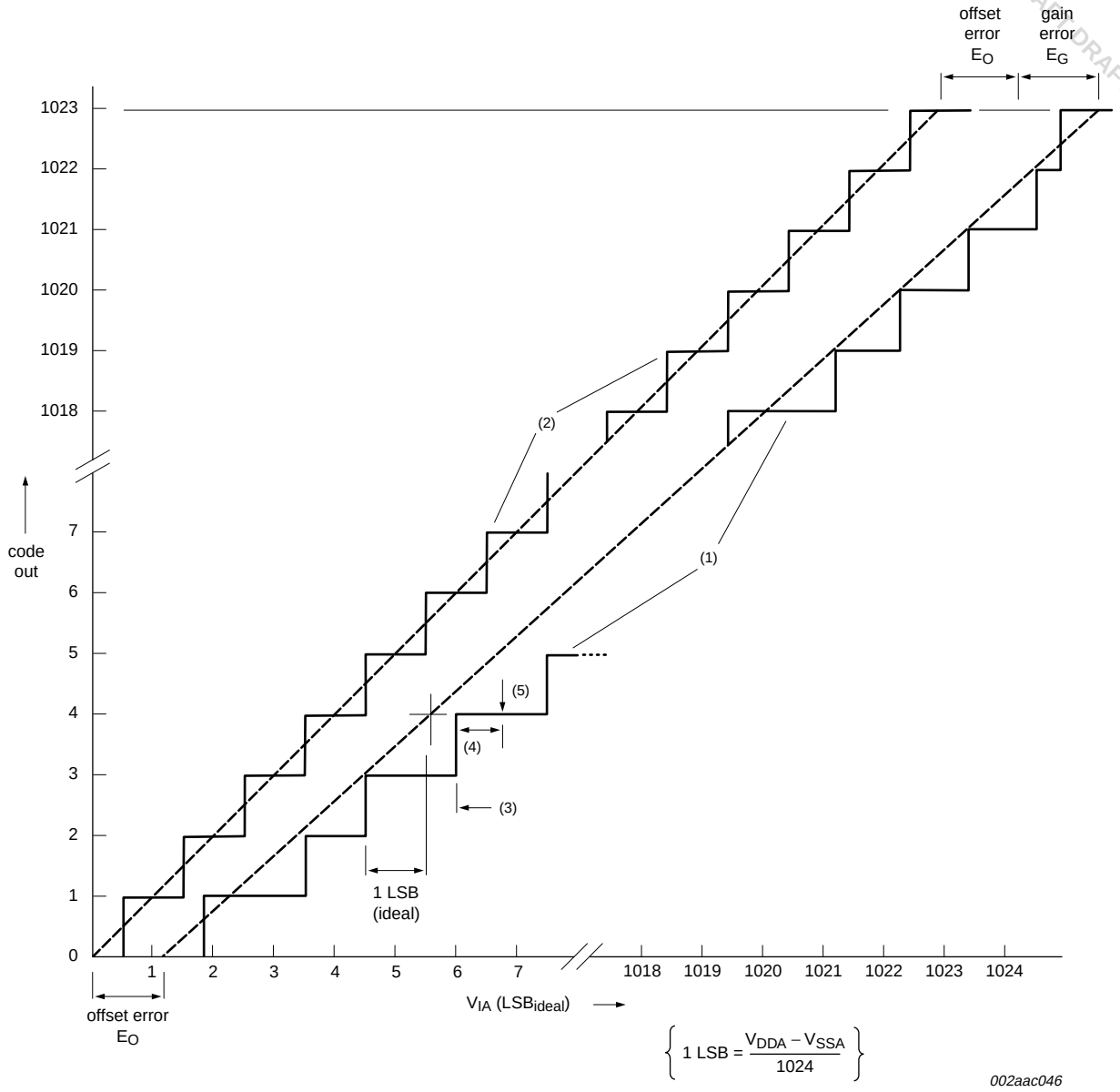
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics

9. Dynamic characteristics

9.1 Clocking and I/O Port pins

Table 7. Dynamic characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset						
$f_{W(RESET\_N)}$	external RESET_N pulse width	[2]	10	-	-	ms
External clock						
f_{ext}	external clock frequency	[2]	1	13	20	MHz
Port pins						
t_r	rise time		-	5	-	ns
t_f	fall time		-	5	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Supplied by an external crystal.

9.2 SDR SDRAM controller

Table 8. EMC SDR SDRAM memory interface dynamic characteristics for LPC3180/01

T_a = −40 °C to +85 °C, unless otherwise specified.[1][2]

Symbol	Parameter	Min	Typical	Max	Unit
f_{oper}	operating frequency [3]		104	104	MHz
T_{CLCL}	clock cycle time	-	9.6	-	ns
t_{CLCX}	clock LOW time	-	4.8	-	ns
t_{CHCX}	clock HIGH time	-	4.8	-	ns
$t_{d(CV)}$	control valid delay time [4]	-	(CMD_DLY x 0.25) + 2.7		ns
$t_{h(C)}$	control hold time [4]		(CMD_DLY x 0.25) + 1.2	-	ns
$t_{d(AV)}$	address valid delay time	-	(CMD_DLY x 0.25) + 3.4		ns
$t_{h(A)}$	address hold time		(CMD_DLY x 0.25) + 1.2	-	ns
$t_{d(QV)}$	data output valid delay time	-	(CMD_DLY x 0.25) + 3.5		ns
$t_{h(Q)}$	data output hold time		(CMD_DLY x 0.25) + 1.2	-	ns
$t_{su(D)}$	data input set-up time	-	0.6	-	ns
$t_{h(D)}$	data input hold time	-	0.9	-	ns
t_{QZ}	data output high-impedance time			$<T_{CLCL}$	ns

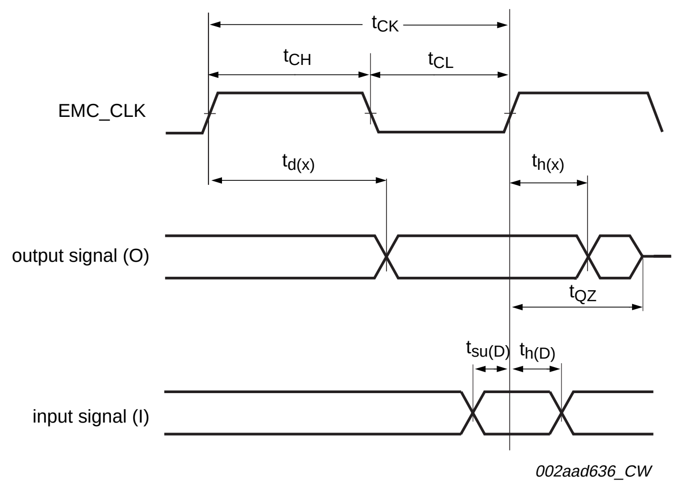
[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] All values valid for EMC pads set to high slew rate. VDD_EMC = 1.8 ± 0.18 V. VDD_CORE = 1.2 ± 0.12 V or EMC pads set to low slew rate. VDD_EMC = 3.3 ± 0.3 V. VDD_CORE = 1.2 ± 0.12 V.

[3] $f_{oper} = 1/t_{CLCL}$

[4] Applies to signals: DQM, CSN, RASN, CASN, WEN, CKE.

[5] CMD_DLY = COMMAND_DELAY bitfield in SDRAMCLK_CTRL[18:14] register.



(1) x can represent the following names: address (A), control (C) or data (Q)

Fig 6. SDR SDRAM Signal timing

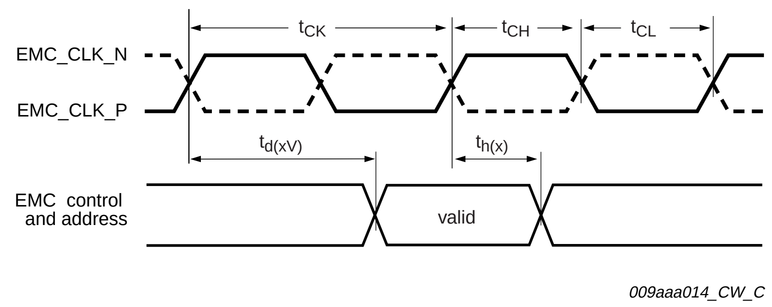
9.3 DDR SDRAM Controller

Table 9. EMC DDR SDRAM memory interface dynamic characteristics[1]
C_L = 25 pF; T_{amb} = 40 °C.

Symbol	Parameter		Min	Typical	Max	Unit
-	Operating frequency			104		MHz
t_{CK}	Clock cycle time			9.6		ns
t_{CH}	Clock high level width			0.5		tCK
t_{CL}	Clock low level width			0.5		tCK
$t_{d(CV)}$	control valid delay time			(CMD_DLY x 0.25) + 1.5		ns
$t_{h(C)}$	control hold time			(CMD_DLY x 0.25) - 1.5		ns
$t_{d(AV)}$	address valid delay time			(CMD_DLY x 0.25) + 1.5		ns
$t_{h(A)}$	address hold time			(CMD_DLY x 0.25) - 1.5		ns
t_{DS}	DQ & DM output setup time to DQS out			0.275		tCK
t_{DH}	DQ & DM output hold time to DQS out			0.225		tCK
t_{DQSH}	Write DQS output high width			0.5		tCK
t_{DQSL}	Write DQS output low width			0.5		tCK
t_{DQSS}	Write cmd to 1st DQS out latching transition			tCK + (CMD_DLY x 0.25)		tCK
t_{DSS}	DQS in falling edge to CK setup time			.5		tCK
t_{DSH}	DQS in falling edge hold time from CK			.5		tCK
t_{DQSD}	DQS_in to DQS_DELAY	[2]		DQS_DELAY		ns
$t_{su(D)}$	data input set-up time			0.3		ns
$t_{h(D)}$	data input hold time			0.5		ns

[1] All values valid for EMC pads set to high slew rate at 1.8V .

[2] DQS_DELAY, see LP3180/01 user manual, SDRAM Memory Controller Chapter, Section 8 DDR DQS delay calibration for details on configuring this value.



(1) x can represent the following names: address (A) or control (C)

Fig 7. DDR Control timing parameters

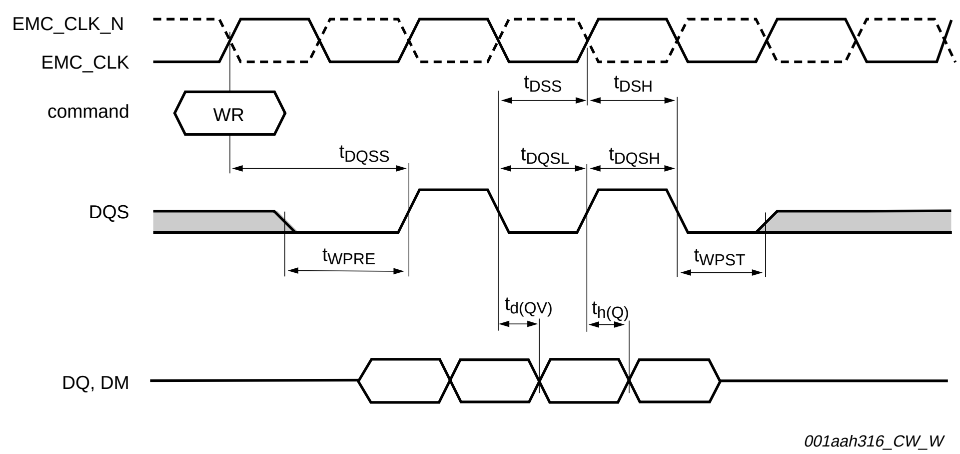
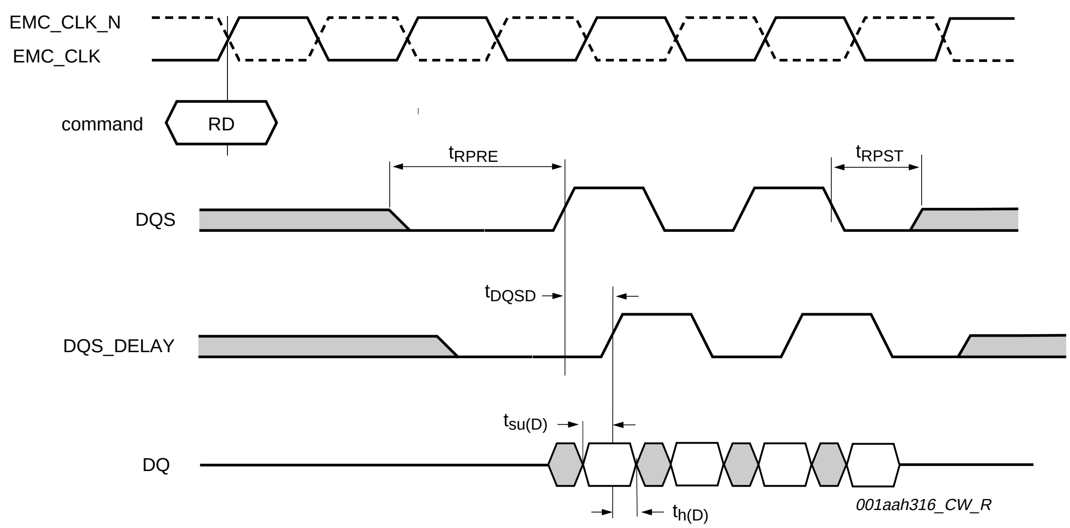


Fig 8. DDR Write timing parameters



DQS_DELAY is an internal signal shown for reference only

Fig 9. DDR Read timing parameters

9.4 USB Controller

Table 10. Dynamic characteristics USB digital I/O pins

$V_{DD(IO)}$ = 3.3 V; T_{amb} = −40 °C to +85 °C, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TIO}	bus turnaround time (I/O)	OE_N/INT_N to DAT/VP and SE0/VM	-	7	-	ns
t_{TOI}	bus turnaround time (O/I)	OE_N/INT_N to DAT/VP and SE0/VM	-	0	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

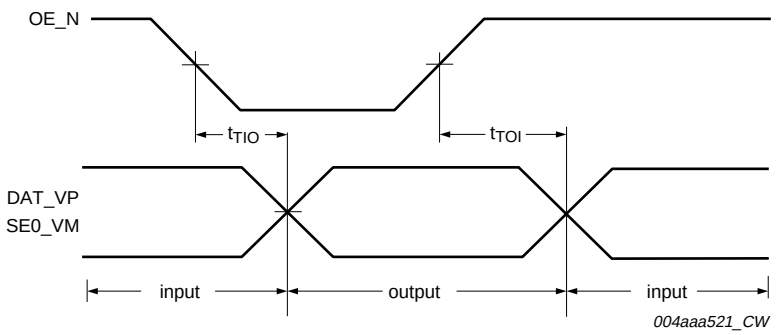


Fig 10. USB bus turnaround time

9.5 Secure Digital (SD) card interface

Table 11. Dynamic characteristics: SD card pin interface

T_{amb} = –40 °C to +85 °C for industrial applications; $V_{DD(1V8)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$T_{cy(clk)}$	clock cycle time	on pin MS_SCLK; Data Transfer Mode	-	-	25	MHz
		on pin MS_SCLK; Identification Mode	-	-	400	kHz
$t_{su(D)}$	data input set-up time	on pins MS_BS, MS_DIO[3:0] as inputs		2.7		ns
$t_{h(D)}$	data input hold time	on pins MS_BS, MS_DIO[3:0] as inputs		0		ns
$t_{d(QV)}$	data output valid delay time	on pins MS_BS, MS_DIO[3:0] as outputs		9.7		ns
$t_{h(Q)}$	data output hold time	on pins MS_BS, MS_DIO[3:0] as outputs		7.7		ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

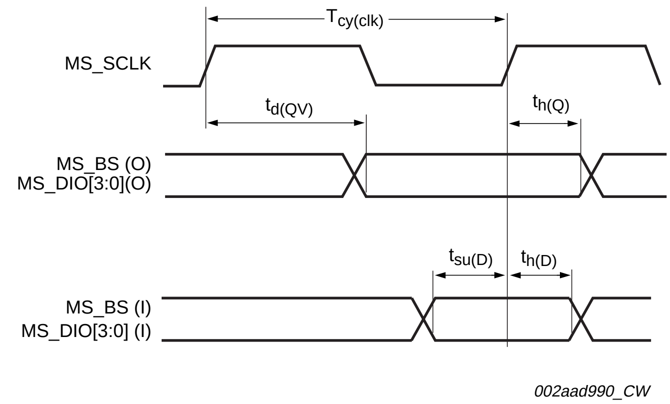


Fig 11. SD card pin interface timing

9.6 MLC NAND flash memory controller

Table 12. Dynamic characteristics of MLC NAND Flash Memory pins

Symbol	Parameter (from NAND Flash controller perspective)		Typical	Unit
$t_{d(CERE)}$	CE# to RE# time	[1][8]	T_{HCLK} x CEA_D	ns
t_{RC}	RE# cycle time	[1][4][5]	T_{HCLK} x (R_L + 1) + T_{HCLK} x (R_H - R_L)	ns
t_{REH}	RE# high time	[1][4][5]	T_{HCLK} x (R_H - R_L)	ns
t_{RHZ}	RE# high to output hi-Z	[1][4][6]	T_{HCLK} x (R_H - R_L) + T_{HCLK} x (R_{HZ})	ns
t_{RP}	RE# pulse width	[1][4]	T_{HCLK} x (R_L + 1)	ns
t_{RB}	RE# high to R/B#	[1][7]	T_{HCLK} x (B_D)	ns
t_{WB}	WE# high to R/B# low	[1][7]	T_{HCLK} x (B_D)	ns
t_{WC}	WE# cycle time	[1][2][3]	T_{HCLK} x (W_L + 1) + T_{HCLK} x (W_H - W_L)	ns
t_{WH}	WE# high time	[1][2][3]	T_{HCLK} x (W_H - W_L)	ns
t_{WP}	WE# pulse width	[1][2]	T_{HCLK} x (W_L + 1)	ns

[1] T_{HCLK} = 1/HCLK

[2] W_L = bitfield WR_LOW[3:0] in register MLC_TIME_REG[3:0]

[3] W_H = bitfield WR_HIGH[3:0] in register MLC_TIME_REG[7:4] f

[4] R_L = bitfield RD_LOW[3:0] in register MLC_TIME_REG[11:8]

[5] R_H = bitfield RD_HIGH [3:0] in register MLC_TIME_REG[15:12]

[6] R_{HZ} = bitfield NAND_TA[2:0] in register MLC_TIME_REG[18:16]

[7] B_D = bitfield BUSY_DELAY[4:0] in register MLC_TIME_REG[23:19]

[8] CEA_D = bitfield TCEA_DELAY[1:0] in register MLC_TIME_REG[25:24]

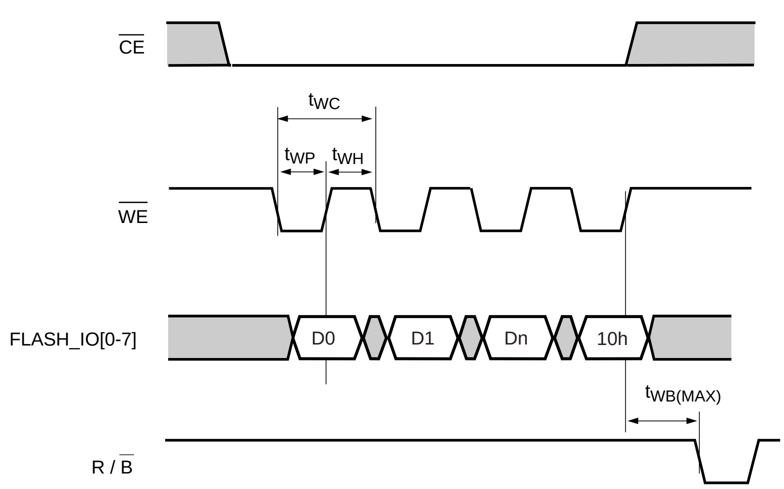


Fig 12. MLC NAND flash controller write timing

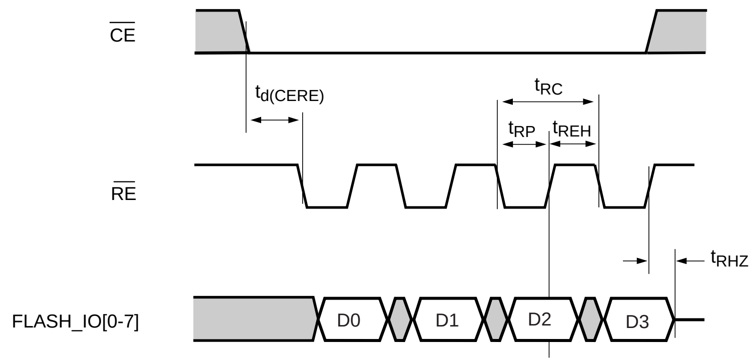


Fig 13. MLC NAND flash controller read timing

Table 13. Dynamic characteristics of SLC NAND Flash Memory pins

Symbol	Parameter (from NAND Flash perspective)		Typical Reads	Typical Writes	Unit
t_{ALS}	ALE setup time	[1][2][4][6]	(T_{HCLK} x (Rsu + Rw))	(T_{HCLK} x (Wsu + Ww))	ns
t_{ALH}	ALE hold time	[1][7]	(T_{HCLK} x (Rh))	(T_{HCLK} x (Wh))	ns
t_{AR}	ALE to RE# delay	[1][2][6]	(T_{HCLK} x (Rsu))	(T_{HCLK} x (Wsu))	ns
t_{CEA}	CE# access time	[1][2][4][6][8]	(T_{HCLK} x (Rsu + Rw))	(T_{HCLK} x (Wsu + Ww))	ns
t_{CS}	CE# setup time	[1][2][4][6][8]	(T_{HCLK} x (Rsu + Rw))	(T_{HCLK} x (Wsu + Ww))	ns
t_{CH}	CE# hold time	[1][3]	(T_{HCLK} x (Rh))	(T_{HCLK} x (Wh))	ns
t_{CLS}	CLE setup time	[1][2][4][6][8]	(T_{HCLK} x (Rsu + Rw))	(T_{HCLK} x (Wsu + Ww))	ns
t_{CLH}	CLE hold time	[1][3]	(T_{HCLK} x (Rh))	(T_{HCLK} x (Wh))	ns
t_{CLR}	CLE to RE# delay	[1][2][6]	(T_{HCLK} x (Rsu))	(T_{HCLK} x (Wsu))	ns
t_{DH}	Data hold time (output from MCU)	[1][3][7]	(T_{HCLK} x (Rh))	(T_{HCLK} x (Wh))	ns
t_{DS}	Data setup time (output from MCU)	[1][2][4][6][8]	(T_{HCLK} x (Rsu + Rw))	(T_{HCLK} x (Wsu + Ww))	ns
t_{IR}	Output hi-Z to RE# low	[1][2][6]	(T_{HCLK} x (Rsu))	(T_{HCLK} x (Wsu))	ns
t_{RC}	RE# cycle time	[1][2]	(T_{HCLK} x (Rsu + Rw + Rh))		ns
t_{REA}	RE# access time	[1][4]	(T_{HCLK} x (Rw))		ns
t_{REH}	RE# high time	[1][2][3]	(T_{HCLK} x (Rsu + Rh))		ns
t_{RHOH}	RE# high to output hold (input hold for MCU)		0	0	ns
t_{RHZ}	RE# high to output hi-Z	[1]	(T_{HCLK} x (Rh))		ns
t_{RP}	RE# pulse width	[1][4]	(T_{HCLK} x (Rw))		ns
t_{RR}	Ready to RE# low	[1][2][3]	(T_{HCLK} x (Rsu))		ns
t_{WB}	WE# high to R/B# low	[1][8]		(T_{HCLK} x (Ww))	ns
t_{WC}	WE# cycle time	[1][6][7][8]		(T_{HCLK} x (Wsu + Ww + Wh))	ns
t_{WH}	WE# high time	[1][6][7]		(T_{HCLK} x (Wsu + Wh))	ns

Table 13. Dynamic characteristics of SLC NAND Flash Memory pins

Symbol	Parameter (from NAND Flash perspective)	Typical Reads	Typical Writes	Unit
t_{WHR}	WE# high to RE# low [1][6][7]		(T_{HCLK} x (Wsu + Wh))	ns
t_{WP}	WE# pulse width [1][8]		(T_{HCLK} x (Ww))	ns
t_{RB}	RE# high to R/B# [1][8]		(T_{HCLK} x (Ww))	ns

[1] xxxxT_{HCLK} = 1/HCLK

[2] Rsu = bitfield R_SETUP[3:0] in register SLC_TAC[3:0] for reads

[3] Rh = bitfield R_HOLD[3:0] in register SLC_TAC[7:4] for reads

[4] Rw = bitfield R_WIDTH[3:0] in register SLC_TAC[11:8] for reads

[5] Rb = bitfield R_RDY[3:0] in register SLC_TAC[15:12] for reads

[6] Wsu = bitfield W_SETUP[3:0] in register SLC_TAC[19:16] for writes

[7] Wh = bitfield W_HOLD[3:0] in register SLC_TAC[23:20] for writes

[8] Ww = bitfield W_WIDTH[3:0] in register SLC_TAC[27:24] for writes

[9] Wb = bitfield W_RDY[3:0] in register SLC_TAC[31:28] for writes

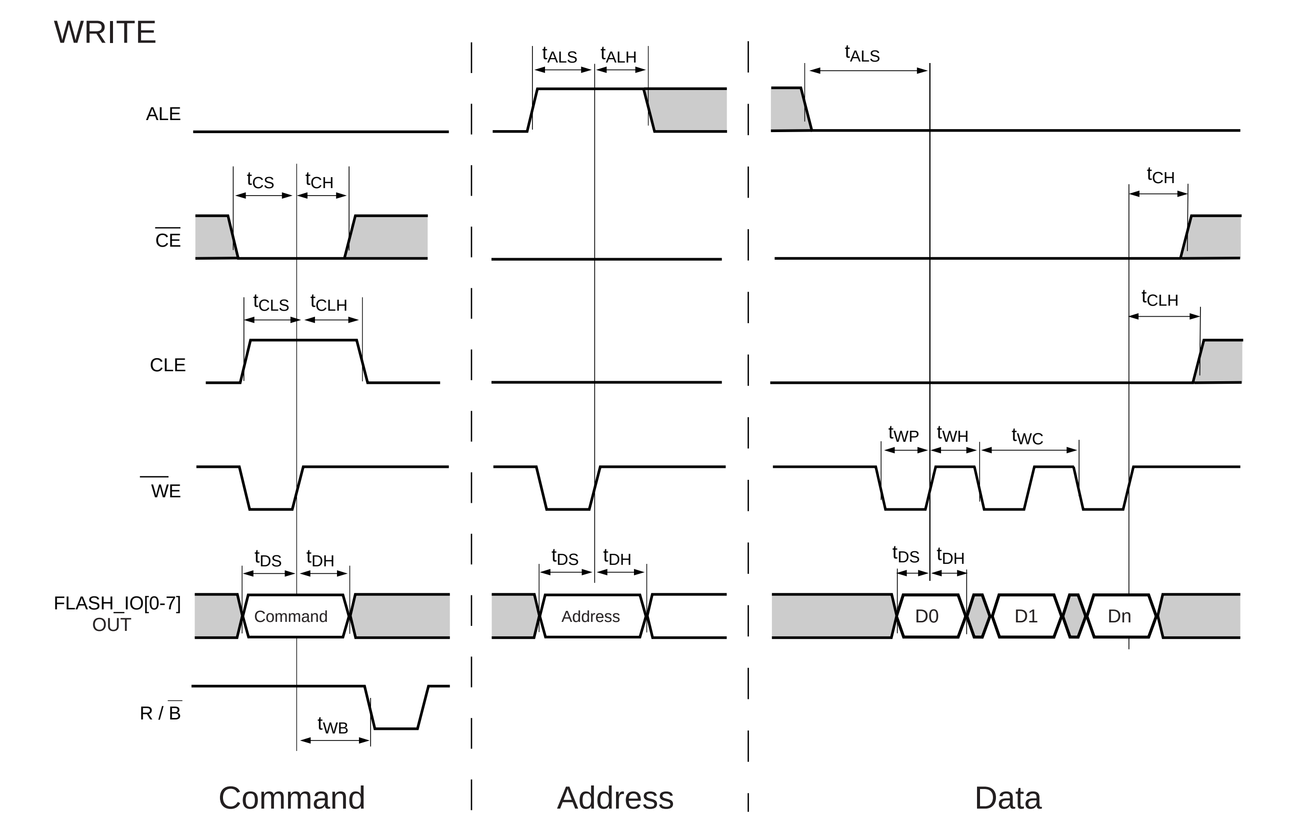


Fig 14. NAND flash memory write timing

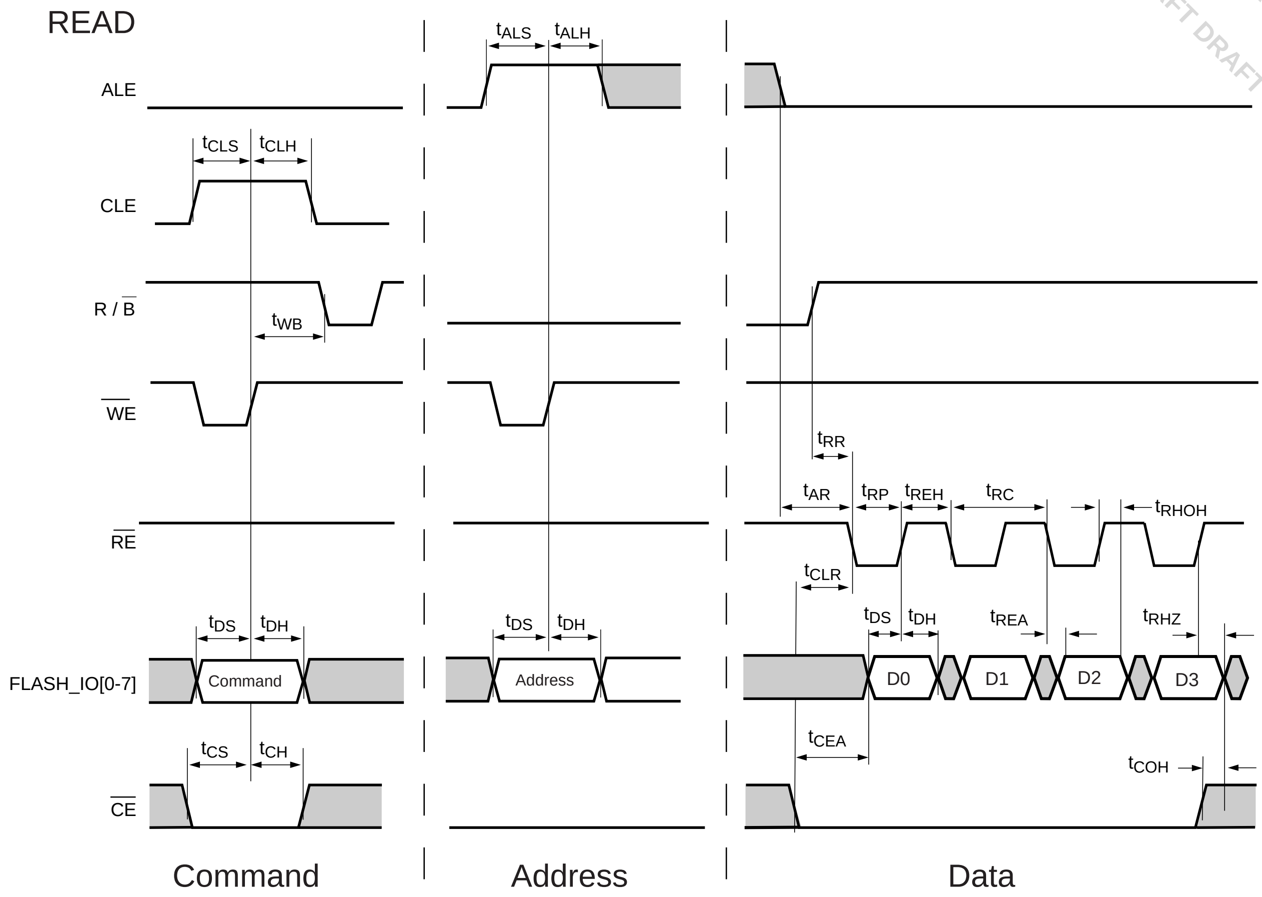


Fig 15. NAND flash memory read timing

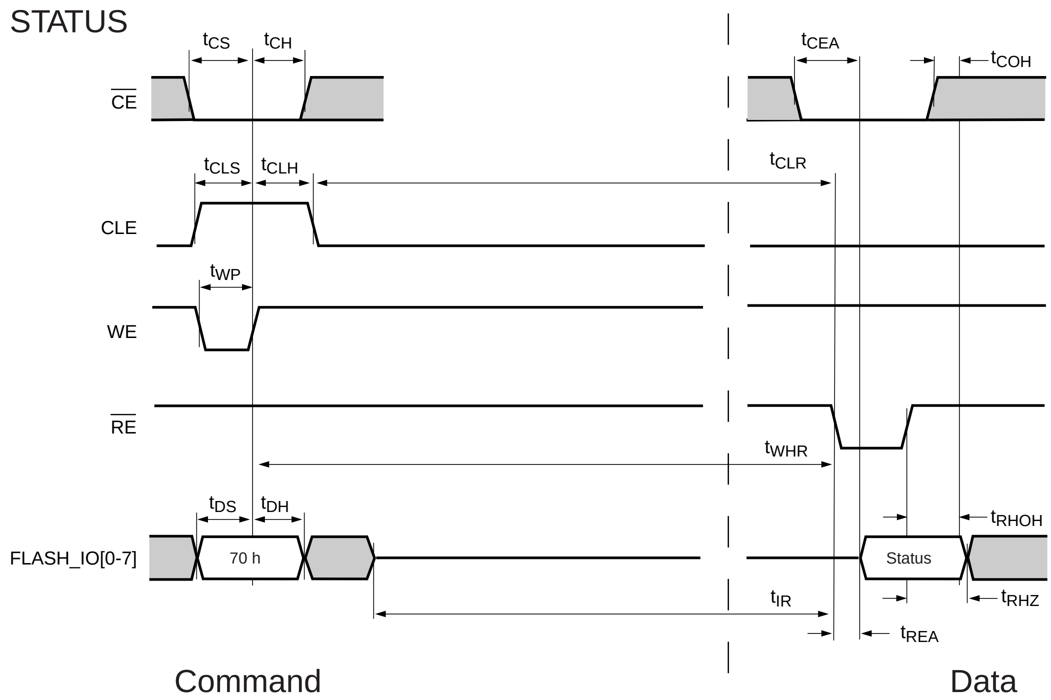


Fig 16. NAND flash memory status timing

9.7 SPI controller

Table 14. Dynamic characteristics of SPI pins for LPC3180/01

Symbol	Parameter		Min	Typ	Max	Unit
T_{SPICYC}	SPI cycle time	[1]	2 T_{HCLK}		256 T_{HCLK}	ns
SPI1						
t_{SPIDSU}	SPI data set-up time			6		ns
t_{SPIDH}	SPI data hold time			0		ns
t_{SPIDV}	SPI enable to output data valid time			2		ns
t_{SPIOH}	SPI output data hold time			0		ns
SPI2						
t_{SPIDSU}	SPI data set-up time			10		ns
t_{SPIDH}	SPI data hold time			0		ns
t_{SPIDV}	SPI enable to output data valid time			2		ns
t_{SPIOH}	SPI output data hold time			0		ns

[1] T_{HCLK} = period time of SPI IP block input clock (HCLK)

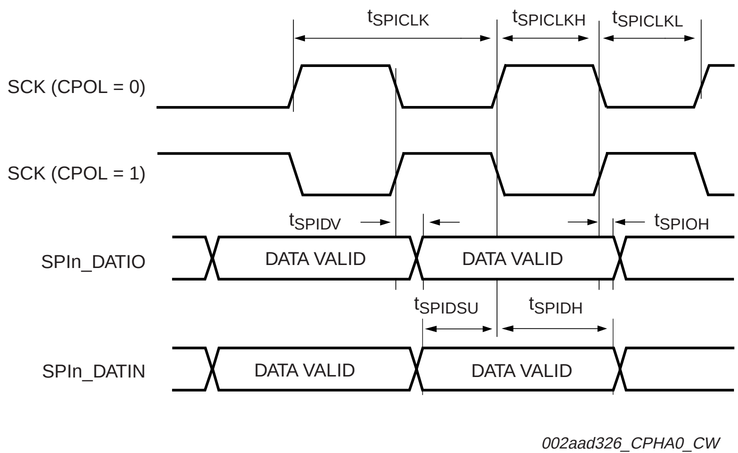


Fig 17. SPI master timing (CPHA = 0)

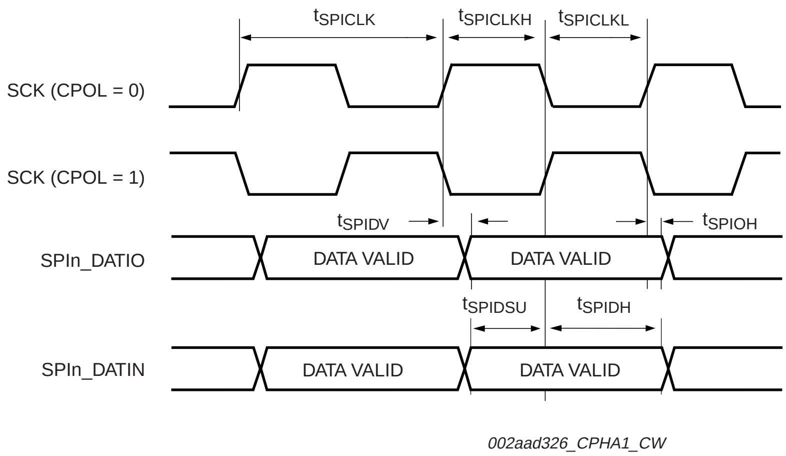
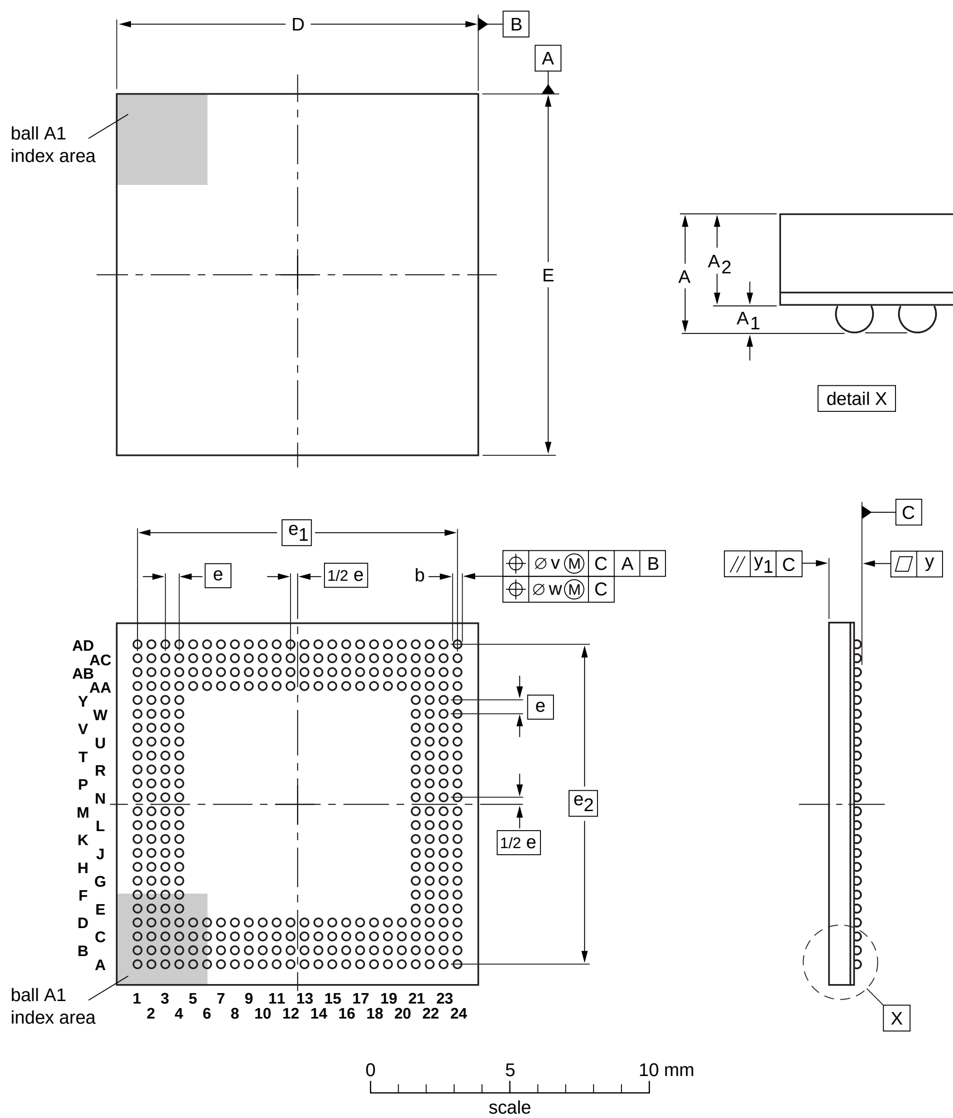


Fig 18. SPI master timing (CPHA = 1)

10. Package outline

LFBGA320: plastic low profile fine-pitch ball grid array package; 320 balls; body 13 x 13 x 0.9 mm **SOT824-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.3	0.3 0.2	1.0 0.8	0.35 0.25	13.1 12.9	13.1 12.9	0.5	11.5	11.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT824-1		- - -				03-07-09

Fig 19. Package outline SOT824-1 (LFBGA320)

11. Appendix

This appendix provides compatibility and comparison information between the LPC3180 and the LPC3180/01.

11.1 Compatibility with LPC3180

1. The reset states on 2 pins of each SPI have changed to better fit typical uses of this type of interface.
   - On reset, the LPC3180 configures the SPI1_CLK and SPI1_DATIO pins as outputs and drives them low; In contrast, the LPC3180/01 configures these pins as inputs and they should be pulled either high or low externally if not used.
   - On reset, the LPC3180 configures the SPI2_CLK and SPI2_DATIO pins as outputs and drives them low; In contrast, the LPC3180/01 configures these pins as inputs and thet should be pulled either high or low externally if not used.
2. The USB block has been integrated into the AHB Matrix. There are small USB timing changes that result from the integration of the USB block into the AHB matrix. These timing differences are application dependant and are unlikely to affect existing applications. Integration of the USB block into the AHB Matrix results in the following differences:
   - The USB block gets its timing from the AHB Matrix, which means the USB_HCLK signal is no longer needed. As a result, the USB clock enable bit PWR_CTRL [6] is no longer needed. This bit is reserved in the LPC3180/01. Writing to this register bit has no effect; the value read from this register bit is undefined.
   - The USB DMA controller can now access the internal SRAM in addition to external memory
3. The pull-ups and pull-downs on the JTAG pins have been changed in order to comply with IEEE JTAG recommendations. This should have no impact on compatibility.
   - The pull-up on TCK is removed.
   - The pull-down on NRST is changed to a pull-up.
4. Pull-ups are removed from the following pins on UART7:
   - U7_RX
   - U7_HCTS

   This change should not affect backward compatibility, with the exception that if the pins are not used they should be pulled either high or low externally.
5. The LPC3180 I^{2}C-bus supports master operation only. The LPC3180/01 has an enhanced I^{2}C-bus block that supports slave and multi-master operation in addition to master operation.
6. Many power, ground, and internally connected pins on the LPC3180 are different from the LPC3180/01. See Table 16 for details. This change should not affect backward compatibility.
7. LPC3180/01 U3_TX and U3_RX pads connect to the VDD_IOD power rail instead of the VDD_IOA power rail. This only affects backward compatibility on existing LPC3180 projects that use a 1.8 V supply for domain VDD_IO1828, the input voltage range on the U3_RX pin and the output voltage of the U3_TX pin will change from 1.8 V to 3 V.

8. The bootloader software BootID has changed from 0x34 to 0x35. This may effect software that checks the BootID version. Version 0x35 of the bootloader code should not change the execution requirements of customer code, with the exception of the check for the value of the BootID itself.
9. The new 3180/01 expands the voltage domains to support a wider range of supply voltages. In general, most I/O pins and the external memory interface can now operate in either a 1.8 V or 3 V (3.3 V Typical, 3.6 V Max) range. See Table 15 for specific details.

Table 15. Power domain comparison LPC3180 to LPC3180/01

3180 Symbol	3180/01 Symbol	Pin
VDD_IO1828	VDD_IOA	This I/O voltage domain is a name change only. The 1.8 V or 3 V power supply for the I/O pins in this domain may operate from either a 1.8 V range or a 3 V range
VDD1828	VDD_IOB	This I/O voltage domain is a name change only. The 1.8 V or 3 V power supply for the I/O pins in this domain may operate from either a 1.8 V range or a 3 V range.
VDD_IO18	VDD_IOC	This I/O voltage domain extends the 1.8 V power supply for I/O pins that operate only at a 1.8 V range. The new range is extended to accept a 3 V power supply. These I/O pins may now operate in either a 1.8 V range or a 3 V range.
VDD_IO28	VDD_IOD	This I/O voltage domain extends the 3 V power supply for I/O pins that operate only at a 3 V range. The new range is extended to accept a 1.8 V power supply. These I/O pins may now operate in either a 1.8 V range or a 3 V range.
VDD_SDRAM18	VDD_EMC	This external Memory domain expands the 1.8 V power supply for the SDRAM controller block to accept a 3 V power supply. The SDRAM pins may now operate in either a 1.8 V range or a 3 V range.
VDD28	-	This domain no longer exists, all LPC3180 pins are no connects in the LPC3180/01
VDD12 VDD_CORE12 VDD_COREFXD12 VDD_OSC12 VDD_PLL397_12 VDD_PLLHCLK_12 VDD_PLLUSB_12 VDD_RTC12 VDD_RTCCORE12 VDD_RTCOSC12	VDD12 VDD_CORE12 VDD_COREFXD12 VDD_OSC12 VDD_PLL397_12 VDD_PLLHCLK_12 VDD_PLLUSB_12 VDD_RTC12 VDD_RTCCORE12 VDD_RTCOSC12	1.2 V power supply. There was no change to these voltage domains

11.2 Power, Ground and Internally connected Pins

There are pin name changes between the LPC3180 and LPC3180/01, Table 16 provides a pin by pin comparison showing the name changes for the power, ground and internally connected pins.

Table 16. Pin comparison 3180 to 3180/01 (power, ground, and internally connected)

3180 Symbol	3180/01 Symbol	Pin	Type	3180 Description
VDD12	VDD12	B14	I	1.2 V power supply for various internal functional blocks that are not included with VDD_CORE or VDD_COREFXD
VDD12	n.c.[1]	A21, B19	I	1.2 V power supply for various internal functional blocks that are not included with VDD_CORE or VDD_COREFXD
VDD_AD28	VDD_AD28	D24, E21	I	3.0 V power supply and positive reference voltage for the ADC
VDD_CORE12_01 to VDD_CORE12_03, VDD_CORE12_05 to VDD_CORE12_08	VDD_CORE12_01 to VDD_CORE12_03, VDD_CORE12_05 to VDD_CORE12_08	AA2, D6, K21, L3, AA12, AB6, AB18	I	1.2 V core main power supply for the CPU and other core logic; this voltage may be reduced to 0.9 V when the core is running at or below 13 MHz; the HIGHCORE pin may be used to signal this condition to an external voltage switch
VDD_COREFXD12_01, VDD_COREFXD12_02	VDD_COREFXD12_01, VDD_COREFXD12_02	C10, D18	I	1.2 V core secondary power supply voltage for the CPU and other core logic; this supply cannot be reduced in the same manner as the VDD_CORE12 supply
VDD1828	VDD_IOB[4]	AA4	I	1.8 V or 3.0 V power supply for I/O pins that may operate from either a 1.8 V range or a 3 V range
VDD1828	n.c.[1]	AD4	I	1.8 V or 3.0 V power supply for I/O pins that may operate from either a 1.8 V range or a 3 V range
VDD_IO1828_01 to VDD_IO1828_02	VDD_IOA[3]	B7, B4	I	1.8 V or 3.0 V power supply for I/O pins that may operate from either a 1.8 V range or a 3 V range
VDD_IO18_01 to VDD_IO18_04	VDD_IOC[5]	AA19, AA15, AB11, AC7	I	1.8 V power supply for I/O pins that operate only from a 1.8 V range
VDD_IO28_01 to VDD_IO28_02	VDD_IOD[6]	U4, G4,	I	3.0 V power supply for I/O pins that operate only from a 3 V range
VDD28	n.c.[1]	D14, A16, A17, C17, A19	I	3.0 V power supply for I/O pins that operate only from a 3 V range
VDD_OSC12	VDD_OSC12	D20	I	1.2 V power supply for the main oscillator
VDD_PLL397_12	VDD_PLL397_12	C22	I	1.2 V power supply for the 397x PLL
VDD_PLLHCLK_12	VDD_PLLHCLK_12	A22	I	1.2 V power supply for the HCLK PLL
VDD_PLLUSB_12	VDD_PLLUSB_12	B22	I	1.2 V power supply for the USB PLL
VDD_RTC12	VDD_RTC12	C12	I	1.2 V power supply for the RTC block
VDD_RTCCORE12	VDD_RTCCORE12	C11	I	1.2 V power supply for the RTC block
VDD_RTCOSC12	VDD_RTCOSC12	C14	I	1.2 V power supply for the 32 kHz RTC oscillator
VDD_SDRAM18_01 to VDD_SDRAM18_09	VDD_RAM[7]	G21, F22, J22, K22, P22, U22, Y21, AC24, AA20	I	1.8 V power supply for the SDRAM controller block
VSS	VSS_RAM	AD11, C19	I	ground for various internal logic blocks that are not included with VDD_CORE or VDD_COREFXD.
VSS	VSS_IOB	AB5	I	ground for various internal logic blocks that are not included with VDD_CORE or VDD_COREFXD.

Table 16. Pin comparison 3180 to 3180/01 (power, ground, and internally connected) *...continued*

3180 Symbol	3180/01 Symbol	Pin	Type	3180 Description
VSS	VSS	AC2, AC3, AC4		
VSS	n.c.[1]	B16, D15, AC11, AB2, AD1, AD5, AC5, AA6, AC6, AD3, AB4, C9, A9, A8, C8, D11, B11, B15, A15, W4, C16, D17, A20,	I	ground for various internal logic blocks that are not included with VDD_CORE or VDD_COREFXD.
VSS_AD	VSS_AD	D22	I	ground for the ADC; this should nominally be the same voltage as VSS, but should be isolated to minimize noise and conversion error
VSS_CORE_01 to VSS_CORE_09	VSS_CORE_01 to VSS_CORE_09	C20, D8, D16, J4, R3, R21, AA5, AA10, AB17	I	ground for the core logic functions
VSS_IO1828_01	VSS_IOD	D4	I	ground for I/O pins that may operate from either a 1.8 V range or a 3 V range
VSS_IO1828_02	VSS_IOA	A10	I	ground for I/O pins that may operate from either a 1.8 V range or a 3 V range
VSS_IO18_01, VSS_IO18_02, VSS_IO18_04	VSS_IOC	AC16, AD15, AB8	I	ground for I/O pins that operate only from a 1.8 V range
VSS_IO18_03	n.c.[1]	AC12	I	ground for I/O pins that operate only from a 1.8 V range
VSS_IO28_01 to VSS_IO28_03	VSS_IOD	E3, F1, N3	I	ground for I/O pins that operate only from a 3 V range
VSS_OSC	VSS_OSC	B21	I	ground for the main oscillator
VSS_PLL397	VSS_PLL397	C23	I	ground for the 397x PLL
VSS_PLLHCLK	VSS_PLLHCLK	D19	I	ground for the HCLK PLL
VSS_PLLUSB	VSS_PLLUSB	B20	I	ground for the USB PLL
VSS_RTCCORE	VSS_RTCCORE	B13	I	ground for the RTC block
VSS_RTCOSC	VSS_RTCOSC	C13	I	ground for the 32 kHz RTC oscillator

Table 16. Pin comparison 3180 to 3180/01 (power, ground, and internally connected) *…continued*

3180 Symbol	3180/01 Symbol	Pin	Type	3180 Description
VSS_SDRAM_01 to VSS_SDRAM_9	VSS_RAM	F23, G22, J23, M21, N22, R22, W22, AA22, AB21	I	ground for the SDRAM controller block
VSS_SDRAM_10	n.c.[1]	AA18	I	ground for the SDRAM controller block
i.c.[2]	n.c[1]	A18, B17, B18, C18, U1, AD2, AA13, AD16, AB16, AA14, AC14, AB15, AD14, AC13, AB14, AD13, AB13, AD12, H2, G1, G2, H4, D21, B24, A24, C15		internally connected

[1] n.c. means not connected.

[2] These pins are connected internally and must be left unconnected in an application.

[3] VDD_IOA is a voltage domain name change only the 1.8 V or 3 V power supply for the I/O pins in this domain that may operate from either a 1.8 V range or a 3 V range.

[4] VDD_IOB is a voltage domain name change only the 1.8 V or 3 V power supply for the I/O pins in this domain that may operate from either a 1.8 V range or a 3 V range .

[5] The VDD_IOC voltage domain extends the 1.8 V power supply for I/O pins that operate only at a 1.8 V range. The new range is extended to accept a 3 V power supply. These I/O pins may now operate in either a 1.8 V range or a 3 V range.

[6] The VDD_IOD voltage domain extends the 3 V power supply for I/O pins that operate only at a 3 V range. The new range is extended to accept a 1.8 V power supply. These I/O pins may now operate in either a 1.8 V range or a 3 V range.

[7] The VDD_RAM voltage domain expands the 1.8 V power supply for the SDRAM controller block to accept a 3 V power supply. The SDRAM pins may now operate in either a 1.8 V range or a 3 V range.

12. Abbreviations

Table 17. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CISC	Complex Instruction Set Computer
DDR	Double Data Rate
DMA	Direct Memory Access
DSP	Digital Signal Processing
FAB	Fast Access Bus
FIFO	First In, First Out
FIQ	Fast Interrupt Request
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
IRQ	Interrupt Request
MAC	Multiply-Accumulate
MMU	Memory Management Unit
OHCI	Open Host Controller Interface
OTG	On-The-Go
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RC	Resistor-Capacitor
SDR	Single Data Rate
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

13. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC3180_01_1	<tbd>	Preliminary data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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