Si570/Si571

10 MHz to 1.4 GHz I²C Programmable XO/VCXO

Features

- Any programmable output frequencies from 10 to 945 MHz and select frequencies to 1.4 GHz
- I²C serial interface
- 3rd generation DSPLL® with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available LVPECL, CMOS, LVDS, and CML outputs
- Industry-standard 5x7 mm package
- Pb-free/RoHS-compliant
- 1.8, 2.5, or 3.3 V supply

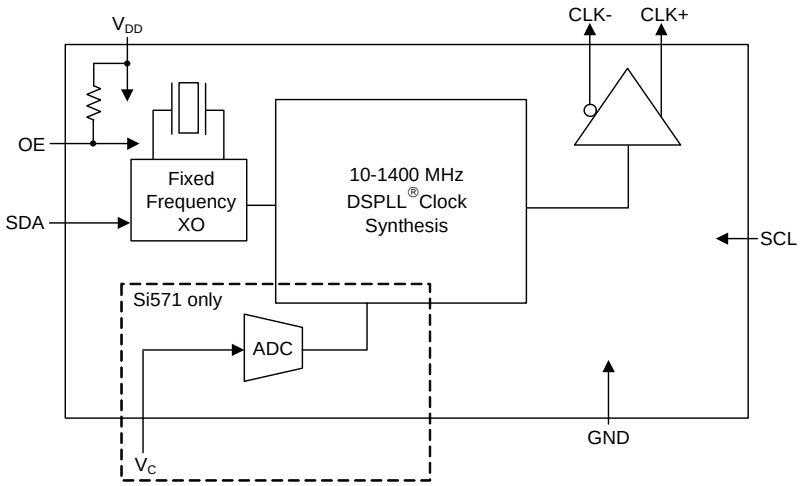
Applications

- SONET/SDH
- xDSL
- 10 GbE LAN/WAN
- Low-jitter clock generation
- Optical modules
- Clock and data recovery

Description

The Si570 XO/Si571 VCXO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low-jitter clock at any frequency. The Si570/Si571 are user-programmable to any output frequency from 10 to 945 MHz and select frequencies to 1400 MHz with <1 ppb resolution. The device is programmed via an I²C serial interface. Unlike traditional XO/VCXOs where a different crystal is required for each output frequency, the Si57x uses one fixed-frequency crystal and a DSPLL clock synthesis IC to provide any-frequency operation. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low-jitter clocks in noisy environments typically found in communication systems.

Functional Block Diagram



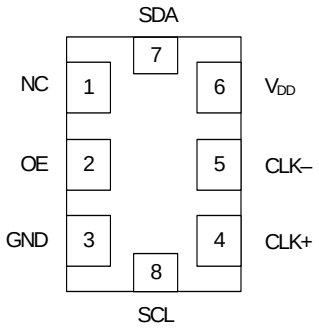
Ordering Information:

See page 24.

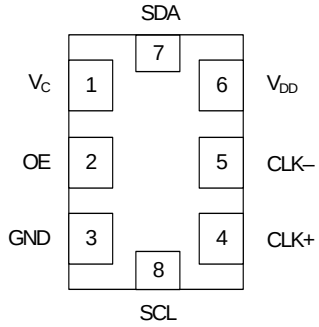
Pin Assignments:

See page 23.

(Top View)



Si570



Si571

TABLE OF CONTENTS

Section **Page**

1. Detailed Block Diagrams

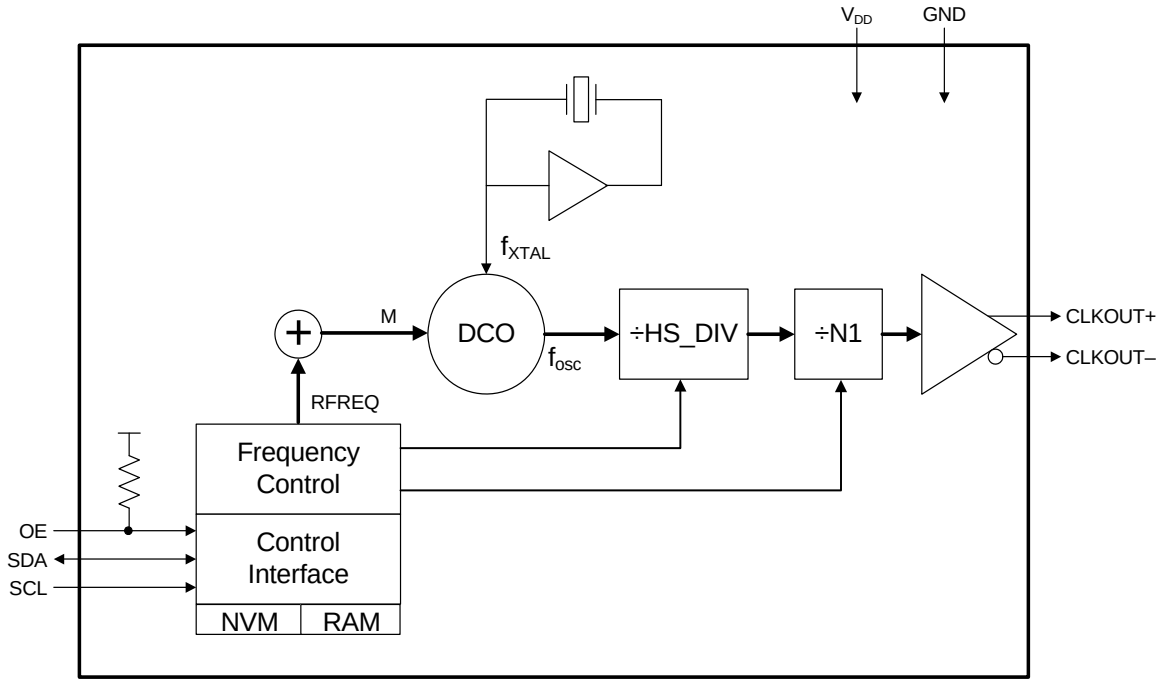


Figure 1. Si570 Detailed Block Diagram

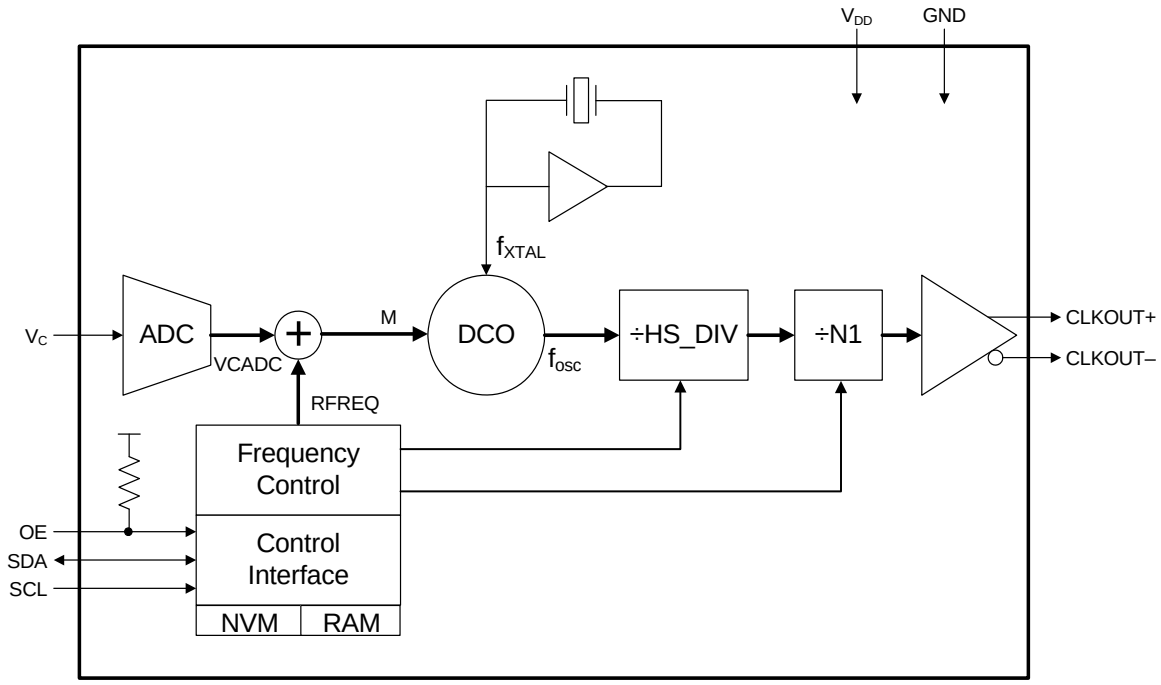


Figure 2. Si571 Detailed Block Diagram

2. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I_{DD}	Output enabled LVPECL CML LVDS CMOS	 — — — —	 120 108 99 90	 130 117 108 98	mA
		TriState mode	—	60	75	
Output Enable (OE)[2], Serial Data (SDA), Serial Clock (SCL)		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	
Operating Temperature Range	T_A		–40	—	85	ºC

Notes:
1. Selectable parameter specified by part number. See Section "7. Ordering Information" on page 24 for further details.
2. OE pin includes a 17 kΩ pullup resistor to V_{DD}. See “7.Ordering Information”.

Table 2. V_C Control Voltage Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope[1,2,3]	K_V	V_C 10 to 90% of V_{DD}	—	33 45 90 135 180 356	—	ppm/V
Control Voltage Linearity[4]	L_{VC}	BSL	–5	±1	+5	%
		Incremental	–10	±5	+10	
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V_C Input Impedance	Z_{VC}		500	—	—	kΩ
Nominal Control Voltage	V_{CNOM}	@ f_O	—	$V_{DD}/2$	—	V
Control Voltage Tuning Range	V_C		0		V_{DD}	V

Notes:
1. Positive slope; selectable option by part number. See "7. Ordering Information" on page 24.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application’s minimum APR requirements. See “AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)” for more information.
3. K_V variation is ±10% of typical values.
4. BSL determined from deviation from best straight line fit with V_C ranging from 10 to 90% of V_{DD}. Incremental slope is determined with V_C ranging from 10 to 90% of V_{DD}.

Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Programmable Frequency Range[1,2,3]	f_O	LVPECL/LVDS/CML	10	—	1417.5	MHz
		CMOS	10	—	160	
Temperature Stability[1,4]		T_A = –40 to +85 ºC	–20 –50 –100	— — —	+20 +50 +100	ppm
Initial Accuracy			—	1.5	—	ppm
Aging	f_a	Frequency drift over first year	—	—	±3	ppm
		Frequency drift over 15 year life	—	—	±10	ppm
Total Stability		Temp stability = ±20 ppm	—	—	±31.5	ppm
		Temp stability = ±50 ppm	—	—	±61.5	ppm
Absolute Pull Range[1,4]	APR		±25	—	±375	ppm
Power up Time[5]	t_{OSC}		—	—	10	ms

Notes:

1. See Section "7. Ordering Information" on page 24 for further details.
2. Specified at time of order by part number. Three speed grades available:
   Grade A covers 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417.5 MHz.
   Grade B covers 10 to 810 MHz.
   Grade C covers 10 to 280 MHz.
3. Nominal output frequency set by V_{CNOM} = 1/2 x V_{DD}.
4. Selectable parameter specified by part number.
5. Time from power up or tristate mode to f_O.

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option[1]	V_O	mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option[2]	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option[2]	V_O	2.5/3.3 V option mid-level	—	V_{DD} – 1.30	—	V
		1.8 V option mid-level	—	V_{DD} – 0.36	—	V_{PP}
	V_{OD}	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V
		1.8 V option swing (diff)	0.35	0.425	0.50	V_{PP}
CMOS Output Option[3]	V_{OH}	I_{OH} = 32 mA	0.8 x V_{DD}	—	V_{DD}	V
	V_{OL}	I_{OL} = 32 mA	—	—	0.4	
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C_L = 15 pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V_{DD} – 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V_{DD}/2	45	—	55	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).
3. C_L = 15 pF

Table 5. CLK± Output Phase Jitter (Si570)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)* for $F_{OUT} \geq$ 500 MHz	ϕ_J	12 kHz to 20 MHz (OC-48)	—	0.25	0.40	ps
		50 kHz to 80 MHz (OC-192)	—	0.26	0.37	
Phase Jitter (RMS)* for F_{OUT} of 125 to 500 MHz	ϕ_J	12 kHz to 20 MHz (OC-48)	—	0.36	0.50	ps
		50 kHz to 20 MHz (OC-192)	—	0.34	0.42	
Phase Jitter (RMS) for F_{OUT} of 10 to 160 MHz CMOS Output Only	ϕ_J	12 kHz to 20 MHz (OC-48)	—	0.62	—	ps
		50 kHz to 80 MHz (OC-192)	—	0.61	—	

***Note:** Refer to AN256 for further information.

Table 6. CLK± Output Phase Jitter (Si571)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2,3] for $F_{OUT} \geq 500$ MHz	ϕ_J	Kv = 33 ppm/V				ps
		12 kHz to 20 MHz (OC-48)	—	0.26	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 45 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.27	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 90 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.32	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 135 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.40	—	
		50 kHz to 80 MHz (OC-192)	—	0.27	—	
		Kv = 180 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.49	—	
		50 kHz to 80 MHz (OC-192)	—	0.28	—	
		Kv = 356 ppm/V				
		12 kHz to 20 MHz (OC-48)	—	0.87	—	
		50 kHz to 80 MHz (OC-192)	—	0.33	—	

Notes:

1. Differential Modes: LVPECL/LVDS/CML. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Single ended mode: CMOS. Refer to the following application notes for further information:
   "AN255: Replacing 622 MHz VCSO Device with the Si55x VCXO"
   "AN256: Integrated Phase Noise"
   "AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)"

Table 6. CLK± Output Phase Jitter (Si571) (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[2,4] for F_{OUT} 10 to 160 MHz CMOS Output Only	ϕ_J	Kv = 33 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.63 0.62	 — —	ps
		Kv = 45 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.63 0.62	 — —	
		Kv = 90 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.67 0.66	 — —	
		Kv = 135 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.74 0.72	 — —	
		Kv = 180 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.83 0.8	 — —	
		Kv = 356 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 1.26 1.2	 — —	

Notes:

1. Differential Modes: LVPECL/LVDS/CML. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Single ended mode: CMOS. Refer to the following application notes for further information:
   "AN255: Replacing 622 MHz VCSO Device with the Si55x VCXO"
   "AN256: Integrated Phase Noise"
   "AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)"

Table 6. CLK± Output Phase Jitter (Si571) (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2,3] for F_{OUT} of 125 to 500 MHz	ϕ_J	Kv = 33 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.37 0.33	 — —	ps
		Kv = 45 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.37 0.33	 — —	
		Kv = 90 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.43 0.34	 — —	
		Kv = 135 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.50 0.34	 — —	
		Kv = 180 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.59 0.35	 — —	
		Kv = 356 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 1.00 0.39	 — —	

Notes:

1. Differential Modes: LVPECL/LVDS/CML. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Single ended mode: CMOS. Refer to the following application notes for further information:
   "AN255: Replacing 622 MHz VCSO Device with the Si55x VCXO"
   "AN256: Integrated Phase Noise"
   "AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)"

Table 7. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J_{PER}	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	

***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to "AN279: Estimating Period Jitter from Phase Noise" for further information.

Table 8. Typical CLK± Output Phase Noise (Si570)

Offset Frequency (f)	120.00 MHz LVDS	156.25 MHz LVPECL	622.08 MHz LVPECL	Units
100 Hz	–112	–105	–97	dBc/Hz
1 kHz	–122	–122	–107	
10 kHz	–132	–128	–116	
100 kHz	–137	–135	–121	
1 MHz	–144	–144	–134	
10 MHz	–150	–147	–146	
100 MHz	n/a	n/a	–148	

Table 9. Typical CLK± Output Phase Noise (Si571)

Offset Frequency (f)	74.25 MHz 90 ppm/V LVPECL	491.52 MHz 45 ppm/V LVPECL	622.08 MHz 135 ppm/V LVPECL	Units
100 Hz	–87	–75	–65	dBc/Hz
1 kHz	–114	–100	–90	
10 kHz	–132	–116	–109	
100 kHz	–142	–124	–121	
1 MHz	–148	–135	–134	
10 MHz	–150	–146	–146	
100 MHz	n/a	–147	–147	

Table 10. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage, 1.8 V Option	V_{DD}	–0.5 to +1.9	V
Supply Voltage, 2.5/3.3 V Option	V_{DD}	–0.5 to +3.8	V
Input Voltage	V_I	–0.5 to V_{DD} + 0.3	V
Storage Temperature	T_S	–55 to +125	ºC
ESD Sensitivity (HBM, per JESD22-A114)	ESD	>2500	V
Soldering Temperature (lead-free profile)	T_{PEAK}	260	ºC
Soldering Temperature Time @ T_{PEAK} (lead-free profile)	t_P	20–40	seconds

Notes:
1. Stresses beyond the absolute maximum ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at www.silabs.com/VCXO for further information, including soldering profiles.

Table 11. Environmental Compliance

The Si570/571 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross & Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036

Table 12. Programming Constraints and Timing

(V_{DD} = 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequency Range	CKO_F	HS_DIV x N1 > = 6	10	—	945	MHz
		HS_DIV x N1 = 5 N1 = 1	970	—	1134	MHz
		HS_DIV = 4 N1 = 1	1.2125	—	1.4175	GHz
Frequency Reprogramming Resolution	M_{RES}	114.285 MHz	—	0.09	—	ppb
Internal Oscillator Frequency	f_{OSC}		4850	—	5670	MHz
Internal Crystal Frequency Accuracy	f_{XTAL}	Maximum variation is ±2000 ppm	—	114.285	—	MHz
Delta Frequency for Continuous Output		From center frequency	–3500	—	+3500	ppm
Unfreeze to NewFreq Timeout					10	ms
Settling time for small frequency change		<±3500 ppm from center frequency	—	—	100	µs
Settling time for large frequency change		>±3500 ppm from center frequency after setting NewFreq bit	—	—	10	ms

3. Functional Description

The Si570 XO and the Si571 VCXO are low-jitter oscillators ideally suited for applications requiring programmable frequencies. The Si57x can be programmed to generate virtually any output clock in the range of 10 MHz to 1.4 GHz. Output jitter performance exceeds the strict requirements of high-speed communication systems including OC-192/STM-64 and 10 Gigabit Ethernet (10 GbE).

The Si57x consists of a digitally-controlled oscillator (DCO) based on Silicon Laboratories' third-generation DSPLL technology, which is driven by an internal fixed-frequency crystal reference.

The device's default output frequency is set at the factory and can be reprogrammed through the two-wire I^2C serial port. Once the device is powered down, it will return to its factory-set default output frequency.

While the Si570 outputs a fixed frequency, the Si571 has a pullable output frequency using the voltage control input pin. This makes the Si571 an ideal choice for high-performance, low-jitter, phase-locked loops.

3.1. Programming a New Output Frequency

The output frequency (f_{out}) is determined by programming the DCO frequency (f_{DCO}) and the device's output dividers (HS_DIV, N1). The output frequency is calculated using the following equation:

$$f_{out} = \frac{f_{DCO}}{\text{Output Dividers}} = \frac{f_{XTAL} \times RFREQ}{HSDIV \times N1}$$

The DCO frequency is adjustable in the range of 4.85 to 5.67 GHz by setting the high-resolution 38-bit fractional multiplier (RFREQ). The DCO frequency is the product of the internal fixed-frequency crystal (f_{XTAL}) and RFREQ.

The 38-bit resolution of RFREQ allows the DCO frequency to have a programmable frequency resolution of 0.09 ppb.

As shown in Figure 3, the device allows reprogramming of the DCO frequency up to ±3500 ppm from the center frequency configuration without interruption to the output clock. Changes greater than the ±3500 ppm window will cause the device to recalibrate its internal tuning circuitry, forcing the output clock to momentarily stop and start at any arbitrary point during a clock cycle. This re-calibration process establishes a new center frequency and can take up to 10 ms. Circuitry receiving a clock from the Si57x device that is sensitive to glitches or runt pulses may have to be reset once the recalibration process is complete.

3.1.1. Reconfiguring the Output Clock for a Small Change in Frequency

For output changes less than ±3500 ppm from the center frequency configuration, the DCO frequency is the only value that needs reprogramming. Since $f_{DCO} = f_{XTAL}$ x RFREQ, and that f_{XTAL} is fixed, changing the DCO frequency is as simple as reconfiguring the RFREQ value as outlined below:

1. Using the serial port, read the current RFREQ value (registers 0x08–0x12).
2. Calculate the new value of RFREQ given the change in frequency.

$$RFREQ_{new} = RFREQ_{current} \times \frac{f_{out\_new}}{f_{out\_current}}$$

3. Using the serial port, write the new RFREQ value (registers 0x08—0x12).

Example:

An Si570 generating a 148.35 MHz clock must be reconfigured "on-the-fly" to generate a 148.5 MHz clock. This represents a change of +1011.122 ppm, which is well within the ±3500 ppm window.

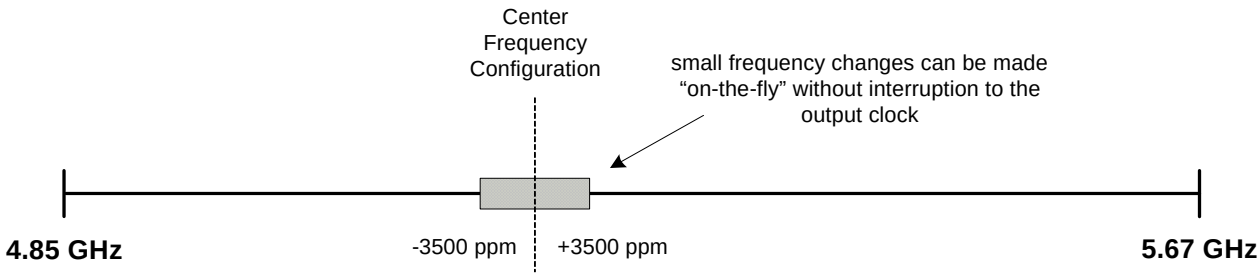


Figure 3. DCO Frequency Range

A typical frequency configuration for this example:

$RFREQ_{current}$ = 0x2EBB04CE0

$F_{out\_current}$ = 148.35 MHz

F_{out_new} = 148.50 MHz

Calculate $RFREQ_{new}$ to change the output frequency from 148.35 MHz to 148.5 MHz:

$$RFREQ_{new} = 0x2EBB04CE0 \times \frac{148.50\ MHz}{148.35\ MHz}$$

$$= 0x2EC71D666$$

Note that performing calculations with RFREQ requires a minimum of 38-bit arithmetic precision.

Even relatively small changes in output frequency may require writing more than 1 RFREQ register. Such multi-register RFREQ writes can impact the output clock frequency on a register-by-register basis during updating.

Interim changes to the output clock during RFREQ writes can be prevented by using the following procedure:

1. Freeze the “M” value (Set Register 135 bit 5 = 1).
2. Write the new frequency configuration (RFREQ).
3. Unfreeze the “M” value (Set Register 135 bit 5 = 0)

3.1.2. Reconfiguring the Output Clock for Large Changes in Output Frequency

For output frequency changes outside of ±3500 ppm from the center frequency, it is likely that both the DCO frequency and the output dividers need to be reprogrammed. Note that changing the DCO frequency outside of the ±3500 ppm window will cause the output to momentarily stop and restart at any arbitrary point in a clock cycle. Devices sensitive to glitches or runt pulses may have to be reset once reconfiguration is complete.

The process for reconfiguring the output frequency outside of a ±3500 ppm window is shown below:

1. Using the serial port, read the current values for RFREQ, HSDIV, and N1.
2. Calculate f_{XTAL} for the device. Note that because of slight variations of the internal crystal frequency from one device to another, each device may have a different RFREQ value or possibly even different HSDIV or N1 values to maintain the same output frequency. It is necessary to calculate f_{XTAL} for each device.

$$f_{XTAL} = \frac{F_{out} \times HSDIV \times N1}{RFREQ}$$

Once f_{XTAL} has been determined, new values for RFREQ, HSDIV, and N1 are calculated to generate a new output frequency (f_{out_new}). New values can be calculated manually or with the Si57x-EVB software, which provides a user-friendly application to help find the optimum values.

The first step in manually calculating the frequency configuration is to determine new frequency divider values (HSDIV, N1). Given the desired output frequency (fout_new), find the frequency divider values that will keep the DCO oscillation frequency in the range of 4.85 to 5.67 GHz.

$$f_{DCO\_new} = f_{out\_new} \times HSDIV_{new} \times N1_{new}$$

Valid values of HSDIV are 4, 5, 6, 7, 9 or 11. N1 can be selected as 1 or any even number up to 128 (i.e. 1, 2, 4, 6, 8, 10 … 128). To help minimize the device's power consumption, the divider values should be selected to keep the DCO's oscillation frequency as low as possible. The lowest value of N1 with the highest value of HS_DIV also results in the best power savings.

Once HS_DIV and N1 have been determined, the next step is to calculate the reference frequency multiplier (RFREQ).

$$RFREQ_{new} = \frac{f_{DCO\_new}}{f_{XTAL}}$$

RFREQ is programmable as a 38-bit binary fractional frequency multiplier with the first 10 most significant bits (MSBs) representing the integer portion of the multiplier, and the 28 least significant bits (LSBs) representing the fractional portion.

Before entering a fractional number into the RFREQ register, it must be converted to a 38-bit integer using a bitwise left shift operation by 28 bits, which effectively multiplies RFREQ by 2^{28}.

Example:

RFREQ = 46.043042064d

Multiply RFREQ by 2^{28} = 12359584992.1

Discard the fractional portion = 12359584992

Convert to hexadecimal = 02E0B04CE0h

In the example above, the multiplication operation requires 38-bit precision. If 38-bit arithmetic precision is not available, then the fractional portion can be separated from the integer and shifted to the left by 28-bits. The result is concatenated with the integer portion to form a full 38-bit word. An example of this operation is shown in Figure 4.

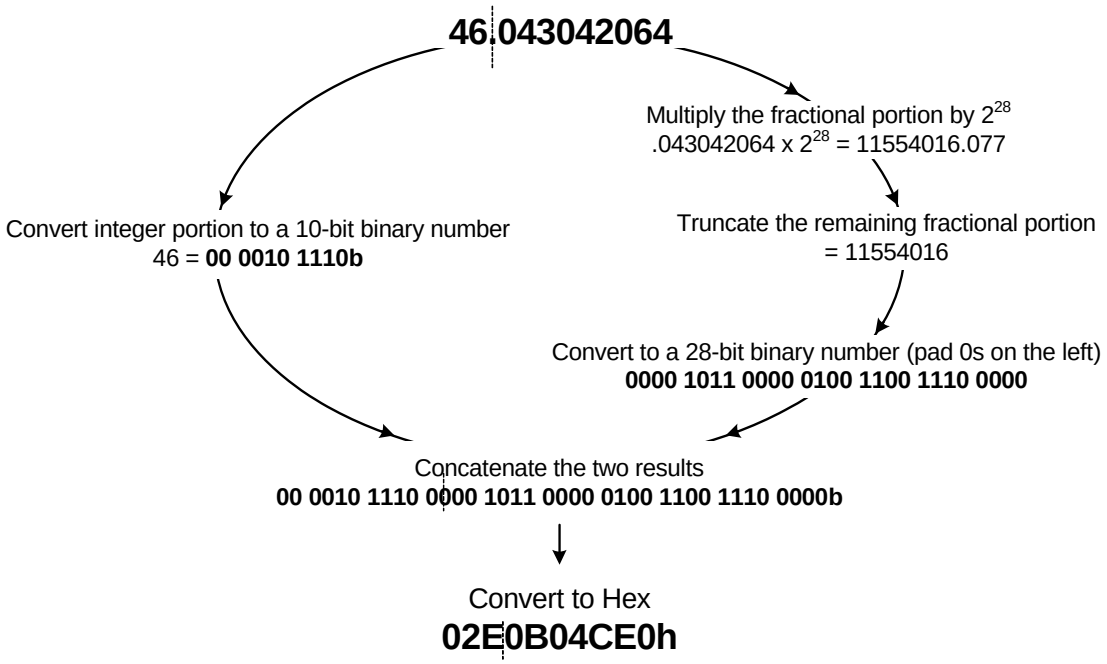


Figure 4. Example of RFREQ Decimal to Hexadecimal Conversion

Once the new values for RFREQ, HSDIV, and N1 are determined, they can be written directly into the device from the serial port using the following procedure:

1. Freeze the DCO (bit 4 of Register 137)
2. Write the new frequency configuration (RFREQ, HS_DIV, N1)
3. Unfreeze the DCO and assert the NewFreq bit (bit 6 of Register 135) within the maximum Unfreeze to NewFreq Timeout specified in Table 12, "Programming Constraints and Timing," on page 12.

The process of freezing and unfreezing the DCO will cause the output clock to momentarily stop and start at any arbitrary point during a clock cycle. This process can take up to 10 ms. Circuitry that is sensitive to glitches or runt pulses may have to be reset after the new frequency configuration is written.

Example:

An Si570 generating 156.25 MHz must be re-configured to generate a 161.1328125 MHz clock (156.25 MHz x 66/64). This frequency change is greater than ±3500 ppm.

f_{out} = 156.25 MHz

Read the current values for RFREQ, HS_DIV, N1:

$RFREQ_{current}$ = 0x2BC011EB8h = 11744124600d,
11744124600d x 2^{28} = 43.7502734363d

HS_DIV = 4

N1 = 8

Calculate f_{XTAL}, $f_{DCO\_current}$

$$f_{DCO\_current} = f_{out} \times HSDV \times N1 = 5.000000000\ GHz$$

$$f_{XTAL} = \frac{f_{DCO\_current}}{RFREQ_{current}} = 114.285\ MHz$$

Given f_{out_new} = 161.1328125 MHz, choose output dividers that will keep f_{DCO} within the range of 4.85 to 5.67 GHz. In this case, keeping the same output dividers will still keep f_{DCO} within its range limits:

$$f_{DCO\_new} = f_{out\_new} \times HSDV_{new} \times N1_{new}$$

$$= 161.1328125\ MHz \times 4 \times 8 = 5.156250000\ GHz$$

Calculate the new value of RFREQ given the new DCO frequency:

$$RFREQ_{new} = \frac{f_{DCO\_new}}{f_{XTAL}} = 45.11746934$$

$$= 0x2D1E12788$$

3.2. I²C Interface

The control interface to the Si570 is an I²C-compatible 2-wire bus for bidirectional communication. The bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL). Both lines must be connected to the positive supply via an external pullup.Fast mode operation is supported for transfer rates up to 400 kbps as specified in the I²C-Bus Specification standard.

Figure 5 shows the command format for both read and write access. Data is always sent MSB. Data length is 1 byte. Read and write commands support 1 or more data bytes as illustrated. The master must send a Not Acknowledge and a Stop after the last read data byte to terminate the read command. The timing specifications and timing diagram for the I2C bus can be found in the I2C-Bus Specification standard (fast mode operation). The device I2C address is specified in the part number.

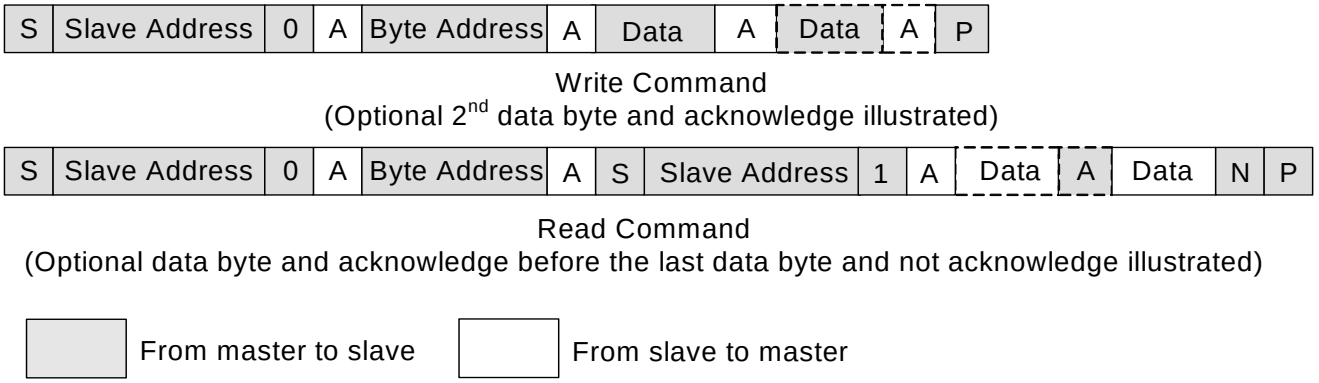


Figure 5. I²C Command Format

4. Serial Port Registers

Note: Any register not listed here is reserved and must not be written. All bits are R/W unless otherwise noted.

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7	High Speed/ N1 Dividers	HS_DIV[2:0]			N1[6:2]				
8	Reference Frequency	N1[1:0]		RFREQ[37:32]					
9	Reference Frequency	RFREQ[31:24]							
10	Reference Frequency	RFREQ[23:16]							
11	Reference Frequency	RFREQ[15:8]							
12	Reference Frequency	RFREQ[7:0]							
135	Reset/Freeze/ Memory Control	RST_REG	NewFreq	Freeze M	Freeze VCADC				RECALL
137	Freeze DCO				Freeze DCO				

Register 7. High Speed/N1 Dividers

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HS_DIV[2:0]			N1[6:2]				
Type	R/W			R/W				

Bit	Name	Function
7:5	HS_DIV[2:0]	**DCO High Speed Divider.** Sets value for high speed divider that takes the DCO output f_{OSC} as its clock input. 000 = 4 001 = 5 010 = 6 011 = 7 100 = Not used. 101 = 9 110 = Not used. 111 = 11
4:0	N1[6:2]	**CLKOUT Output Divider.** Sets value for CLKOUT output divider. Allowed values are [1] and [2, 4, 6, ..., 2^7]. Illegal odd divider values will be rounded up to the nearest even value. The value for the N1 register can be calculated by taking the divider ratio minus one. For example, to divide by 10, write 0001001 (9 decimal) to the N1 registers. 0000000 = 1 1111111 = 2^7

Register 8. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1[1:0]		RFREQ[37:32]					
Type	R/W		R/W					

Bit	Name	Function
7:6	N1[1:0]	**CLKOUT Output Divider.** Sets value for CLKOUT output divider. Allowed values are [1, 2, 4, 6, ..., 2^7]. Illegal odd divider values will be rounded up to the nearest even value. The value for the N1 register can be calculated by taking the divider ratio minus one. For example, to divide by 10, write 0001001 (9 decimal) to the N1 registers. 0000000 = 1 1111111 = 2^7
5:0	RFREQ[37:32]	**Reference Frequency.** Frequency control input to DCO.

Register 9. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[31:24]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[31:24]	**Reference Frequency.** Frequency control input to DCO.

Register 10. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[23:16]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[23:16]	**Reference Frequency.** Frequency control input to DCO.

Register 11. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[15:8]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[15:8]	**Reference Frequency.** Frequency control input to DCO.

Register 12. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[7:0]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[7:0]	**Reference Frequency.** Frequency control input to DCO.

Register 135. Reset/Freeze/Memory Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RST_REG	NewFreq	Freeze M	Freeze VCADC	N/A			RECALL
Type	R/W	R/W	R/W	R/W	R/W			R/W

Reset settings = 00xx xx00

Bit	Name	Function
7	RST_REG	**Internal Reset.** 0 = Normal operation. 1 = Reset of all internal logic. Output tristated during reset. Upon completion of internal logic reset, RST_REG is internally reset to zero. **Note:** Asserting RST_REG will interrupt the I^2C state machine. It is not the recommended approach for starting from initial conditions.
6	NewFreq	**New frequency Applied.** Alerts the DSPLL that a new frequency configuration has been applied. This bit will clear itself when the new frequency is applied.
5	Freeze M	**Freezes the M Control Word.** Prevents interim frequency changes when writing RFREQ registers.
4	Freeze VCADC	**Freezes the VC ADC Output Word.** May be used to hold the nominal output frequency of an Si571.
3:1	N/A	**Always zero.**
0	RECALL	**Recall NVM into RAM.** 0 = No operation. 1 = Write NVM bits into RAM. Bit is internally reset following completion of operation. **Note:** Asserting RECALL reloads the NVM contents in to the operating registers without interrupting the I^2C state machine. It is the recommended approach for starting from initial conditions.

Register 137. Freeze DCO

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				Freeze DCO				
Type	R/W							

Reset settings = 00xx xx00

Bit	Name	Function
7:5	Reserved	
4	Freeze DCO	**Freeze DCO.** Freezes the DSPLL so the frequency configuration can be modified.
3:0	Reserved	

5. Si570 (XO) Pin Descriptions

(Top View)

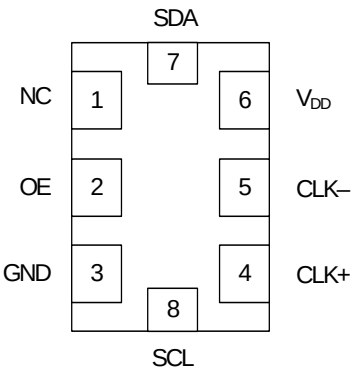


Table 13. Si570 Pin Descriptions

Pin	Name	Type	Function
1	NC	N/A	No Connect. Make no external connection to this pin.
2	OE	Input	Output Enable: See "7. Ordering Information" on page 24.
3	GND	Ground	Electrical and Case Ground.
4	CLK+	Output	Oscillator Output.
5	CLK– (NC for CMOS*)	Output (N/A for CMOS*)	Complementary Output. (NC for CMOS*).
6	V_{DD}	Power	Power Supply Voltage.
7	SDA	Bidirectional Open Drain	I^2C Serial Data.
8	SCL	Input	I^2C Serial Clock.
***Note:** CMOS output option only: make no external connection to this pin.			

6. Si571 (VCXO) Pin Descriptions

(Top View)

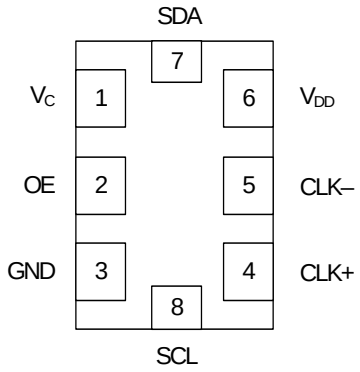


Table 14. Si571 Pin Descriptions

Pin	Name	Type	Function
1	V_C	Analog Input	Control Voltage
2	OE	Input	Output Enable: See "7. Ordering Information" on page 24.
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK– (NC for CMOS*)	Output (N/A for CMOS*)	Complementary Output. (NC for CMOS*).
6	V_{DD}	Power	Power Supply Voltage
7	SDA	Bidirectional Open Drain	I^2C Serial Data
8	SCL	Input	I^2C Serial Clock
***Note:** CMOS output option only: make no external connection to this pin.			

7. Ordering Information

The Si570/Si571 supports a wide variety of options including frequency range, start-up frequency, temperature stability, tuning slope, output format, and V_{DD}. Specific device configurations are programmed into the Si570/Si571 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si570/Si571 XO/VCXO series is supplied in an industry-standard, RoHS compliant, 8-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.

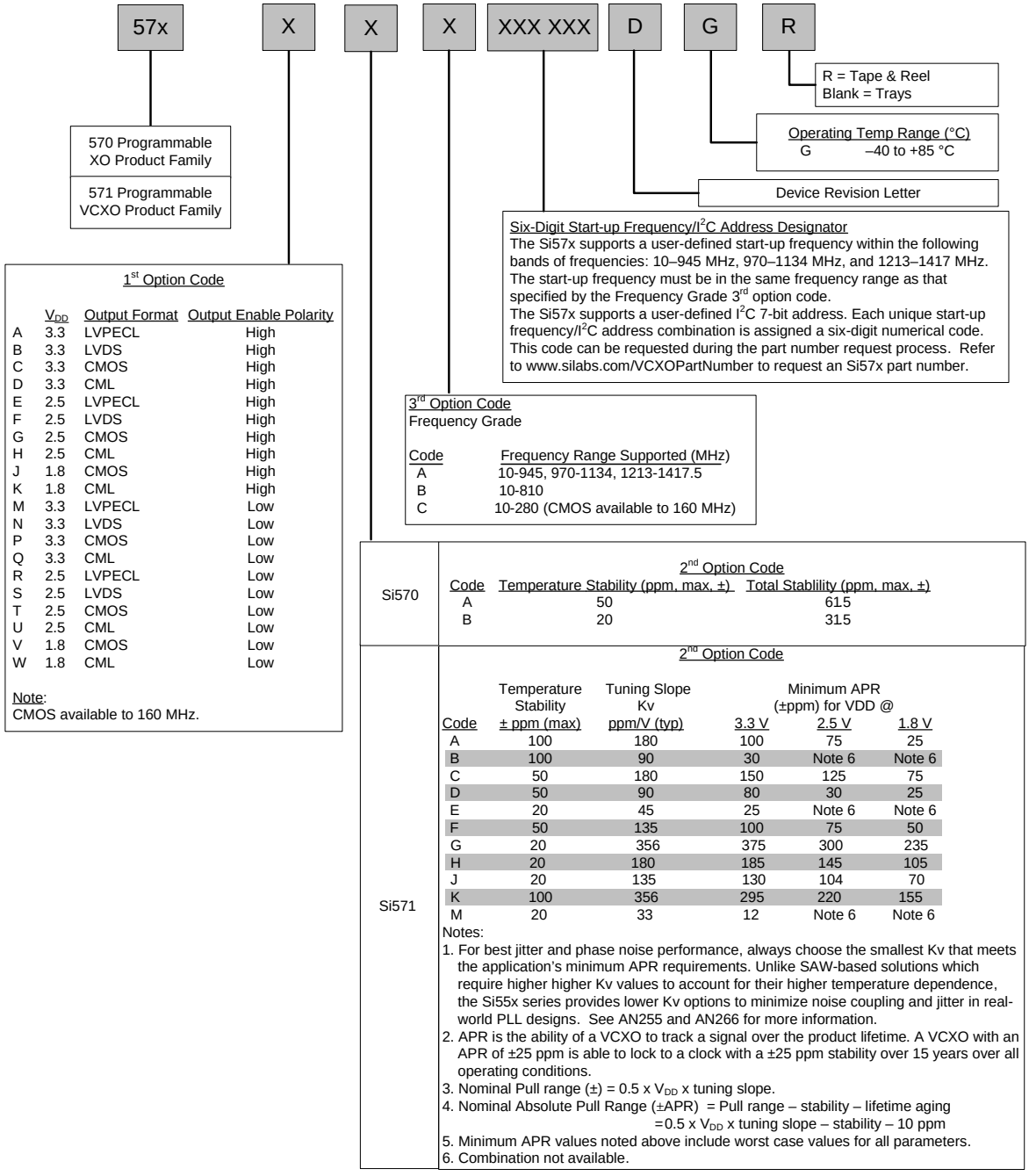


Figure 6. Part Number Convention

8. Si57x Mark Specification

Figure 7 illustrates the mark specification for the Si57x. Table 15 lists the line information.

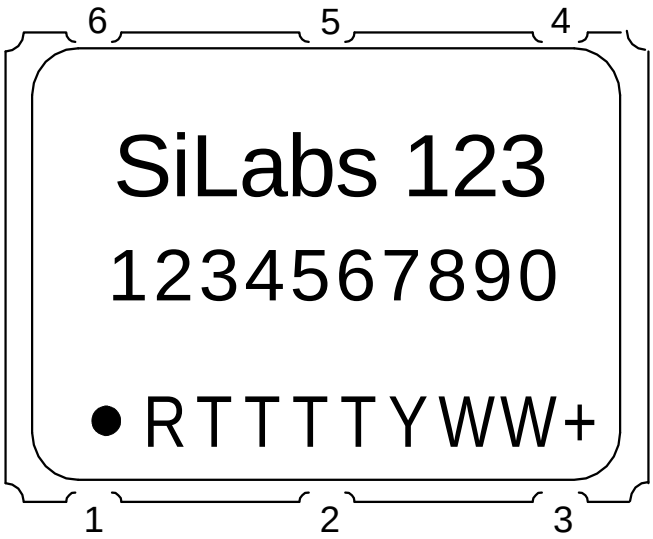


Figure 7. Mark Specification

Table 15. Si57x Top Mark Description

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 5xx (First 3 characters in part number)
2	1–10	Si570, Si571: Option1 + Option2 + Option3 + ConfigNum(6) + Temp
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

9. Outline Diagram and Suggested Pad Layout

Figure 8 illustrates the package details for the Si570/Si571. Table 16 lists the values for the dimensions shown in the illustration.

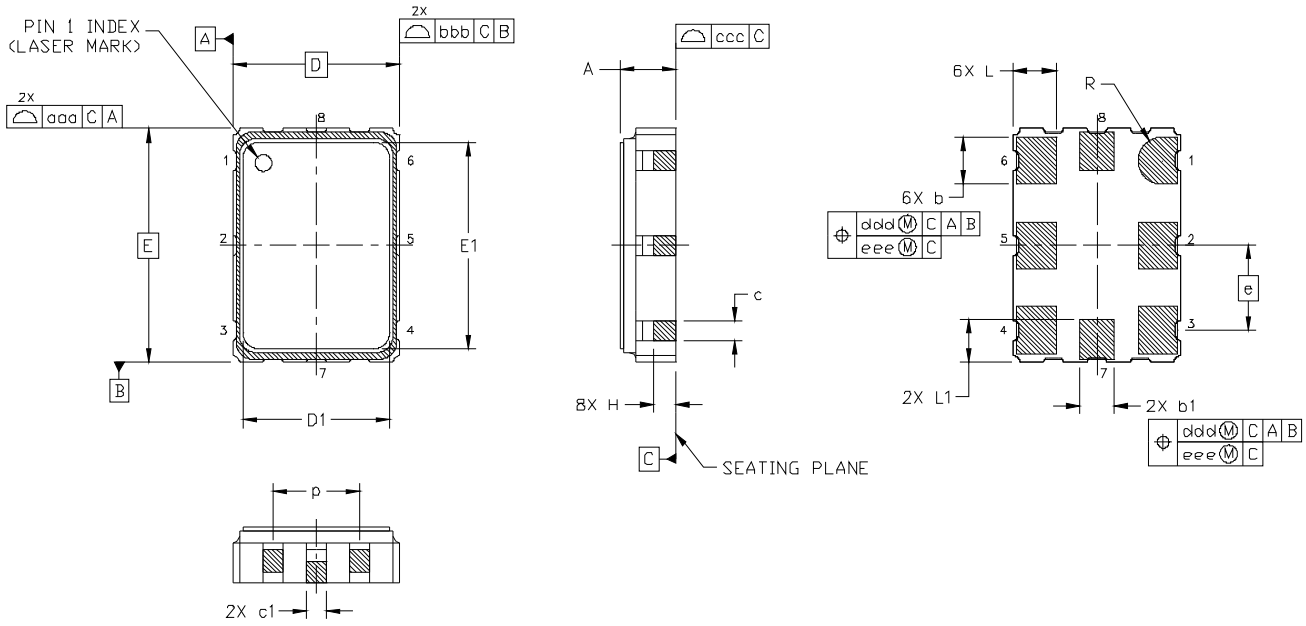


Figure 8. Si570/Si571 Outline Diagram

Table 16. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
b1	0.90	1.00	1.10
c	0.50	0.60	0.70
c1	0.30	—	0.60
D		5.00 BSC	
D1	4.30	4.40	4.50
e		2.54 BSC	
E		7.00 BSC	
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	1.07	1.17	1.27
p	1.80	—	2.60
R		0.70 REF	
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10
eee	—	—	0.05

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

10. 8-Pin PCB Land Pattern

Figure 9 illustrates the 8-pin PCB land pattern for the Si570/Si571. Table 17 lists the values for the dimensions shown in the illustration.

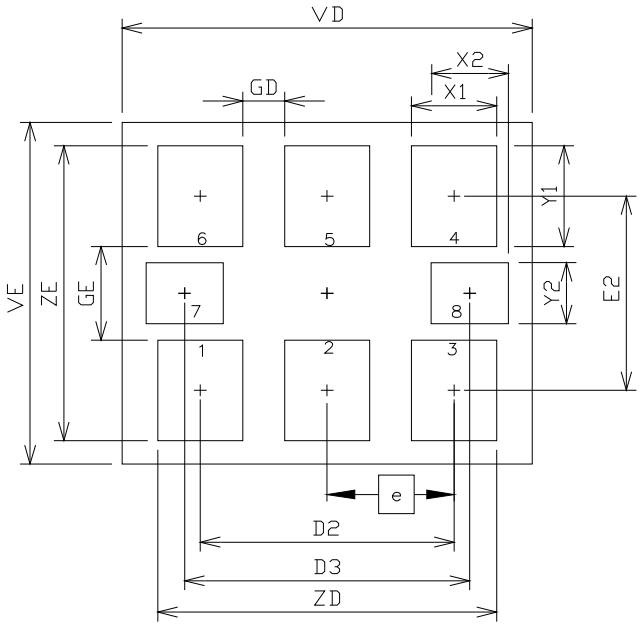


Figure 9. Si570/Si571 PCB Land Pattern

Table 17. PCB Land Pattern Dimensions (mm)

Dimension	Min	Max
D2	5.08 REF	
D3	5.705 REF	
e	2.54 BSC	
E2	4.20 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X1	1.70 TYP	
X2	1.545 TYP	
Y1	2.15 REF	
Y2	1.3 REF	
ZD	—	6.78
ZE	—	6.30

Note:

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design follows IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

Document Change List

Revision 0.2 to Revision 0.3

- Updated Table 1, “Recommended Operating Conditions,” on page 5.
  - Device maintains stable operation over –40 to +85 ºC operating temperature range.
  - Supply current specifications updated.
- Updated Table 4, “CLK± Output Levels and Symmetry,” on page 7.
  - Updated LVDS differential peak-peak swing specifications.
- Updated Table 5, “CLK± Output Phase Jitter (Si570),” on page 7.
- Updated Table 6, “CLK± Output Phase Jitter (Si571),” on page 8.
- Updated Table 7, “CLK± Output Period Jitter,” on page 10.
  - Revised period jitter specifications.
- Updated Table 10, “Absolute Maximum Ratings,” on page 11 to reflect the soldering temperature time at 260 ºC is 20–40 sec per JEDEC J-STD-020C.
- Updated device programming procedure in Section "3.2.3. Programming Procedure" on page 12.
- Updated "7. Ordering Information" on page 24.
  - Changed ordering instructions to revision D.
- Added "8. Si57x Mark Specification" on page 25.

Revision 0.3 to Revision 0.31

- Updated "3.2.3. Programming Procedure" on page 12.
  - Corrected Step 6 to read “bit 4”.
- Corrected Freeze DCO bit location in Register 137 to bit 4 on pages 14 and 18.

Revision 0.31 to Revision 1.0

- Updated " Functional Block Diagram" on page 1.
- Updated Figure 1, “Si570 Detailed Block Diagram,” on page 4.
- Updated Figure 2, “Si571 Detailed Block Diagram,” on page 4.
- Updated Figure 6, “Part Number Convention,” on page 24.
- Updated Table 1, “Recommended Operating Conditions,” on page 5.
- Updated Table 3, “CLK± Output Frequency Characteristics,” on page 6.
- Updated Table 6, “CLK± Output Phase Jitter (Si571),” on page 8.
- Updated Table 12, “Programming Constraints and Timing,” on page 12.
- Updated Table 12, “Programming Constraints and Timing,” on page 12.
- Updated "3. Functional Description" on page 13.
- Updated "3.1. Programming a New Output Frequency" on page 13.
- Updated "3.1.1. Reconfiguring the Output Clock for a Small Change in Frequency" on page 13.
- Updated "3.1.2. Reconfiguring the Output Clock for Large Changes in Output Frequency" on page 14.
- Updated “7.Ordering Information”.
  - Updated Figure 6, “Part Number Convention,” on page 24.

Revision 1.0 to Revision 1.1

- Restored programming constraint information on page 15 and in Table 12, page 12.
- Clarified NC (No Connect) pin designations in Tables 13–14 on pages 22–23.

Revision 1.1 to Revision 1.2

- Replaced “Unfreeze to Newfreq Delay” with the clearer terminology “Unfreeze to Newfreq Timeout” on page 15 and in Table 12 on page 12.
- Added Freeze M procedure on page 14 for preventing output clock changes during small frequency change multi-register RFREQ writes.
- Added Freeze M, Freeze VCADC, and RST_REG versus RECALL information to Register 135 references in "4. Serial Port Registers" on pages 17 and 20.
- Updated Figure 8 and Table 16 on page 26 to include production test sidepads. This change is for reference only as the sidepads are raised above the seating plane and do not impact PCB layout.
- Corrected errors in Table 11 on page 12.

NOTES:

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