MSC8156ADS Reference Manual

MSC8156 Application Development System
Supports MSC8156 DSP Family
and MSC8256 DSP Family
rev Pilot

MSC8156ADSRM
Rev 2.1, April 2010

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Contents

General Information 1

The MSC8156 application development system (MSC8156ADS) is a complete debugging environment intended for engineers developing applications for the MSC8156 family and MSC8256 family of Freescale digital signal processors (DSPs).

- The MSC8156 and MSC8256 devices are highly integrated DSP processors that contains six StarCore SC3850 DSP subsystems (48 GMACS at 1 GHz).
- The MSC8154 and MSC8254 devices contain four StarCore SC3850 DSP subsystems (32 GMACS at 1 GHz).
- The MSC8252 device contains two StarCore SC3850 DSP subsystems (16 GMACS at 1 GHz).
- The MSC8251 device contains one StarCore SC3850 DSP subsystem (8 GMACS at 1 GHz).

Each SC3850 subsystem includes:

- SC3850 DSP core
- 32 KB DCache
- 32 KB ICache
- 512 KB unified L2 cache/M2 shared memory
- Memory management unit (MMU)
- Write queue
- Dual timers
- Extended programmable interrupt controller (EPIC) that supports 256 interrupts
- Real-time debug support and a profiling unit (DPU)

In addition, the MSC8156 family and MSC8256 devices each contain:

- 1 MB of M3 shared memory
- Two DDR2/DDR3 memory controllers with a 64-bit data rate up to 800 M
- High speed serial interface (HSSI) with two 4-channel SerDes port that multiplex:
  - Two serial RapidIO® 1x/4x interface at 1.25/2.5/3.125 GBaud over LYNX1,2 ports.
  - PCI express 1x/2x/4x at 2.5 GBaud over LYNX2 port
  - Two SGMII interfaces
- Dual RISC QUICC Engine™ subsystem that supports
  - 2 RGMII Ethernet ports with direct PHYs or 2 SGMII ports through the HSSI
  - SPI
- Four 1024-channel 400 Mbps time-division multiplexing (TDM) interfaces
- UART
- I^2C
- Multi-Protocol Baseband Accelerator (MAPLE-B) (MSC8156 family only)

The MSC8156 DSP family targets high-bandwidth highly computational DSP applications and is optimized for 3GPP, TD-SCDMA, 3G-LTE, and WiMAX applications. The MSC8256 DSP family targets high-performance medical, aerospace and defense, and advanced test and measurement markets. The MSC8156ADS is intended to serve as a platform for software and hardware development in the MSC8156 DSP and MSC8256 DSP family environment. On-board resources and the associated debugger enable developers to perform a variety of tasks, including:

- Download and run code
- Set breakpoints
- Display memory and registers
- Connect proprietary hardware via an expansion connector

The board (shown in **Figure 1-1**) can function in a stand-alone configuration or as an AMC board in the MicroTCA system.

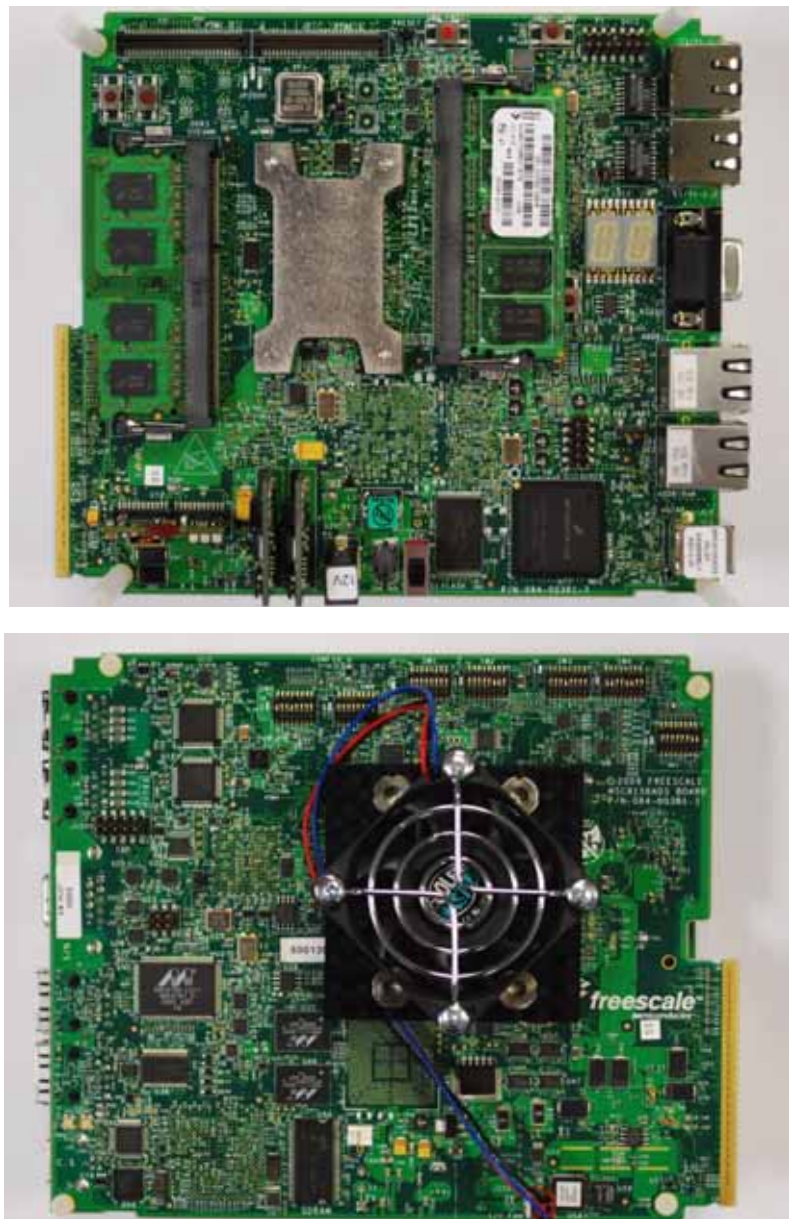


Figure 1-1. MSC8156ADS Double AMC Form Factor Board

1.1 Working Configurations

The MSC8156ADS supports two working configuration:

- *Stand-Alone Mode*. The MSC8156ADS can run in a stand-alone mode like other application development systems, with direct connections to debuggers, power supply, and other external connections.
- *AMC Mode*. The MSC8156ADS is inserted in a standard MicroTCA backplane that allows testing of the high-speed serial RapidIO and PCI Express ports against other platforms. By using a proprietary B2B adaptor card, the MSC8156 can work with a second MSC8156 device on an additional ADS board. The AMC edge connector carries all interface signal at high speed between the devices. The ADS is compatible with standard MicroTCA chassis, such as a Schroff or TUNDRA development platform.

1.2 MSC8156ADS Feature List

The ADS is based on a MSC8156 DSP family single chip.

- Includes an MSC8156 DSP. Supports application development for the MSC8154, MSC8156, MSC8251, MSC8252, MSC8254, or MSC8156 DSPs running at up to 1000 MHz with core voltages of 1 V.
- Power can be applied to six cores for the MSC8156/MSC8256 or one/two/four core devices including the MSC8254/MSC8251/MSC8252/MSC8254.
- The first DDR controller (DDRC1) is configured in DDR2 mode: 200-pin SOCDIMM with ECC support, 64-bit @ 800 Mbps 1 GB of memory.
- The second DDR controller (DDRC2) is configured in DDR3 mode: 204-pin SODIMM, 64-bit @ 800 Mbps, No-ECC, 1 GB of memory.
- The DDR3-to-DDR2 interposer (from the MPC8569MDS project) allows you to verify DDR2 module on the MSC8156 DDRC2 controller.
- The DSP RGMII (at ports GE1 and GE2) connects to two single Marvell 88E1111 GETH PHYs for regular board configuration.
- A Marvel 10-port SGMII switch 88E6182 links the DSP SGMII lines to 2xRJ-45 copper connectors and to the 1000Base-X over AMC MicroTCA connector ports 0 and 2.
- Pericom PI2DBS212ZHE Diff Signal Switch parts support programmable SerDes lines multiplexing to AMC edge connector or to the SGMII the switch.
- Two Dallas E1/T1 framers connect to the four DSP TDM ports.
- The PTMC pinout complies with the PT3MC standard (TDM). P1 and P3 connectors carry MSC8156 GPIO and TDM signals.
- The DSP configuration and boot support includes the following:
  - Reset Configuration Reset Source three bits set by appropriate DIP-switches.
  - Parallel load of Programmable Reset Configuration Word from FPGA registers sampled previously from DIP-Switch array.
  - Serial configuration and boot from a large (64 KB) or small (1 KB) I^2C EEPROM.
  - Boot from Serial 8 MB SPI Flash.
  - Boot from communications ports: from SerDes-serial RapidIO interface or from Ethernet—SGMII or RGMII ports.
- Two available debug interfaces:
  - On-board USB TAP controller (eUTAP)
  - OnCE 14-pin header for any external TAP controller
- FPGA logic:
  - Board Control and Status Register (BCSR)
  - JTAG controller allows full board programming
  - Multiplexing of JTAG source signals

  - I^2C controllers: Master and Slave
  - MII controller to program RGMII PHY
  - SPI controller
  - Boot Sequencer configures ADS peripherals for Boot over Ethernet.
  - Generation of TDM clock and sync
  - Two-digit, 14-segment LED display provides current board settings and core temperature
- 100 MHz clock oscillator for MSC8156 clock-in.
- An external pulse generator as clock source connects to the CLKIN connector. The MSC8156 clock output signal may be measured on CLKOUT test point.
- Can function in various main supply configurations (configurable via DIP switches or BCSR):
  - Stand-alone mode with an external power 12 VDC @ 5 A when S1 switch is “ON”.
  - As an AMC card in the microTCA system or interconnection with AMC-X-Over card. If the ADS is fed outside the S1 power switch should be “OFF”.
- Onboard power system comprises two regulator steps:
  - Primary power system is a Power-One Power Manager with 1.0 V POL regulator for MSC8156 loads: cores, MAPLE-B, and M3; 2.5 V for I/O; and 3.3 V for onboard peripherals.
  - DDR switching power supplies for DDRC1 and DDRC2 ports.
  - LDOs, for onboard peripherals, are fed from 2.5 V and 3.3 V POLs and 12 V input voltage.
  - Voltage supervisor monitors all the ADS power supply. Power Good (PG) signal and dedicated LED LD14 indicate power system status. Any failure causes to nPRST signal be low continuously.
- Push Buttons
  - Main Power-On-Reset (SW8)
  - Hard Reset (SW9)
  - Soft Reset (SW11)
  - NMI (SW10)
  - Scroll (SW12) to select display mode

1.3 MSC8156ADS Block Diagram

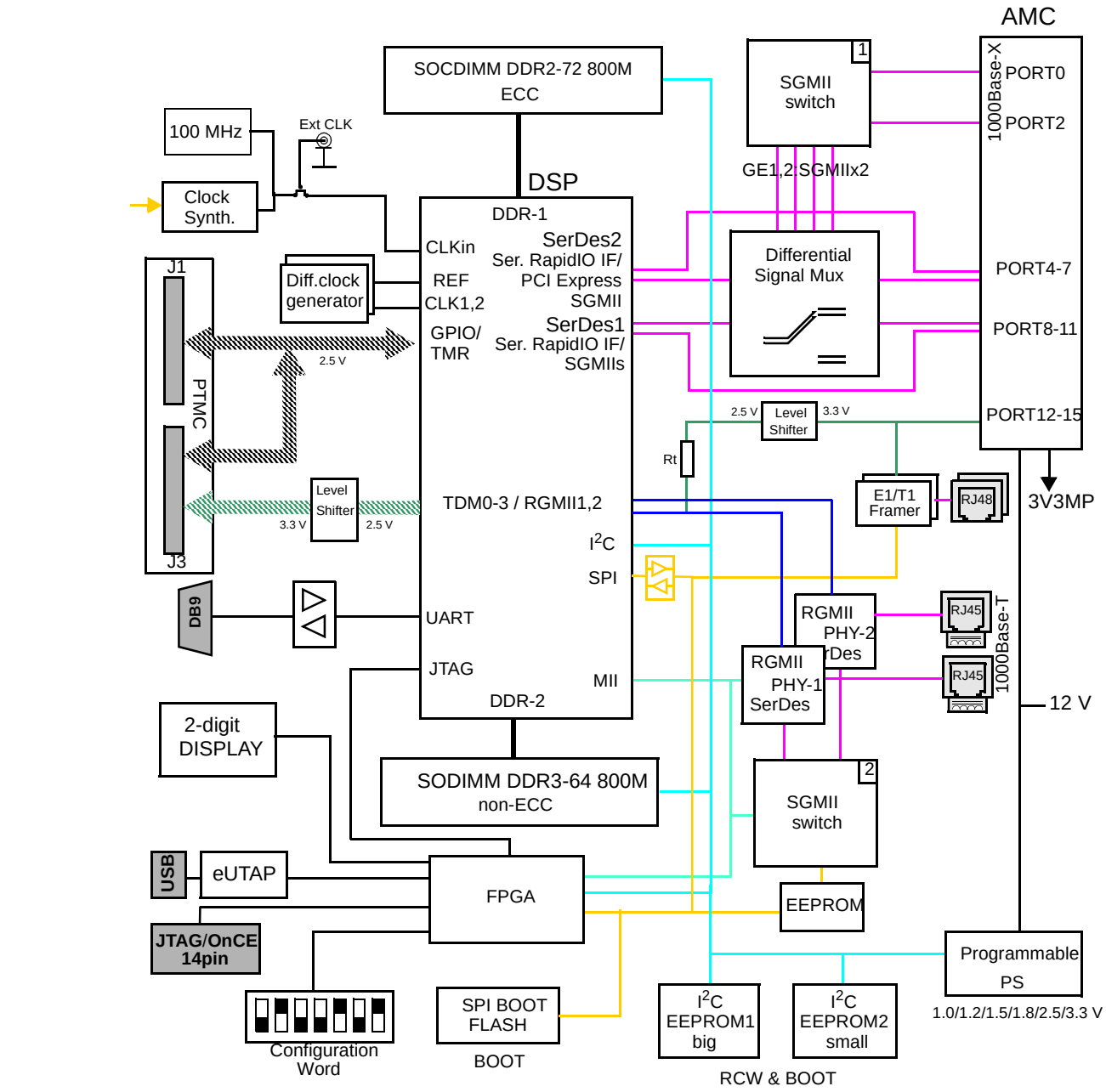


Figure 1-2. ADS Block Diagram

1.4 Definitions, Acronyms, and Abbreviations

ADS	Application Development System
AMC	Advanced Mezzanine Card
ATCA/microTCA/microTCA	Advanced (Micro) Telecommunications Computing Architecture
BCSR	Board Control and Status Register
BSP	Board Support Package
CS	Chip Select
CW	*Code Warrior*® IDE
DDR2, DDR3	Double Data Rate, or Double Data Rate SDRAM Type 2,3
DDR-1, DDR-2	The MSC8156 DDR Controller 1 and DDR Controller 2
DIP	Dual-In-Line Package.
DMA	Direct Memory Access
EEPROM	Electrical Erasable Programmable Memory
eUTAP	Embedded USB TAP Controller, populated on the ADS
FLASH	Non volatile reprogrammable memory.
FPGA	Field-Programmable Gate Array
GETH	Giga-bit Ethernet
I^2C	Philips Semi Serial Bus
ISP	In-Circuit Programming
JTAG	Joint Test Access Group
LED	Light Emitting Diode
lsb	least significant bit
CCSLLD	Low Level Debugger
LYNX1/LYNX2	SerDes ports of the MSC8156
MI/MII	Ethernet Management Interface
msb	most significant bit
OnCE	On-Chip Emulation Port
PC	IBM-compatible Personal Computer
PCIe	Experess Peripheral Components Interconnect
PHY	Physical Layer
POL	Point-of-Load DC-DC converter
PS, PSU	Power Supply Unit
RGMII	Reduced Gigabit Media Independent Interface
RCW(L,H)	Reset Configuration Word (Low/High)

SGMII	Serial Gigabit Media Independent Interface
SerDes	Serializer/Deserializer
SODIMM	Mini DIMM Form Factor
SOCDIMM	Mini DIMM Form Factor with ECC Support
SPD	Serial Present Detect
SPI	System Programming Interface
T1, E1	A time-division multiplexing protocols
TDM	Time-division multiplexing

1.5 Related Documentation

Freescale provides the following documentation with this kit:

- MSC8156ADS Hardware Getting Started Guide
- MSC8156ADS Reference Manual
- MSC8156ADS Using Code Warrior™ and MSC8156ADS Kit Configuration Guide

Specific device documentation for MSC8154, MSC8156, MSC8251, MSC8252, MSC8254, and MSC8256 can be obtained from the Freescale website (*www.freescale.com*), including the device technical data sheets and reference manuals.

1.6 Specifications

The MSC8156ADS specifications are given in **1-1**.

Table 1-1. MSC8156 ADS Specifications

Characteristics	Specifications
DSP	MSC8156 **Note:** See **Figure 2-18** for details on configuring the board for the MSC8156 versus the one/two/four core DSPs.
Power requirements	12 V @ 4 A (min.) external DC power supply for stand alone mode. **Note:** No extra power supply is required for AMC mode; power comes from the microTCA backplane.
Ambient temperature	0°C to 70°C
Storage temperature	–25°C to 85°C
Relative humidity	5% to 90% (non-condensing)
Dimensions according to Double-width AMC form factor (except the high):	Length: 148 mm Width: 181 mm Height: 27 mm with socket or 17.5 mm with soldered chip PCB Thickness: 1.6 mm
Operating frequency	Cores run up to 1.2 GHz @ 1V

Table 1-1. MSC8156 ADS Specifications (Continued)

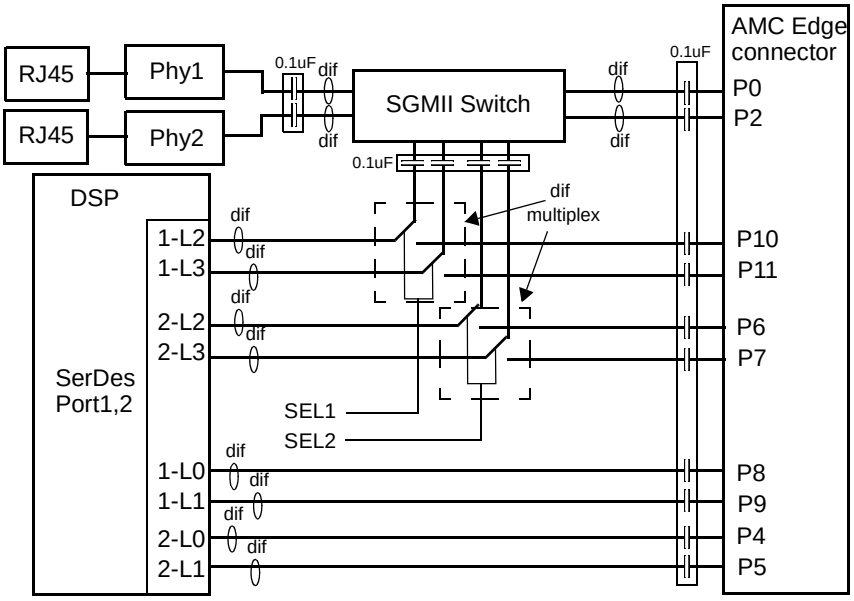
Characteristics		Specifications
Memory:	Internal: M2, M3, ICache, DCache	—
	DDR2 Module on DDR-1 port	1 GB space 64 bit wide + 8-bit ECC Memory Module in SOCDIMM200 form factor. Clock 400 MHz, Data rate 800 Mbps
	DDR3 Module on DDR-2 port	1 GB space 64-bit wide Memory Module in SODIMM204 form factor. Clock 400 MHz, Data rate 800 Mbps
	Serial: I^2C EEPROM SPI Flash memory	 64 kB and 1 Kb serial EEPROMs. 8 MB serial Flash for Program Code.
COM ports	Gigabit Ethernet	Two Gbps Ethernet Ports for RGMII (multiplexed with TDM ports) interface.
	TDM	Four TDM ports together support up to 1K time-slots for receive and 1K time-slots for transmit up to 256 PCM channels per link. TDM ports are present on AMC connector and on PTMC connectors J3. TDM lines are multiplexed with RGMII. Two E1/T1 Framers link to four TDM ports. **Note:** This interface uses a 2.5 V source and is not compatible with a 3.3 V interface.
	UART	Bit rate up to 6.25 Mbps. RS-232 transceiver allows data exchange at 115 Kbps. **Note:** This interface uses a 2.5 V source and is not compatible with a 3.3 V interface.
	I^2C	Compliant with standard. Running up to 400 Kbps
	SPI	Synchronous peripheral serial bus. Running up to 20 Mbps **Note:** This interface uses a 2.5 V source and is not compatible with a 3.3 V interface.
	SerDes ports 1,2	1x/4x serial RapidIO endpoint operates at 1.25, 2.5, or 3.125 Gbaud and complies with Specification 1.2. 1x/2x/4x PCI Express endpoint operates at 2.5 Gbaud and complies with Specification 1.0. SGMII at 1.25 GBaud.

Functional Description 2

2.1 SerDes Configuration

SerDes1 and SerDes2 of the MSC8156 family high speed serial interface (HSSI) are independent, configurable, multiprotocol four-lane serial ports. SerDes1 supports Serial RapidIO and SGMII ports; SerDes2 supports Serial RapidIO, SGMII, and PCI Express ports in different modes. The ADS supports all available MSC8156 family SerDes configurations. Refer to the *Device Specific Reference Manual* for details on multiplexing configuration.

The ADS links the MSC8156 family SerDes ports to the AMC ports. When the SerDes port is configured in SGMII mode, the differential signals go to the SGMII switch over the Pericom PI2DBS212ZHE 1:2 differential channel multiplexer/demultiplexer switch as shown on the **Figure 2-1**.



Note: Some configuration modes do not use all lanes. SGMII switch ports are configured for working lanes only. It's shown setting while SW5.2,3 SEL1 and SEL2 are OFF

Figure 2-1. SerDes Connection Scheme

The multiplexer is capable of data rates up to 1.8 GHz or 3.6 Gbps and is able to multiplex two differential pairs in two directions. DIP-switches SW5.2,3 SEL1 and SEL2 dispatch SerDes lanes. All SerDes lines have DC blocking capacitors 0.1 µF. Differential pairs are routed with 100 Ω impedance.

Table 2-1 summarizes the switch settings. Lanes 0 and 1 of the both SerDes ports are tied directly to MicroTCA AMC edge connector.

Table 2-1. Differential Signal Multiplexer Settings

Mode/ Multiplexed Port	Destination			
	2xPort x (2xSerDes)	2xSerDes Port1 + 2xSGMII Port2	2xSGMII Port1 + 2xSerDes Port2	2xPort x (2xSGMII)
SEL1	0	1	0	1
SEL2	0	0	1	1
SerDes1-Lane2	SSW Port 0	AMC Port 10	SSW Port 0	AMC Port 10
SerDes1-Lane3	SSW Port 1	AMC Port 11	SSW Port 1	AMC Port 11
SerDes2-Lane2	SSW Port 2	SSW Port 2	AMC Port 6	AMC Port 6
SerDes2-Lane3	SSW Port 3	SSW Port 3	AMC Port 7	AMC Port 7
Note: SSW denotes the SGMII switch.				

The predefined switch scheme is available for the hard reset configuration word (HRCW) loaded from a DIP-switch. The default setting from the factory selects the following configuration:

- SerDes1: Serial RapidIO interface is 4x at 3.125 Gbps.
- SerDes2: Serial RapidIO interface is 4x at 3.125 Gbps.
- Ethernet: two RGMII at 1 Gbps as 1000Base-X (over AMC) and 1000Base-T (over RJ-45)

The multiplexing selection can be changed “on the fly” by setting bits SEL1 and SEL2 in the BCSR10.0-1.

2.2 Gigabit Ethernet Ports

The MSC8156 has two gigabit Ethernet controllers (GE1 and GE2) that can be configured independently for RGMII or SGMII interface mode.

The RGMII mode supports a MAC-to-MAC connection using an RGMII switch and MAC-to-PHY. The standard ADS version does not contain the optional RGMII switch, instead it has 0 Ω resistors; see **Figure 2-2**. Low speed TDM bus peripherals, E1/T1 framers, are isolated from high-speed RGMII signals with serial 220 Ω resistors located close to the GE port pins. GETH PHYs transform the RGMII bus to a SGMII bus; this links the GETH PHYs with the SGMII switch.

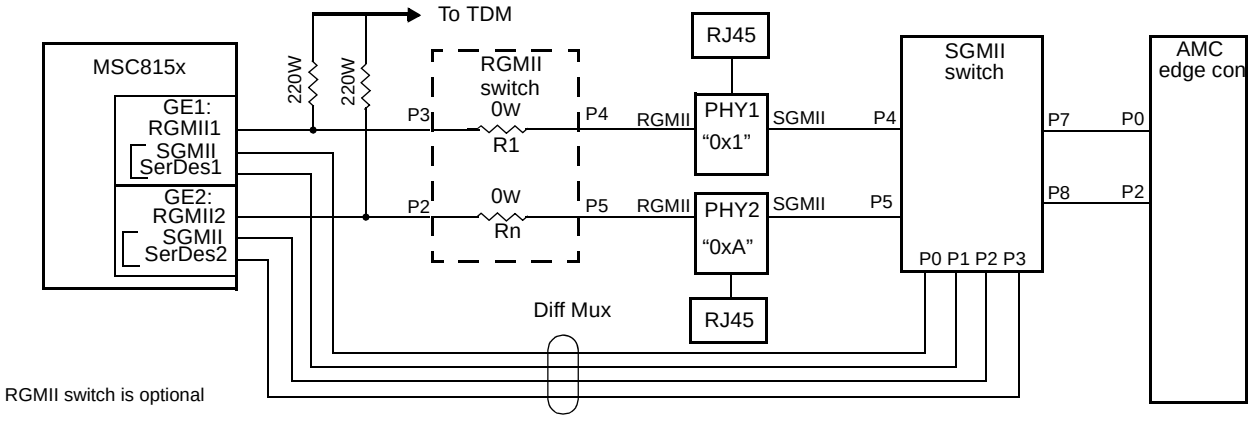


Figure 2-2. ADS Gigabit Ethernet Links

The second available GETH data path is provided over the SGMII interface. The MSC8156 family SGMII mode uses the SerDes interface available through the SerDes1,2 ports. The SGMII signals go to the Marvell 88E6182 SGMII switch over an analog differential multiplexer.

The clock buffer splits the PHY1-generated 125 MHz clock output signal between three destinations:

- RGMII switch
- MSC815x GE1 port
- MSC815x GE2 port

If RCW GE1 and GE2 bits are set low to select TDM I/F instead of RGMII I/F then the FPGA Boot Sequencer module programs RGMII PHYs in isolation mode and disables the clock buffer; this ensures proper operation of the MSC8156 family TDM bus.

2.2.1 RGMII Port: PHY

Two Marvell 88E1111 single GETH PHYs serve the MSC8156 family RGMII ports. The PHYs convert RGMII signals to analog SerDes or Base-T interfaces. The PHY for GE Port1 has MII bus address “0x1”; the GE Port2 uses “0xA”. The PHY is from the Alaska family which is compliant to the 10/100/1000 Base-T standard. It features:

- GMII/TBI/RGMII/RTBI and SGMII interfaces support
- Virtual Cable Tester
- Automatic MDI/MDIX crossover
- Low power

The hardware configuration mechanism allows to provide setup from programmable device (FPGA)

2.2.2 SGMII Port: Switch

The Marvell 88E6182 device integrates ten triple-speed SerDes ports providing non-blocking switching performance in all traffic environment. It may connect gluelessly to the Alaska 10/100/1000 ETH phy like 88E1111. Three ports support either SerDes (SGMII) or 1000Base-X interfaces for microTCA backplane.

The switch works in unmanaged or smart-managed applications. The ADS configuration supports unmanaged mode only. The device supports an external SPI serial EEPROM for programming its internal registers. An external SPI EPPROM saves the initial configuration and loads it to the switch after reset. The EEPROM is programmed from the MSC8156 if the switch stands in reset—bit SGMIIRST BCSR9.2.

The Management Interface bus accesses Switch internal registers or an external PHY. MDC buffers isolate MDC_DSP signals upon SRESET assertion. This enables the FPGA MII controller to act as Master on the Management Interface and configure GETH PHYs in RGMII mode.

2.2.3 Gigabit Ethernet Management Interface

There are three ADS Master management interfaces (MI):

- MSC8156 family GE ports with common MI
- SGMII switch
- FPGA MII controller

The MI bus switches U32,U33 TS3L110RGYR provide desired connection MI master device to the PHY, depend on chosen mode. **Figure 2-3** shows the MI bus connectivity for different Ethernet modes.

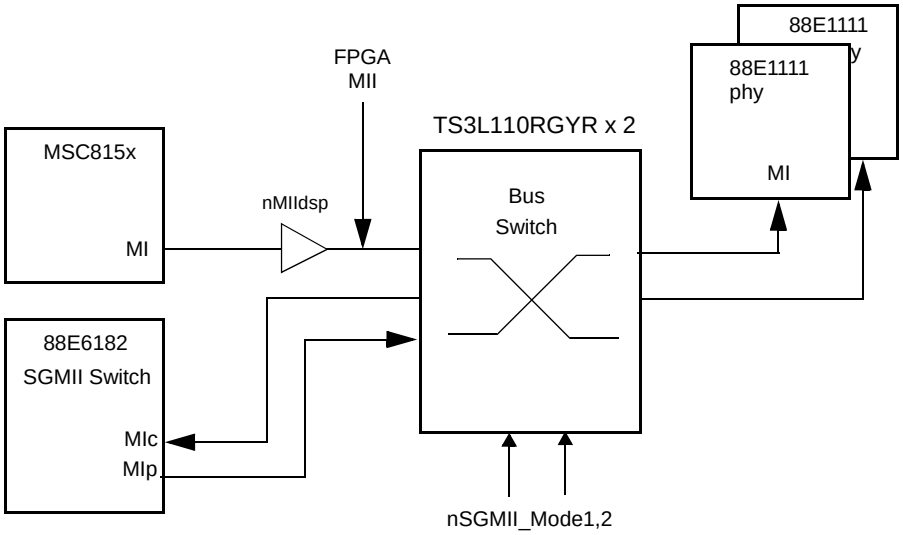


Figure 2-3. Management Bus Connectivity

FPGA MII Interface allows to configure devices like PHY and SGMII switch prior to the MSC8156 family boot from Ethernet.

Table 2-2. MI Configuration

GETH Mode		Backplane Mode	Path	MI Interconnection
MSC815x GE1	MSC815x GE2			
RGMII	RGMII	no	MSC815x-> Copper	MSC815x->88E1111 or if RGMII switch presents 7380->88E1111
RGMII	RGMII	yes	MSC815x-> AMC	MSC815x->88E6182[a]->88E1111
SGMI	RGMII	no	MSC8156-> Copper	MSC815x->88E6182[a]->88E1111 (SGMII) MSC815x->88E1111(RGMII) or if RGMII switch presents 7380->88E1111(RGMII)
RGMII	SGMII			
SGMII	RGMII	yes	MSC815x-> AMC or MSC815x-> Copper	MSC815x->88E6182[a]->88E1111 (SGMII) MSC815x->88E1111(RGMII) or if RGMII switch presents 7380->88E1111(RGMII)
RGMII	SGMII			

a. Indirect access via MI controller of 88E6182

2.3 Boot Over Ethernet

Boot over Ethernet can execute from different sources, depending on the ADS environment. **Figure 2-4** shows the available boot configurations.

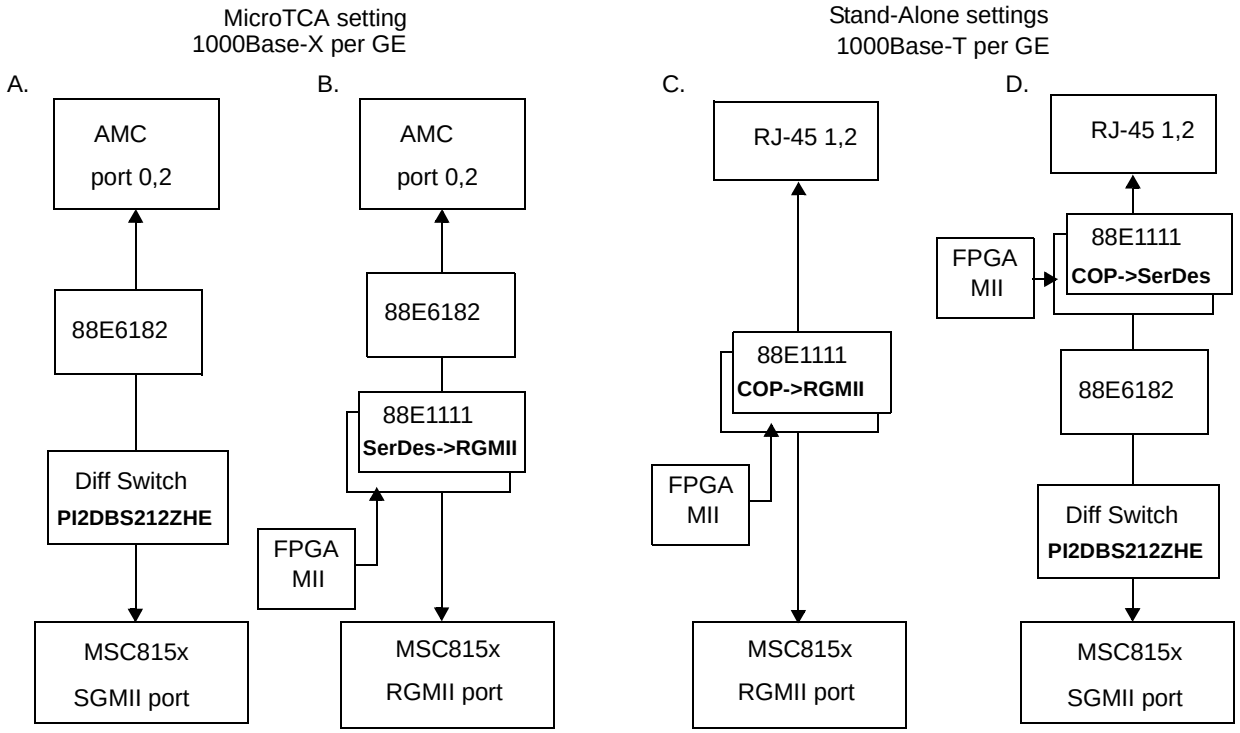


Figure 2-4. Boot-over-ETH configuration

In scenario “A” and “B”, the ADS is inserted into a MicroTCA backplane to make the AMC EN signal go low. Boot is performed over the backplane using the 1000-BX protocol. Scenarios “C” and “D” reflect ADS standalone mode. Boot configuration, through RGMII or SGMII ports, is selected via appropriate DIP-switch settings. The FPGA MII controller sets clock delay bits in GETH PHY internal registers to provide correct timing for MSC8156 RGMII ports.

2.4 DDR2 Module

The DDR2 Module is a VL491T2863E-E7S by Virtium Electronic inserted in SOCDIMM200 socket. It has 1 GB accessed via a 64-bit Data Bus with 8-bit ECC. The 200-pin socket 1827341-5 produced by Tyco. The module has an I^2C bus programmed temperature sensor and SPD EEPROM at address 0x51.

2.5 DDR3 Module

The DDR3 Module is an MT8JSF12864H(I)Y-1G1 by Micron inserted in SODIMM204 socket. It has 1GB accessed via a 64-bit Data Bus. The socket is 78193-3012 produced by Molex. The module has I^2C bus programmed temperature sensor and SPD EEPROM at address 0x52.

2.6 DDR3-to-DDR2 Interposer

The interposer is not part of MSC8156ADS Bill-of-material. It may be used for DDR-2 port validation in DDR2 configuration mode. The interposer is taken from MPC8569MDS project.

2.7 SPI Flash

The M25P64 is a 64 Mbit (8M x 8) Serial Flash produced by ST. The Serial SPI Flash is used as indirect boot memory for MSC8156 for large-size code (> 64 kB) segments from the I^2C Boot EEPROM. The memory is accessed by a high speed SPI-compatible bus. By using the Page Program instruction, the memory can be programmed from 1 to 256 bytes at a time. The Write Protect (WP) input allows the user to freeze the size of the area of memory that is protected against program or erase instructions when low. The WP pin is controlled from the BCSR12.4. The reset state is write disable. To enable memory write operation, WP bit BCSR12.4 should be set high.

2.8 TDM Level Shifter

MSC8156 GPIO power is 2.5 V. The external TDM bus (CT-bus) is a 3.3 V level. The level shifter includes bidirectional buffers converting 2.5 V to 3.3 V signals and vice versa, shown in **Figure 2-5**.

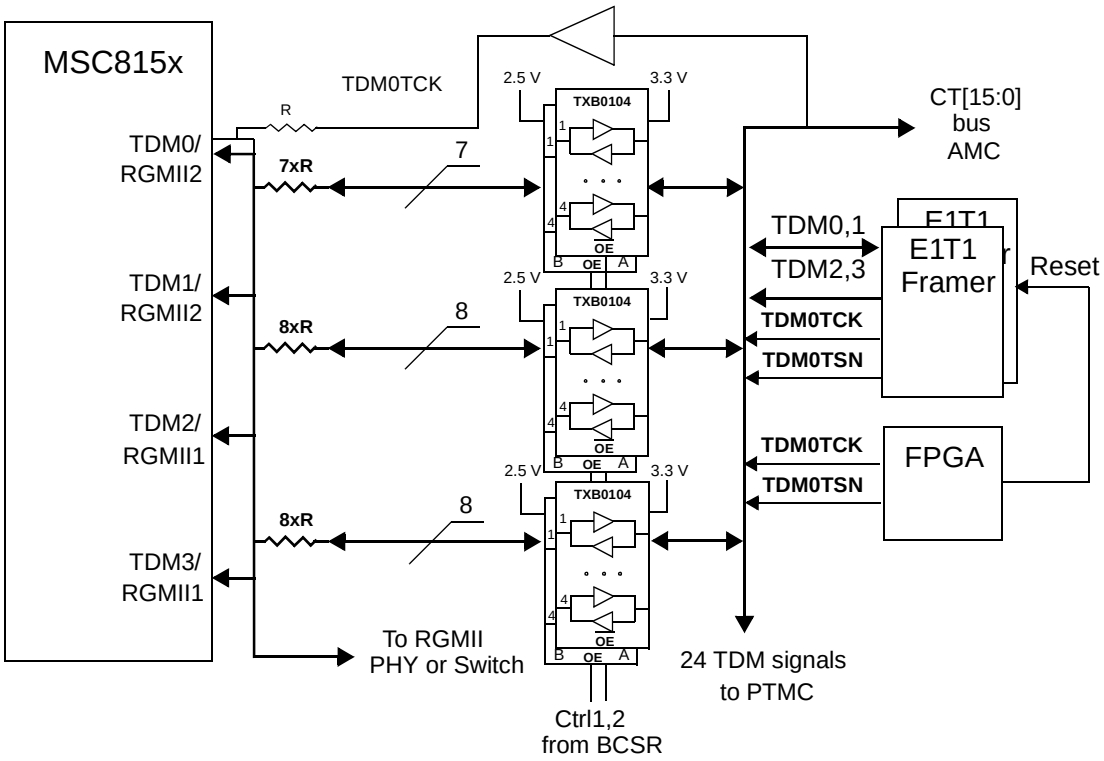


Figure 2-5. TDM Bus

The bus uses a 4-bit bidirectional level shifter with auto-direction sensing TXB0104 by TI. Port A signal levels can be in the range of 1.2 V–3.6 V and Port B in the range of 1.65 V–5.5 V. TXB0104 architecture does not require a direction-control signal to control the direction of data flow from A to B or from B to A. The detailed pinout of PTMC and AMC connectors are found in **Chapter 3**, *Expansion Options*.

TDM ports are multiplexed with RGMII ports on MSC8156. To eliminate extra load on the fast RGMII signals due to TDM routing, the serial termination 220 Ω is implemented. Buffer output control signals from BCSR isolate unused TDM ports when the RGMII interface is selected.

An FPGA can generate programming for the TDM main Clock and Sync signals. See BCSR12 control register on page 2-34. Working with FPGA synchronization requires disabling the E1/T1 framers by clearing the FRMEN bit in BCSR9.1.

2.9 E1/T1 Framer

The E1/T1 framer is implemented using the DS26521 by Dallas, as on the MSC8144ADS. This is a single chip framer and LIU combination for T1, E1, and J1 applications and supports both long haul and short haul lines. The transceiver is composed of a line interface unit, framer, HDLC controller, elastic store, and a TDM backplane interface (H.100).

The framer is configured via the SPI bus. Access is available from the SPI port of the MSC8156 SPI port as well as via the FPGA SPI controller. The line interface is done via a transformer and dual RJ48 connector.

The TDM interface to the MSC8156 TDM port is based on a backplane configuration with an elastic store enable. All clocks are produced from a master clock of 2.048 MHz. The MSC8156 TDM ports 0–3 are programmed in Clock/Sync shared mode. Data channels use TDM port 0 and 2. Signaling channels use TDM port 1 and 3. Common reset signal driven by BCSR9.3 FRMEN bit enable the both framer, when negated. In additional RGMII clock buffer is disable, since the MSC8156 RGMII input clock pin is multiplexed with TDM data line.The default state of framers depend on DIP switch setting. When any of MSC8156 RGMII port is enable the framers stay in reset to prevent contention on signal lines. The second TDM select mode is linkage to the board’s outside TDM peripherals over PTMC or AMC connectors as shown in **Figure 2-5**. These allows by isolating the framer’s outputs in reset state and enable TDM buffers bits when GE1,GE2 BCSR6.3-4 bits are high.

TDM operations should only be used on the board when the RGMII PHYs are in isolation mode (see **2.2**, *Gigabit Ethernet Ports*). Otherwise, the PHY Rx drivers can distort the appropriate TDM signals. The 125 MHz GETH input clock buffer is disabled when TDM mode is selected for both GE/TDM ports.

2.10 I²C Bus

Figure 2-6 shows the I²C bus diagram.

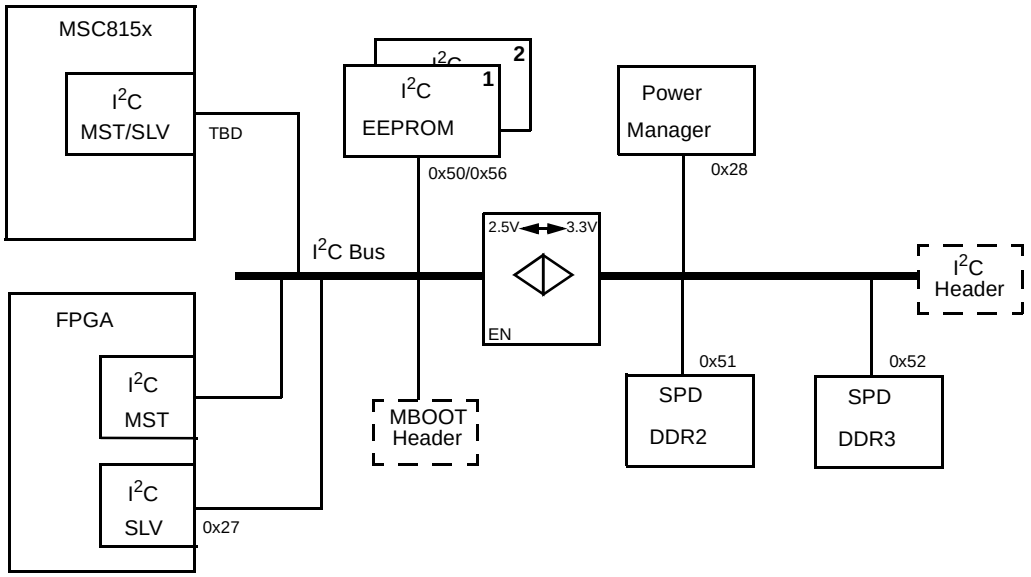


Figure 2-6. I²C Bus Peripherals

There are three Masters on the I²C bus:

- MSC8156 I²C controller
- FPGA hardware I²C module containing I²C Master and I²C Slave Controllers
- [Optional] External boot master over 2.5 V MBOOT header
- [Optional] I²C header on 3.3 V side may be used for Power Manager programming with Power One dedicated equipment.

The on-board masters can access all the I²C slaves on the bus. The SPD EEPROM on the DDR Module contains configuration data needed to program the DDR controller.

2.10.1 Using I2C for Boot

Using the FPGA I2C master for I2C Boot EEPROM programming prior MSC8156 first run is simple way to prepare RCW and boot data.

2.10.2 I2C EEPROM Parts

MSC8156 may load configuration word from one-byte (short) and two-byte (long) addressing I2C EEPROM parts. On the ADS are populated the both memory type. The RCW source part should have device address 0x50. The second I2C EEPROM gets address 0x56 for bypass when boot. See below on the **Figure 2-7**.

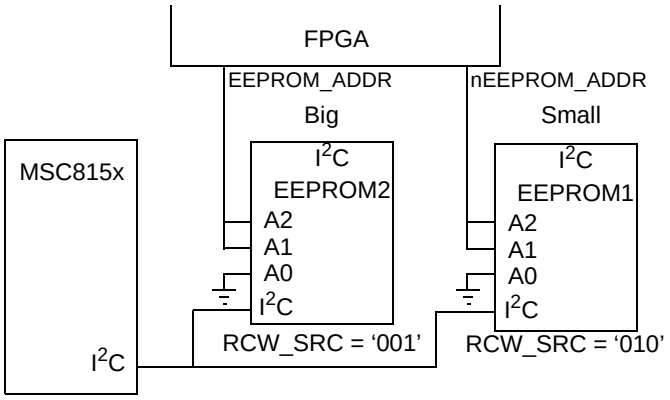


Figure 2-7. I2C EEPROM Select

The short address I2C EEPROM is AT24C01A-10TU-2.7 1Kb by Atmel. The second-long address one is M24512-WMW6 512Kb by ST.

2.11 SPI Bus

SPI bus connectivity is shown in **Figure 2-8**. The MSC8156 SPI controller can access any bus slave: SPI BOOT Flash, Clock Synthesizer, SGMII Boot EEPROM, RGMII switch (optional), and two E1/T1 Framers. Six MSC8156 GPIO pins serve as SPI chip enables.

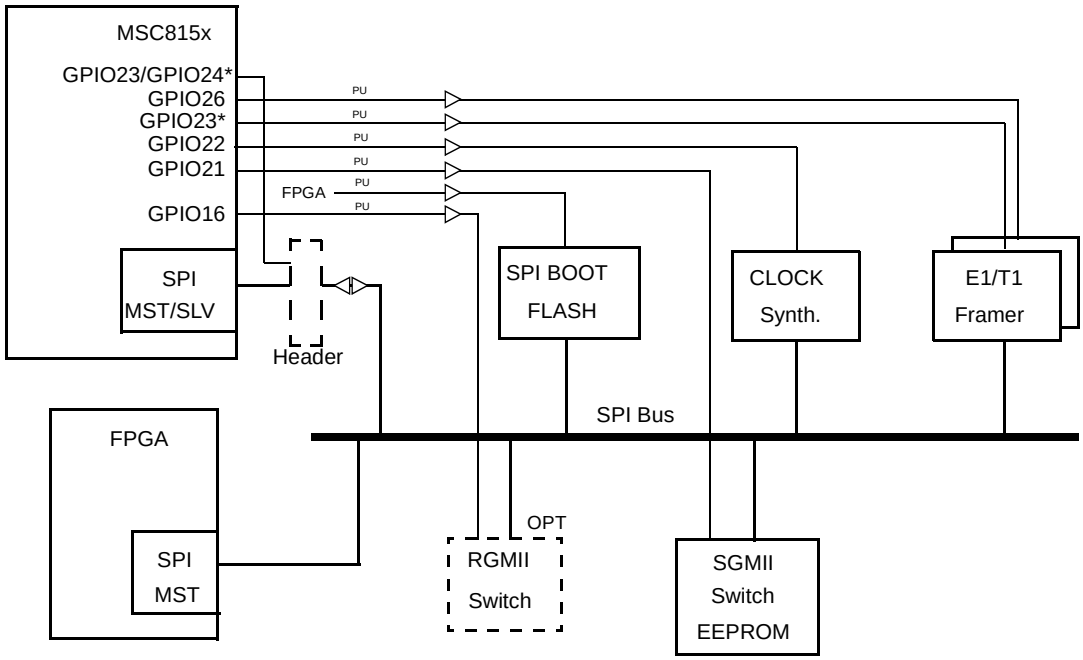


Figure 2-8. SPI Bus Peripherals

The SPI chip select signal to the Flash has two GPIO sources:

- GPIO23. Acts by default, specifically when a boot from SPI occurs.
- GPIO24. An additional chip select signal used for different software applications.

The BCSR8.4 SPIFL bit selects one of two available SPI chip select signals. When the bit is high (1), GPIO23 serves as the SPI Flash chip select signal; if low (0), it uses GPIO24.

The optional 5-pin 0.1” header carries the following bus signals:

- MISO. SPI Master Data Input
- MOSI. SPI Master Data Output
- SCK. SPI Clock
- nSL. SPI Slave Enable
- GND

Because the MSC8156 uses 2.5 V for the I/O interfacxe, SPI bus level buffers are required to interface with 3.3 V SPI devices.

2.12 JTAG Debug Interface

The ADS JTAG interconnection scheme is shown in **Figure 2-9** below:

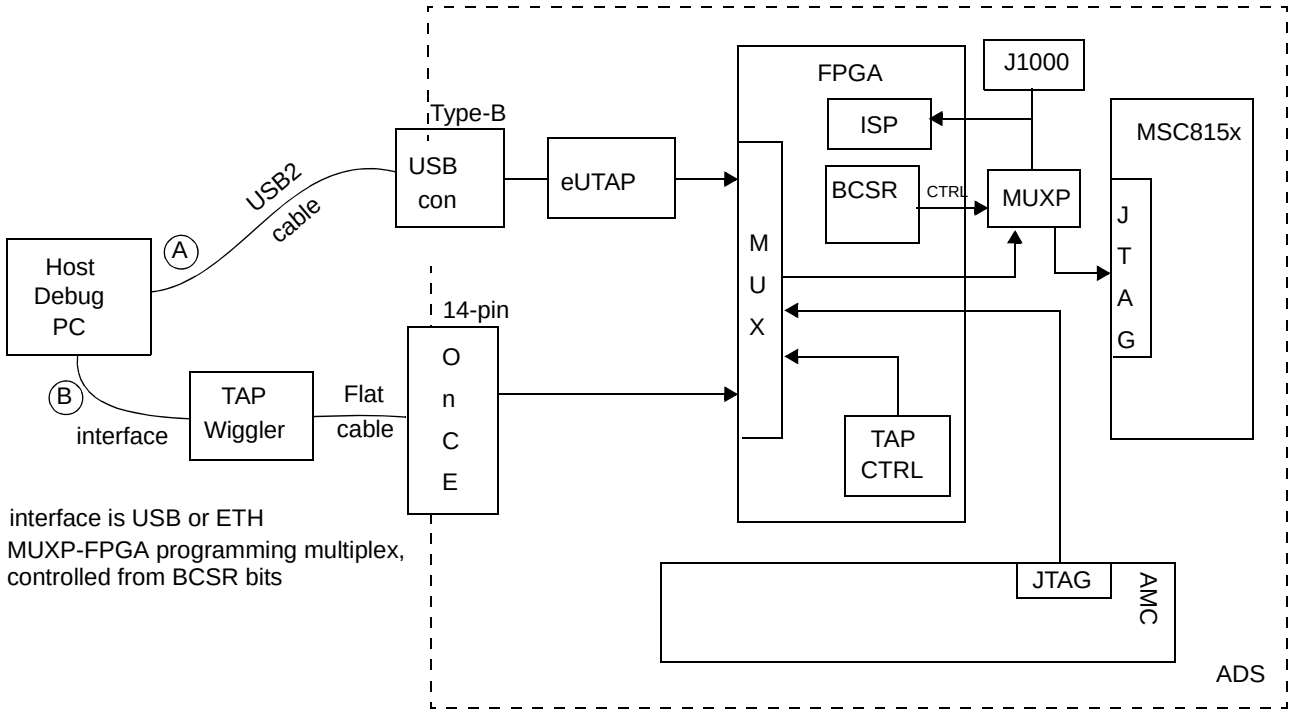


Figure 2-9. ADS JTAG Multiplexer

The MSC8156 Debug Port (JTAG) may be interface to Host Debug Machine over USB port ("A" path) or through standard 14-pin OnCE header ("B" path). The "B" configuration requires an external device transformed the Host interface (USB or Ethernet) to JTAG signals.

The default "A" interconnection uses only USB cable. On the ADS embedded USB-to-TAP drives JTAG signals to the FPGA multiplex. Select of JTAG source direction is done logically by USB Vbus sensing. All time the USB cable is disconnect the MSC8156 Debug Port is linked to the 14-pin OnCE header.

The FPGA TAP controller can be activated with the appropriate signal sequence. By default, the controller is disabled, so that the TAP controller is invisible (zero-bypass) over the JTAG chain. Upon activation, the controller inserts into the JTAG chain.

When the ADS is used in an AMC B2B expander, both boards can added to the entire JTAG chain.

The JTAG position is defined according to the geographic address of the ADS as an AMC card. Also, the two ADS boards can have a common HRST signal via the AMC RSRV6 line for synchronization. **Figure 2-10** shows the setup for JTAG chain operation. See **Table 2-3** for the different JTAG chain configurations. If GA = 0, The DUT is first in the JTAG chain.

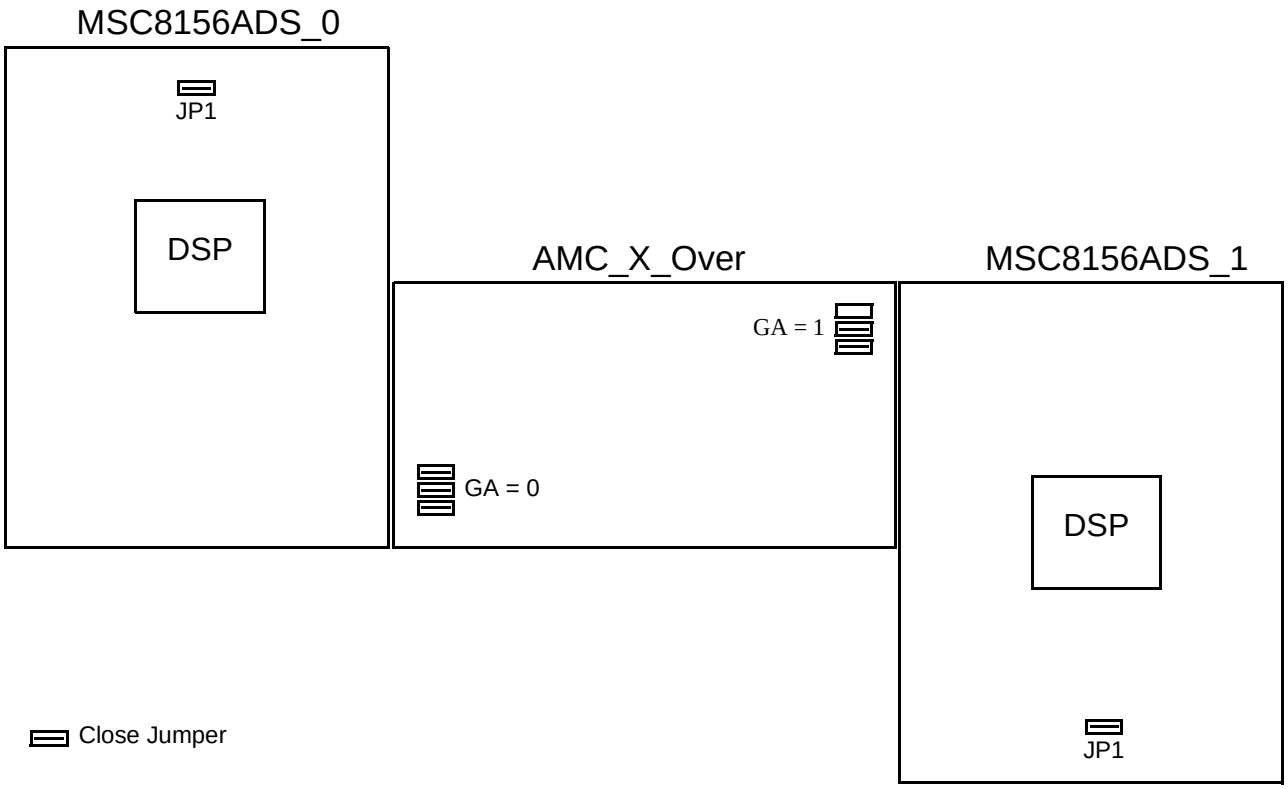


Figure 2-10. JTAG Chain over AMC-X-Over Card

Table 2-3. JTAG Port' Order in Chain

Configuration	Order in Chain
Single MSC8156	MSC8156
Activate TAP ctrl	TAP_ctrl, MSC8156
AMC-X-Over card with two ADS connection	(TAP_ctrl[a] + MSC8156)_0[b], (TAP_ctrl + MSC8156)_1

a. FPGA TAP controller insertion is optional.
b. Index means geographic address of the ADS as AMC card

2.12.1 FPGA Programming

MUXP shown in **Figure 2-9** allows for FPGA programming. An erased device provides a control signal selecting the ISP connector. This allows you to program the FPGA once after power-on. Initiated FPGA logic releases the control signal to direct the JTAG signals to the MSC8156 Debug Port. To re-program the FPGA content, the two BCSR bits 12.5 and 13.4 (FPGA_PRG1,2) should be cleared (0). After that, the update SVF image file can be loaded via the Embedded UTAP. The next power OFF/ON sequence returns the MUXP in the initiate state. The dedicated ISP 10-pin connector J1000 is used to program the FPGA with the Lattice programming tool at any time. The programming mode can be forced by the appropriate setting of the 3-pin JP1000 PRG jumper; see **Table 2-4**.

Table 2-4. PRG Jumper Setting

Programming Mode	Setting
FPGA burning via J1000 with Lattice programmer	CLOSE 1-2
Force over-eUTAP FPGA burning	CLOSE 2-3
Possible burning over eUTAP with setting BCSR12.5 and13.4	OPEN

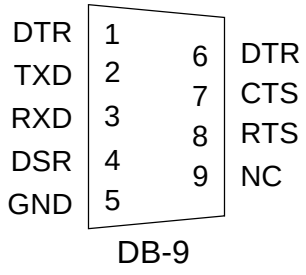
2.12.2 eUTAP Controller

The USB TAP controller connects to a host debug machine via a high-speed USB 2.0 connection and provides debug features through the JTAG port. It is a reduced version of the standard UTAP device targeted to the OnCE debug port. The eUTAP drives JTAG signals, over the FPGA JTAG multiplex, to the target.

2.13 RS-232 Port

The ADS implements an LTC2801 by Linear. It is a single interface and RS-232 transceivers can operate over a supply range of 1.8 V to 5.5 V, including the 2.5 V I/O power on the ADS. An integrated DC-to-DC converter generates power supplies for driving RS-232 levels. Two control pins “PS” and “MODE” select the transceiver normal or shutdown modes. The last mode disables both the receiver and transmitter. RS232EN BCSR9.0 bit controls the part mode. Low (0) enables the transceiver. High (1) disables the part output to use the appropriate GPIO28 and GPIO29 signals of the MSC8156.

A 9-pin female D-Type RS-232 connector is configured to connect directly (via a flat cable) to a standard IBM-PC-like RS-232 connector. **Figure 2-11** below illustrates the RS-232 connector pinouts. Directions “I”, “O” are relative to the MSC8156 (for example, “I” means input to the ADS). The RS-232 connector is intended for null-modem connectivity.



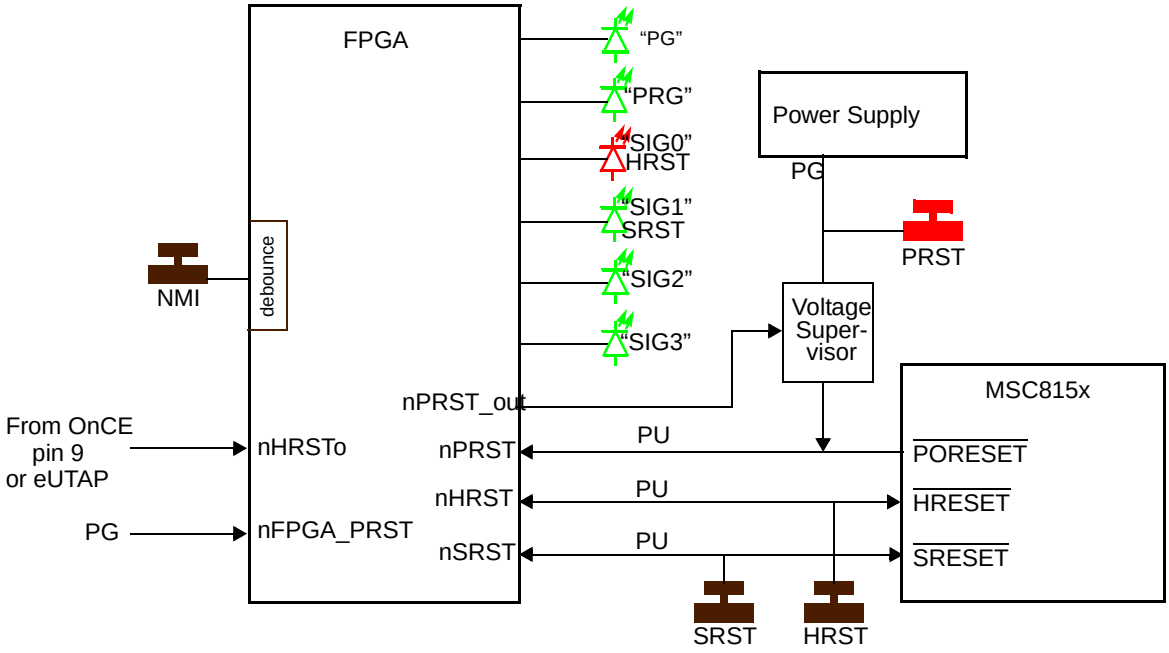
DTR—Data Terminal Ready (O)—NC
TXD—Transmit Data (O)
RXD—Receive Data (I)
DSR—Data Set Ready (I)—NC
CTS—Clear To Send (I)—NC
RTS—Request To Send (O)—NC

Figure 2-11. RS-232 Serial Port Connectors.

2.14 Reset Operation and Configuration

2.14.1 Reset Connectivity

Figure 2-12 shows the reset connectivity scheme. Section 2.14.2 and Section 2.14.3 describe the board configuration and boot sequence.



Note: PD = Pull-Down, PU = Pull-Up, PG = Power Good

Figure 2-12. ADS Reset Scheme

2.14.2 MSC815x Hardware Configuration

With active nPRST signal the FPGA samples DIP-switches with nSW_COM low. Internal pull-ups on the FPGA inputs save additional resistors on the board. After that, the FPGA drives the configuration signals correspondingly to chose the reset configuration source defined by three sampled bits RCW_SRC[0–2] until the $\overline{\text{HRESET}}$ signal is asserted to ensure MSC8156 setting loading. When the $\overline{\text{HRESET}}$ signal goes high, the FPGA finishes driving the configuration signal and sets the outputs to tri-state (high impedance) to prevent possible contention with MSC8156 GPIOs in working mode. See the connection scheme in **Figure 2-13**.

The FPGA supports all the MSC8156 hardware configuration modes:

Table 2-5. MSC8156 Configuration Modes

RCW_SRC[0:2]	Source Type	Description
000	Multiplexed external RCW loading	The whole 64-bit configuration word sampled previously from the DIP-switches is driven by FPGA in four cycles by 16- bit each time. The MSC8156 RCW_LSEL[3–0] output selects the appropriate configuration bits subset.
001	Small I^2C EEPROM	The small EEPROM applies address 0x50 to provide configuration data. Configuration DIP-switches don't care.
010	Big I^2C EEPROM	The big EEPROM applies address 0x50 to provide configuration data. Configuration DIP-switches don't care.
011	External 22-bits (reduced) Configuration Word	At first the FPGA samples 22 appropriate DIP-switches. At the second time interval the data is driven to the MSC8156.
100 and 101	Hard Coded Configuration Word	Only RCW_SRC three bits are driven the rest configuration DIP-switches don't care.

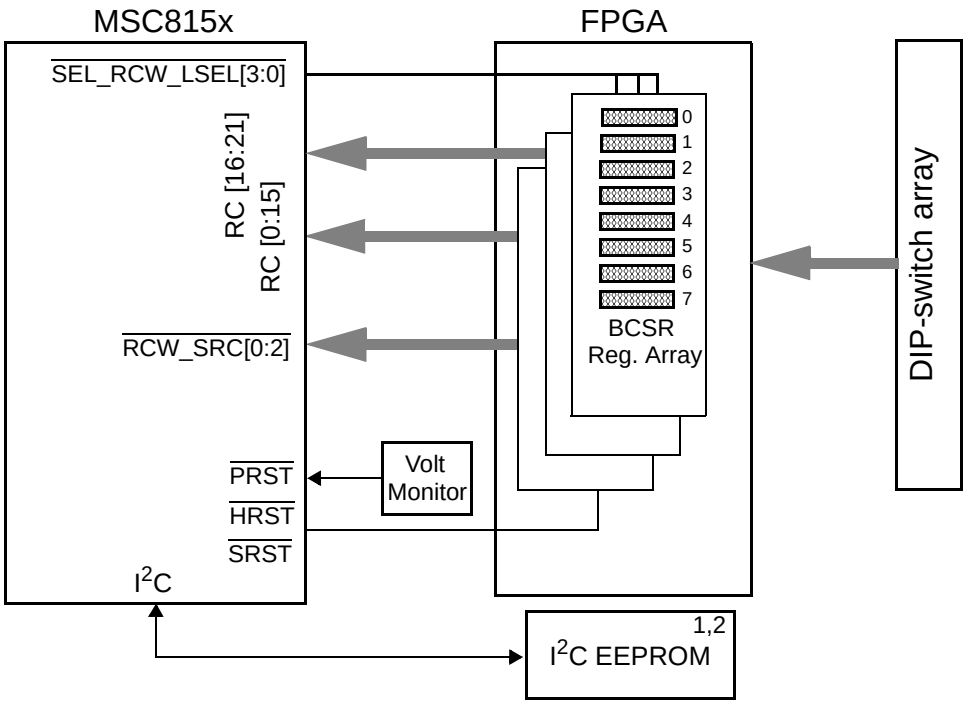


Figure 2-13. General Configuration Scheme

When RCW = '001' or '010', the configuration word originates from either the small or big I^2C EEPROM. The FPGA selects the suitable part as per the RCW value.

These initial values are defined by DIP-Switches, latched in FPGA BCSR registers during PORESET and driven towards the appropriate MSC8156 pins until SRESET is negated. The MSC8156ADS preferable default setting is RCW_SRC = ‘000’ allowing control entire RCW bits array loaded from the BCSR implemented in FPGA. Access to the BCSR via JTAG (when FPGA JTAG controller is active) allows to rewrite the RC registers at any time. The next Power-on-Reset, initiated by the FPGA (by writing a 0 into the PRST bit in BCSR13.0) or by depressing the PRST pushbutton, reconfigures the DSP. By previously clearing the locking bit CNFLOCK in BCSR13.7, you prevent reloading of the configuration from the DIP-switches and the MSC8156 starts in the BCSR programmed mode.

After power OFF/ON, the ADS applies the initiated state defined by configuration DIP switches independent from the previous BCSR0-7 RCs register settings.

2.14.3 Boot Mode

The ADS supports all MSC8156 available boot modes defined in the RCW:

Table 2-6. Boot Modes

Item	MSC815x Boot Mode	Source
1	I^2C	I^2C EEPROM 512 KB (big) or 1 KB (small)
2	SPI	SPI Flash 4MB
3	Serial RapidIO	microTCA over AMC connector
3a	Serial RapidIO + I^2C	
4	SGMII1	RJ-45-1 or AMC port 0 over SGMII switch
4a	SGMII1 + I^2C	
5	SGMII2	RJ-45-2 or AMC port 2 over SGMII switch
5a	SGMII2 + I^2C	
6	RGMII1	RJ-45-1 or AMC port 0 over RGMII phy
6a	RGMII1 + I^2C	
7	RGMII2	RJ-45-2 or AMC port 2 over RGMII phy
7a	RGMII2 + I^2C	

RCW sets the boot type; this is reflected in the appropriate BCSR registers. Dedicated DIP-switches define the primary BCSR setting after Power-On-Reset. The Display indicates the chosen boot mode. See **Table 2-6.**

2.15 Clock Options

The main clock source is a 100 MHz, 100PPM 3.3 V clock oscillator. The 2.5 V buffer transforms the 3.3 V clock signal to the 2.5-V level required for MSC8156 CLKIN input. An external clock can be used instead of the on-board clock. Other clocking options include: external pulse generator (over the optional SMB RF connector). The selection between clock sources is done by jumper JP3. The oscillator is selected by closing JP3.1-2. A pulse generator is selected by closing JP3.2-3. The clock circuits generate the clocks for the cores, the internal CLASS buses, the packet processor, the TDM, internal memory, the DDR-SDRAM memory controller, and SERDES interface for the SGMII/RapidIO/PCIe controllers. The clock generation components and clock scheme are shown **Figure 2-14**. The clock circuits are locked, according to the selected clock mode, when the first stage of the system reset configuration is done (reset configuration is controlled by the RESET block). SerDes port test outputs have four test points that serve MSC815x characterization purposes.

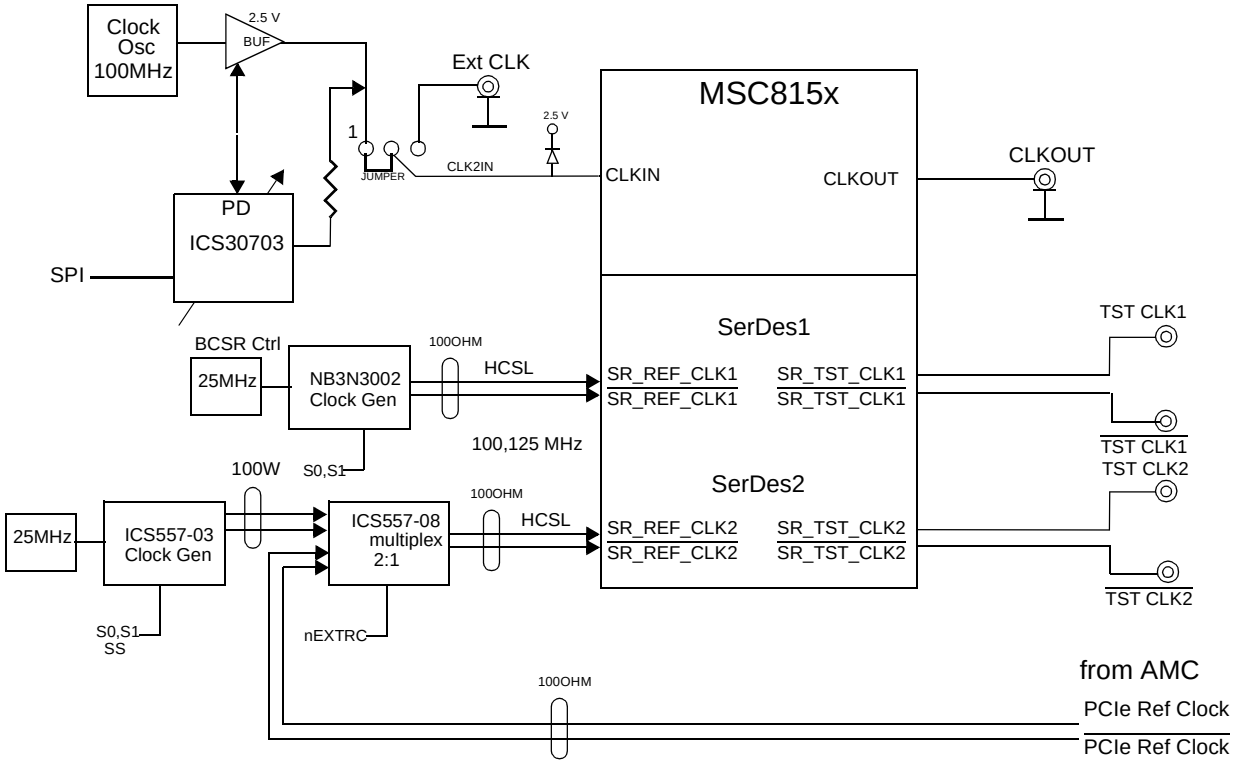


Figure 2-14. MSC8156 Clock Scheme

The clock generator is ICS557-03 part by IDT, providing SerDes2 reference clock from 25MHz crystal with spread spectrum feature. The device has two differential (HCSL) outputs. The spread type and amount are configured via select pin. The Reference Clock SerDes1 input is fed from On-Semi clock generator NB3N3002. Both synthesizers are configured to a 100 or 125 MHz output clock depending on the MSC8156 SCLK configuration bit setting. The ICS557-08 2:1 multiplexer chip allows selection of the SerDes2 clock reference. The on-board SerDes clock reference is used for the ADS standalone configuration. The microTCA backplane mode requires reference clock from external PCIe Root Complex. The selected nEXTRC signal driven by FPGA dispatches the reference clock. S0 and S1 control signals select an output frequency of 100 or 125 MHz. SS enables Spread Spectrum mode for ICS557-03 generator.

2.16 Programming Logic (FPGA)

The Lattice FPGA, LFXP2–8E–5 FT256, is from the XP2 Family; it contains embedded Flash memory blocks that store device configurations thus providing a true single-chip solution.

The FPGA has functional modules with the following features:

- I^2C controller with Master/Slave operation
- Shift register for configuring the clock synthesizer
- MII Management module
- TAP controller that provides an external ADS interface
- Biult-in SPI Controller.
- BCSR—32-byte register file that sets varying ADS modes
- TR—32-byte hidden test register file that supports varying test modes
- Two-digit, 14-segment LED display with serial interface that indicates:
  - — DSP configuration mode
  - — Core temperature measurement
- JTAG multiplexer that selects a JTAG signal source from eUTAP, OnCE, or AMC.
- Clock-in measurement

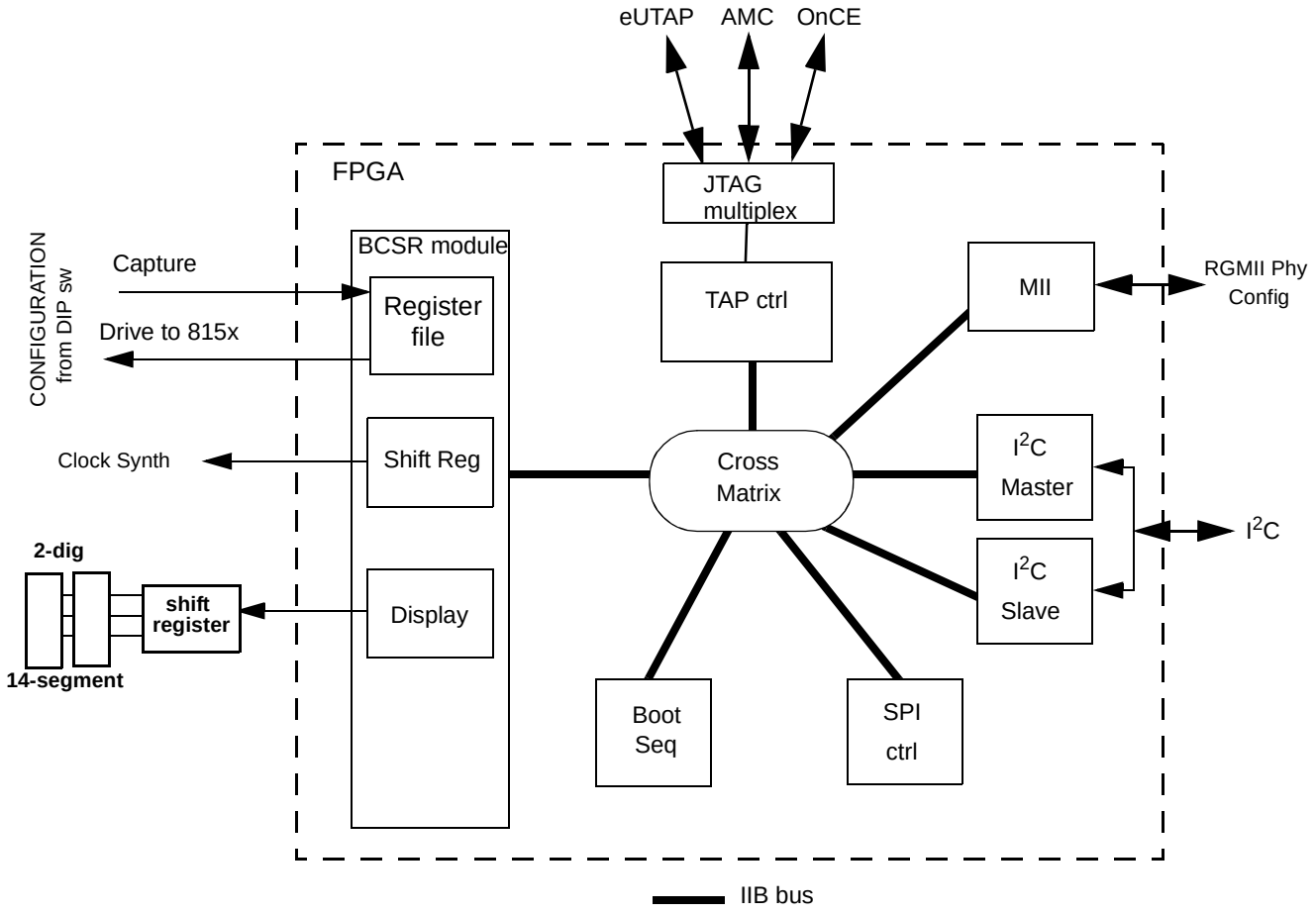


Figure 2-15. FPGA Block Diagram

Internal bus IIB is a simple, asynchronous, multi-access bus. The multi-host arbitration mechanism is provided by hard priority setting. The 8-bit address bus uses three bits as a tag for addressing different peripherals over the cross matrix. Two unidirectional data buses, IN and OUT, are eight bits wide. There are two control read and write access signals, WE and OE; they define data exchange directions. At any given time one of the two signals is active or both are negated.

Host access is finished/terminated with setting the address bus to “FF” meaning the idle IIB state. This grants the IIB for the next bus owner operation. Accordingly to said the tag ‘111’ is reserved and use to release the bus.

All available tags address modes are shown in **Table 2-7**.

Table 2-7. IIB Available Access

		To Slave				
	Slave Tag Value	IDLE ‘111’	BCSR ‘001’	Master I^2C ’010’	SPI ’011’	MII ’100’
Master	TAP Controller	Bus Termination	R/W Configuration	R/W EEPROM,PM, Temp Sensor Programming	R/W	R/W
	I^2C Slave		R/W	-	-	-
	Boot Sequencer		R/W Configuration	R/W	R/W	R/W

2.16.1 TAP Controller

The TAP controller is master on IIB bus. User may access to other modules located on the IIB via the controller. The controller is hidden on the JTAG bus by default with zero bypass mode. Special JTAG sequence wakes up it to move in regular JTAG mode till next nTRST assertion.

Below is list of the TAP controller parameters:

- Length of the Instruction register: 8 bit
- IDCODE_VALUE is 32'hAAFFFF55
- Instructions:
  - EXTEST: 0
  - SAMPLE_PRELOAD: 1
  - IDCODE: 2
  - ADDR_REG: 3 // other module address
  - DATA_RD: 4 // read out data from the IIB
  - DATA_WR: 5 //write data to the IIB
  - EXIT: 8'h66 // Break out to zero bypass mode
  - BYPASS: 8'hff

2.16.2 I^2C Controller

There two separate controllers: I^2C master and I^2C slave. The I^2C Master is controlled from internal JTAG module. The I^2C slave controller allows to access to BCSR register file from I^2C bus.

2.16.2.1 I²C Master Controller

Table 2-8 lists the controller internal registers.

Table 2-8. I²C Master Registers

Offset/ Bit	REG	7	6	5	4	3	2	1	0	Att	Default
0	PREP[15:0]	*PRER[7:0]*								R,W	0xff
1		*PRER[15:8]*									0xff
2	CTR	*CORE_EN*								R,W	0
3	RXR/TXR[a]	*DIN[7:0]*								R/W	0
4	SR/CR[b]	*RXACK*	*I2C_BUSY*	*AL*	*0*	*0*	*0*	*TIP*	*IRQ_FLAG*	R/W	0
5	TXR	*DOUT[7:0]*								R	0
6	CR	*STA*	*STO*	*READ*	*WRITE*	*ACK*	*0*	*0*	*IACK*	R	0

a. TXR field when write see for offset 5 row
b. CR field when write see for offset 6 row

- **PREP Register**
  - Prescaler PREP[15:0] divides block input clock to get I²C serial clock.
- CTR
  - CORE_EN. I²C controller core enable if high.
- **TXR and RXR Registers**: Data registers
- SR
  - RXACK receive acknowledge
  - Shows I²C_BUSY upon completion of I²C bus operation.
  - AL I²C in-process
  - TIP high during read/write operation
  - IRQ_FLAG always generates an interrupt flag.
- CR
  - STA I²C stream with START condition
  - STO I²C stream with STOP condition
  - READ access to I²C bus
  - WRITE access to I²C bus
  - ACK I²C stream with ACK condition
  - IACK I²C stream without ACK condition [only internal]

2.16.2.2 I²C Slave Controller

The controller works in accordance with the I²C bus standard:

Write (random) sequence:

```
<S><DEVICE_SEL><W><ACK><001_BCSR_ADDR><ACK><DATA_TO_WRITE> -> -> <ACK><ST>
```

Read (random) sequence:

```
<S><DEVICE_SEL><W><ACK><001_BCSR_ADDR><ACK> -> -> <S><DEVICE_SEL><R><READ_DATA><NOACK><ST>
```

Where:

- DEVICE SELECT is 7’b0100111
- BCSR_ADDR: five bits refer to 32-BCSR registers.

2.16.3 MII Controller

The controller is part of the Ethernet IP core project http://www.opencores.org/projects/ethernet/. It is fully compliant with **IEEE** 802.3 Media Independent Interface standard. The MII module is an interface to the external ETH PHY switch chip. It is used for setting the PHY configuration registers and reading status from them. The Module is located on the IIB bus with an address prefix '100'. Other Master modules, such as the TAP controller, I^2C slave, and MICO32 may program it. **Table 2-9** gives a summary of the registers in this controller with field descriptions following the table.:

Table 2-9. MII Controller Registers

Offset/Bit	REG	7	6	5	4	3	2	1	0	Att	Default
0	MIIMDR	MIINoPre	CLKDIV[6:0]							R, W	0x64
1	MIICMD	COREEN	0	0	0	0	0	WCTRLDATA	RSTAT	R, W	0
2	MIIPHYAD	0	0	0	PHYADDR[4:0]					R/W	0
3	MIIREGAD	0	0	0	RGADDR[4:0]					R/W	0
4	MIITXD1	TXD[7:0]								R/W	0
5	MIITXD2	TXD[15:8]								R/W	0
6	MIIRXD1	RXD[7:0]								R/W	0
7	MIIRXD2	RXD[15:8]								R/W	0
8	**MIISTS**	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***BUSY***	**R**	**0**
9	**MIIID**	***0***	***0***	***1***	***1***	***0***	***0***	***1***	***1***	**R**	**0**

- MIIMDR:
  - — *MIINoPre*. When low 32-bit preamble of 1's is sent. High disables the preamble.
  - — *CLKDIV*. Seven bit host clock divider. The host clock can be divided by an even number, greater then 1. The default value is 0x64 (100).
- MIICMD Register:
  - — *COREEN*. Enable core operation when high, otherwise all registers are in reset and MII I/F outputs are in tristate.
  - — *WCTRLDATA*. Write 16-bit Control Data—All Data is ready to send via MII when high.
  - — RSTAT. Read 16-bit Status from phy internal registers when high.
- MIIPHYAD Register:
  - — *PHYADDR[4:0]*. Five bits PHY Address.
- MIIREGAD Register:
  - — *RGADDR[4:0]*. Five bits Register Address (within the PHY selected by the PHYADDR).
- MIITXD2 and MIITXD1 Registers:
  - — *TXD[15:0]*.16 bits sent toward PHY TXD data.
- MIIRXD2 and MIIRXD1 Registers:
  - — *RXD[15:0]*.16 bits received from PHY data.
- MIISTS Register:
  - — *BUSY*. The bit indicated that MII controller operation is in progress when high. If low all data in registers is stable.

- MIIID Register:
  - Contains ID = 0x33.

2.16.4 SPI Controller

The controller is part of the SPI IP core project http://www.opencores.org/projects/spi/ adapted for current application. Its features are:

- Full duplex synchronous serial data transfer
- Variable length of transfer word up to 48 bits
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently 6 slave select lines

Table 2-10. SPI Master Registers

Offset/ Bit	REG	7	6	5	4	3	2	1	0	Att	Default
0-5	Tx[0:47][a] Rx[0:47]									W R	0
6	CTRL0	*CHAR_LEN[5:0]*								R,W	0
7	CTRL1	*RSRV*		*ASS*	*RSRV*	*LSB*	*Tx_NEG*	*Rx_NEG*	*GO_BSY*	R/W	0
8	DIV[7:0]	*DIV7*	*DIV6*	*DIV5*	*DIV4*	*DIV3*	*DIV2*	*DIV1*	*DIV0*	R/W	0
9	SS	*RSRV*		*EEPROM*	*FLASH*	*RGMII_phy2*	*RGMII_phy1*	*RGMII_sw*	*CLKSYN*	R/W	8'hff

a. The Data Received registers are read-only registers. A write to these registers actually modifies the Transmit registers because those registers share the same FFs.

The controller uses the following registers:

- *Rx/Tx Register*. The Data Registers hold the value of received data of the last executed transfer (Rx) or to be transmitted in the next transfer (Tx).
- *CTRL Register*. The register contains the following fields:
  - *CHAR_LEN*. 6-bits field specifies how many bits are transmitted in one transfer.
  - *GO_BSY*. Writing 1 to this bit starts the transfer. This bit remains set during the transfer and is automatically cleared after the transfer finished.
  - *Rx_NEG*. If this bit is set, the MISO signal is latched on the falling edge of a CLK, or otherwise the MISO signal is latched on the rising edge of clock
  - *Tx_NEG*. If this bit is set, the MOSI is changed on the falling edge of a CLK, or otherwise the MOSI signal is changed on the rising edge of clock
  - *LSB*. If this bit is set, the LSB is sent first on the line (bit Tx[0]), and the first bit received from the line is put in the LSB position in the Rx register (bit Rx[0]). If this bit is cleared, the MSB is transmitted/received first (which bit in Tx/Rx register that is depends on the CHAR_LEN field in the CTRL register)
  - *ASS*. If this bit is set, SS signals are generated automatically. This means that slave select signal, which is selected in SS register is asserted by the SPI controller, when transfer is started by setting CTRL[GO_BSY] and is negated after transfer is finished.

If this bit is cleared, slave select signals are asserted and negated by writing and clearing bits in SS register.

- *DIV Register*. The value in this field is the frequency divider of the PLL 80MHz to generate the serial clock. The desired frequency is obtained according to the following equation: SCLK = F/ 2*(DIV + 1).
  - *SS Register*. Slave Select Register. If CTRL[ASS] bit is cleared, writing 1 to any bit location of this field sets the proper SS[n] line to an active state and writing 0 sets the line back to inactive state. If CTRL[ASS] bit is set, writing 1 to any bit location of this field selects appropriate SS[n] line to be automatically driven to active state for the duration of the transfer, and is driven to inactive state for the rest of the time.

2.16.5 Boot Sequencer

Boot sequencer (BS) module serves to configure external peripherals prior the MSC815x starts boot routine.

BS is located on the IIB and may access to all slaves like BCSR, I^2C slave, MII and SPI modules. When MSC815x releases the nHRST signal, the BS asserts nSRTS by writing “0” into BCSR 13.1 SRST. That “freezes” the MSC815x at the entry point of the boot routine, but allows configuration of the required peripherals, because their state is independent from the SRST signal level.

The BS performs programming code written in the FPGA CMD RAM memory; each command includes from one to four bytes:.

Table 2-11. BS Command Summary

Mnemonic	Operation	1-st byte (code)	2-nd byte	3-d byte	4-d byte
WR	Write to IIB destination	0x01	<IIB addr>	-	-
RD	Read from IIB source with compare	0x02	<IIB addr>	Mask of read value	Expected masked value
JMP	Change of flow to destination address	0x03	<dest. address>	-	-
LJMP	Long Jump	0x04	<LSB dest. address>	<MSB dest. address>	-
RTA	Read from IIB source to accumulator	0x05	<IIB addr>	-	-
WFA	Write from accumulator to IIB destination	0x06	<IIB addr>	-	-
WT	Wait x cycles. Number of cycles defines in code byte. Up to 125us delay	0b100zzzzz	-	-	-
NOP	No operation - idle command	0xff	-	-	-
END	End of execution	0x00	-	-	-

- Prefix of Address for referred Module on IIB:
  - “001” - BCSR.
  - “010” - Master I^2C.
  - “011” - SPI.

— “100” - MII.

The command sequence is stored in Command RAM (CMD RAM) at 512-byte. The RAM initiated value is programmable using debug mode. BCSR14.7 bit BSEN switches between the running Boot Sequencer (low) and CMD RAM debug mode (high). The active Boot Sequencer routine is selected according to the RCW content when PORESET.

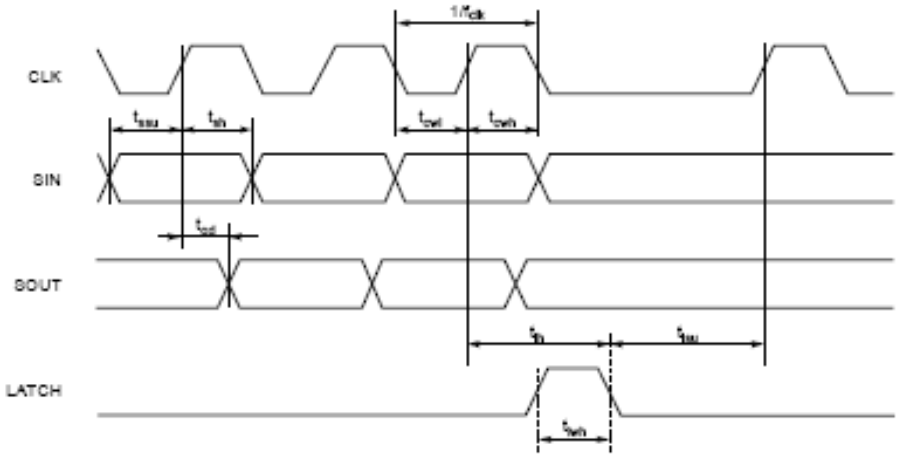


Figure 2-16. LED Display Serial Interface

2.16.6 Board Control & Status Register (BCSR)

The BCSR, an 8-bit wide read / write register file, controls or monitors most of the ADS hardware options. The BCSR is located on Internal Interface Bus and is available from different host through cross-matrix.The BCSR includes up to 32 registers. BCSR is implemented on a FPGA device that provides register and logic functions over some Board signals.

The BCSR controls or monitors the following functions:

- MSC8156 Hardware Reset Configuration signals stored in BCSR registers are available for modification from the JTAG.
- Programmed Power-on-Reset for the board with restored or updated configuration.
- Hard- Soft- Reset and NMI (IRQ0) push buttons debounce function for the MSC8156.
- Switch JTAG signals from OnCE connector and the eUTAP module.
- Enable/Disable to peripherals:
  - RS-232 Transceiver.
  - MSC8156 GE ports isolation.
- The Board Control Functions:
  - Reset Configuration Word dedicated logic.
  - Differential mux control.
  - LED Display control
  - Control reset to the most peripherals on the board.
  - Programmable SRESET for boot operation debugging.
- TDM reference clock/sync generation with programmed frequency.
- DMA validation module—optional.
- BCSR provides h/w write protection for serial SPI FLASH and I^2C EEPROMs parts.
- Logic to prevent signals contention.
- Internal controllers: JTAG and I^2C master/slave to expand board control functions.

- MII signals generator for phy and SGMII parts configuration[1].
- Boot Sequencer to configure RGMII phys prior Boot-Over-ETH.
- 16-bit clock-in frequency counter on BCSR25, BCSR26.
- MSC8156 GPIO signals control with Test Page registers when TSTPG BCSR14.6 bit is high.
- Four indication LEDs:
  - LD7(SIG0) and LD10(SIG1) for software and board reset state signaling.
  - LD6(SIG2) and LD9(SIG3) for sw debugging.
  - Debug indication over the mentioned LEDs when the MSC8156 is out of the socket.
- Additional LEDs:
  - LD5 for BOOT indication—actually recognizes I^2C CLK triggering.
  - LD8 Debug state reflects the MSC8156 EE1 signal level.
- Status registers:
  - bit PRST BCSR 13.0 to monitor nHRST reset signal level.
  - bit SRST BCSR13.1 to monitor nSRST reset signal level.
  - bit NMI BCSR6 to sample interrupt input.
- Revision control:
  - BCSR31 contains BCSR Revision code (can distinguish ADS version as well).
  - BCSR27-30 contains firmware modification date: Day, Month, Year and Hour creation of version in hexadecimal format.

Sections of the BCSR slice control registers generally have low active notations unless there is a special notice otherwise. This means that a bit function is “enabled” while the bit is zero. When a bit is set to high (or ‘1’) a related function is disabled. The most significant bit is bit 0 and the least significant is bit 7.

All BCSR registers (up to 32) are 8-bit joined in two groups: control registers with read/write access and only read status registers. Control registers obtain their default value during Power-on-Reset. The CNFLOCK bit in BCSR13[7] enables saving of settings’ values until the ADS powers down.

The first eight-registers BCSR0–BCSR7 latch the 64 bits of the Reset Configuration Word Low and High (see the Reset chapter in the *MSC815x Reference Manual* for details).

2.16.6.1 BCSR0 Reset Config Register 0

The BCSR0 may be read or written at any time. BCSR0 defaults are attributed at the time of Power-On-Reset. BCSR0 reflects RCWL bits 31-24. The fields are described below in **Table 2-12**:

Table 2-12. BCSR0 RCWL bits 31-24 (Offset 0)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-1	CLKO	***Clock Out.*** When two bits are high the CLKO[1:0] output is disabled and drives a low level. The other settings drive the clock with different frequencies.	SW3.2,3	R,W
2	RSRVL29	***Reserved RCW Low bit 29.***	0	R,W
3-7	S2P	***SERDES2 Protocol.*** Five bits S2P[4:0] choose the SerDes2 protocol according to **Table 2-13**	SW3.1, SW4.5-8	R,W

1. This feature is available starting with the ADS rev Pilot

Table 2-13. SerDes Port 2 Protocol (S2P)

Value (hex)	Protocol
0	Port is deactivated
1	RapidIO 4x @ 1.25GHz
2	RapidIO 4x @ 2.5GHz
3	RapidIO 4x @ 3.125GHz
4	RapidIO 1x @ 3.125GHz
5	RapidIO 1x @ 1.25GHz,SGMII1,SGMII2
6	RapidIO 1x @ 2.5GHz,SGMII1,SGMII2
7	RapidIO 1x @ 1.25GHz,SGMII2
8, 9	Reserved
A	PEX 1x, SGMII1, SGMII2
B	PEX 1x, SGMII1
C	PEX 1x, RapidIO 1x @ 1.25GHz
D	PEX 4x
E	PEX 2x, SGMII1,SGMII2
F	Reserved
10	PEX 1x, RapidIO 1x @ 2.5GHz
11	PEX 1x
12	RapidIO 1x @ 1.25GHz
13	RapidIO 1x @ 2.5GHz
14	RIO 1x @ 2.5GHz, SGMII2
15	Reserved
16	PEX 2x, SGMII2
17	PEX 2x/RIO 1x 1.25 GHz
18	PEX 2x/RIO 1x 2.5 GHz
19	PEX 2x
1A-1F	Reserved

2.16.6.2 BCSR1 Reset Config Register 1

The BCSR1 may be read or written at any time. BCSR1 defaults are attributed at the time of Power-On-Reset. BCSR1 reflects RCWL bits 23–16. The fields are described in **Table 2-14**:

Table 2-14. BCSR1 RCWL bits 23–16 (Offset 1)

BIT	MNEMONIC	Function	DEF	ATT.
0-3	S1P	***SERDES Port 1 Protocol.*** Four bits S1P[3:0] choose SerDes1 SerDes protocol according the **Table 2-15**	SW4.4-1	R,W
4,5	RSRVL1819	***Reserved RCW Low bits 18,19***	'00'	R,W
6	SCLK2	***SerDes2 Reference Clock.*** When **high** SerDes2 reference clock is 125 MHz. If **low** SerDes1 reference clock is 100 MHz.	SW7.7	R,W
7	SCLK1	***SerDes1 Reference Clock.***When **high** SerDes1 reference clock is 125 MHz. If **low** SerDes2 reference clock is 100 MHz.	SW7.8	R,W

Table 2-15. SerDes Port 1 Protocol (S1P)

Value (hex)	Protocol
0	Port is deactivated
1	RapidIO 4x @ 1.25GHz
2	RapidIO 4x @ 2.5GHz
3	RapidIO 4x @ 3.125GHz
4	RapidIO 1x @ 3.125GHz
5	RapidIO 1x @ 1.25GHz,SGMII1,SGMII2
6	RapidIO 1x @ 2.5GHz,SGMII1,SGMII2
7	RapidIO 1x @ 1.25GHz,SGMII1
8	RapidIO 1x @ 1.25GHz,SGMII1
9	RapidIO 1x @ 1.25GHz,
0xA	RapidIO 1x @ 2.5GHz
0xB–0xF	Reserved

2.16.6.3 BCSR2 Reset Config Register 2

The BCSR2 may be read or written at any time. BCSR2 defaults are attributed at the time of Power-On-Reset. BCSR2 reflects RCWL bits 15-8. The fields are described in **Table 2-16**:

Table 2-16. BCSR2 RCWL bits 15-8 (Offset 2)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-6	RSRVL15-9	***Reserved RCW Low bits 15 to 9.*** Not in use.	'0000000'	R,W
7	RSRVL8	***Reserved RCW Low bit 8.*** Not in use.	'0'	R,W

2.16.6.4 BCSR3 Reset Config Register 3

The BCSR3 may be read or written at any time. BCSR3 defaults are attributed at the time of Power-On-Reset. BCSR3 reflects RCWL bits 7–0. The fields are described below in **Table 2-17**:

Table 2-17. BCSR3 RCWL bits 7–0 (Offset 3)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	PLL1DIS	***Disable PLL1.*** Settings this bit disables PLL1 to reduce power consumption for clock modes 1 or 37.	“0”	R,W
1	RSRVL6	***Reserved RCW Low bits 6.*** Not in use.	‘0’	R,W
2-7	MODCK	***Clock Mode.*** MODCK[5:0] six bit set PLL modes.	SW7.6-1	R,W

2.16.6.5 BCSR4 Reset Config Register 4

The BCSR4 may be read or written at any time. BCSR4 defaults are attributed at the time of Power-On-Reset. BCSR4 reflects RCWH bits 31–24. The fields are described in **Table 2-18**:

Table 2-18. BCSR4 Description RCWH bits 31–24 (Offset 4)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	SM	***Secure Mode.*** **High** sets the chip secure mode, if **low**—normal operation.	SW6.5	R,W
1	RC	***Root Complex.*** PCI Express End Point when **low,** otherwise the PCIe controller acts as Root complex.	SW6.4	R,W
2	EWDT	***Enable Watch Dog Timer.*** When **low** the watch dog timer is initially disabled. If **high** it is enable.	SW6.3	R,W
3	PRDY	***PCI Express Ready.*** When **high** MSC8156 is ready to be configured by Root complex on PEX bus.	SW6.2	R,W
4-7	BPRT	***Boot Port Select.*** Four bits BPRT[3:0] select boot port according to the **Table 2-19**	SW6.1, SW1.8-6	R,W

Table 2-19. Boot Port Select (BPRT)

Boot Port	BPRT[3:0] Value (HEX)	Description
I^2C	0	I^2C
RapidIO	1	Serial RapidIO 1 without I^2C
	2	Serial RapidIO 1 with I^2C
SPI	3	SPI
GE1	4	RGMII1 without I^2C
	5	SGMII1 without I^2C
	6	RGMII1 with I^2C
	7	SGMII1 with I^2C

Table 2-19. Boot Port Select (BPRT)

Boot Port	BPRT[3:0] Value (HEX)	Description
GE2	8	RGMII2 without I^2C
	9	SGMII2 without I^2C
	0xA	RGMII2 with I^2C
	0xB	SGMII2 with I^2C
Reserved	0xC-0xF	—

2.16.6.6 BCSR5 Board Control Register 5

The BCSR5 may be read or written at any time. BCSR5 defaults are attributed at the time of Power-On-Reset. BCSR5 reflects RCWH bits 23–16. The fields are described in **Table 2-20**

Table 2-20. BCSR5 Description RCWH bits 23–16 (Offset 5)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	RIO	***RapidIO Access Enable.*** When **high** host access after boot is enabled.	SW1.5	R,W
1	RPT	***RapidIO Pass-Through Enable.*** When **high** RapidIO pass through is enabled.	SW1.4	R,W
2	RHE	***RapidIO Host Enable.*** When **high** RapidIO port is Host and base device ID is taken from RCWHR[DEVID] 3 LSB. If low RapidIO controller acts as agent.	SW1.3	R,W
3	SBETH	***Simple Boot Over Ethernet.*** When **high** the ***MSC8156*** performs simple type boot from Ethernet port.	SW1.2	R,W
4	RSRVH19	***Reserved RCW High bits 19.*** Not in use.	0	R,W
5	RM	***RESET Master.*** When **low** the ***MSC8156*** acts as I^2C Boot Master, when **high**—Boot Slave.	0	R,W
6	BP	***Boot Patch.*** When **high** the ***MSC8156*** jumps to boot patch.	SW1.1	R,W
6	RSRVH16	***Reserved RCW High bits 16.*** Not in use.	0	R,W

2.16.6.7 BCSR6 Reset Config Register 6

The BCSR6 may be read or written at any time. BCSR6 defaults are attributed at the time of Power-On-Reset. BCSR6 reflects RCWH bits 23–16. The fields are described in **Table 2-21**.

Table 2-21. BCSR6 RCWH bits 15–8 (Offset 6)

BIT	MNEMONIC	Function	DEF on PRST	ATT
0	RSRVH15	***Reserved RCW High bit 15.*** Not in use.	0	R,W
1	RSRVH14	***Reserved RCW High bit 14.*** Not in use.	0	R,W
2	RSRVH13	***Reserved RCW High bit 13.*** Not in use.	0	R,W

Table 2-21. BCSR6 RCWH bits 15–8 (Offset 6)

BIT	MNEMONIC	Function	DEF on PRST	ATT
3	GE1	***Select GE1 RGMII.*** **High** enables RGMII on the GE1 port. When ***low***, the GE1 port is disable and appropriate TDM buffers are enable.	SW2.7	R,W
4	GE2	***Select GE2 RGMII.*** **High** enables RGMII on the GE2 port. When **low**, the GE2 port is disable and appropriate TDM buffers are enable.	SW2.6	R,W
5	R1A	***RapidIO1 Accept All.*** With **high** the SerDes port 1 accepts all device IDs.	SW2.5	R,W
6	R2A	***RapidIO2 Accept All.*** With **high** the SerDes port 2 accepts all device IDs.	SW2.4	R,W
7	DEVID-1	***Device ID slice 1.*** Device number value DEVID[5].	SW2.3	R,W

2.16.6.8 BCSR7 Reset Config Register 7

The BCSR7 may be read or written at any time. BCSR7 defaults are attributed at the time of Power-On-Reset. BCSR7 reflects RCWH bits 23–16. The fields are described in **Table 2-22**.

Table 2-22. BCSR7 RCWH bits 7–0 (Offset 7)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-4	DEVID-2	***Device ID slice 2.*** Device number bits DEVID[4:0].	SW2.2,1 SW3.8-6	R,W
5	RSRVH2	***Reserved RCW High bit 2.*** Not in use.	0	R,W
6	RMU	***RMU Local Memory Access Select.*** Local memory port number value.	SW3.5	R,W
7	CTLS	***Transport Is Large System.*** When high Common Transport type system is large. If low—the type is small.	SW3.4	R,W

2.16.6.9 BCSR8 Reset Configuration

On the board, the BCSR8 acts as a register controlled reset configuration. The BCSR8, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR8 fields are described in **Table 2-23**.

Table 2-23. BCSR8 CTRL1 (Offset 8)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-2	CFG_RS	***Reset Configuration Source.*** The MSC8156 Configuration source arranged as RCW_SRC[2:0].	SW6.8-6	R,W
3	DBG_REQ	***Debug Request.*** A **high** value for this bit causes the MSC8156 to enter debug mode by driving “1” to the MSC8156 EE0 input during reset. When this bit is **low** the chip starts running after reset negation.	SW5.1	R,W
4	SPIFL	***SPI Flash Chip Select.*** A **low** selects MSC815x GPIO24 instead of GPIO23 as the SPI select signal for SPI Flash during boot over SPI bus. A **high** provide boot operation.	‘1’	R,W

Table 2-23. BCSR8 CTRL1 (Offset 8)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
5	MBOOT	***I²C Master/Slave Boot.*** A **high** sets I²C Master Boot by asserting STOP_BS signal. When this bit is **low** MSC815x stops boot until STOP_BS input getsa low from Boot Master.	'1'	R,W
6	MIIDSP	***MSC815x MII Bus Select.*** A **low** selects the MSC815x MII bus to program PHYs and the SGMII switch. When this bit is **high**, the FPGA MII controller can access the GETH peripherals.This feature is available starting with the ADS rev Pilot.	'0'	R,W
7	PHYCLK	***PHY2 Clock Enable.*** When **high**, the 125 MHz clock is driven to the PHY2 clockin input. This bit allows you to program the PHY2 even when the ADS is configured in TDM mode. A **low** disables PHY2.	SW2.6 & SW2.7	R,W

2.16.6.10 BCSR9 Board Control Miscellaneous Register 1

On the board, the BCSR9 acts as a board control register. The BCSR9, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR9 fields are described in **Table 2-24**.

Table 2-24. BCSR9 Peripheral Control (Offset 9)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	RS232EN	***UART Port Transceiver Enable***. Upon activation **(low),** the RS-232 Transceiver, using the UART port of the MSC8156, is enabled. When negated (**high**), the RS-232 Transceiver enters standby mode.	0	R,W
1	FRMEN	***TDM E1/T1 Framers 1,2 Enable***. Upon activation **(high)**, the E1/T1 framers work in normal mode. When **low**, the E1/T1 Framers stay in reset and release MSC8156 TDM ports lines for Ethernet functionality.	'0'	R,W
2	SGMIIRST	***Reset to SGMII Switch***. Upon activation **(low),** the switch stays in reset. When negated (**high**), SGMII switch works normally. The SGMII switch configuration EEPROM is programmed at reset of the device.	'0' when nSRST is asserted, otherwise—'1'	R,W
3	RGMIIRST1	***Reset to GE1 port RGMII phy.*** Upon activation **(low),** the phy stays in reset. When negated (**high**), RGMII phy loads configuration and goes in the working mode.	'0' when nSRST is asserted, otherwise—'1'	R,W
4	RGMIIRST2	***Reset to GE2 port RGMII phy.*** Upon activation **(low),** the phy stays in reset. When negated (**high**), RGMII phy loads configuration and goes in the working mode.	'0' when nSRST is asserted, otherwise—'1'	R,W
5	RGMIIRST	***Reset to RGMII Switch.*** Upon activation **(low),** the Switch stays in reset. When negated (**high**), RGMII Switch and goes in the working mode.	'0' when nSRST is asserted, otherwise—'1'	R,W
6	RSTDDRM	***Reset to DDR2,3 Modules.*** When **low** the DDR modules stay in reset. When **high** the DDR Modules function normally.	'1'	R,W
7	RSRV9	Not Implemented.	'1'	-

2.16.6.11 BCSR10 Board Control Misc. Register 2

On the board, the BCSR10 acts as a board control register. The BCSR10, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR10 fields are described below in **Table 2-25**.

Table 2-25. BCSR10 SerDes Control (Offset 0xA)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0–1	SEL	***SerDes Multiplex Select.*** See the multiplex coding in the **Table 2-26**	Defines S1P, S2P settings	R,W
2	SS	***Spread Spectrum Mode.*** Set parameters for Reference Clock generator according to **Table 2-26**. The mode can be changed "on-the-fly."	'1' for pure PCI Express mode (SerDes Port 2 is configured for PCI Express 4x, 2x, or 1x mode only) '0' for all other cases	
3	EXTRC	***Reference Clock from External PCI Express Root Complex.*** This bit is valid for PCI Express configuration of SerDes2. The bit controls clock multiplex U34 Select input **High** means on-board PCI Express clock source; when **low**, the reference clock is driven from the AMC connector.	'0' for pure PCI Express and AMC mode (SerDes Port 2 is configured for PCI Express 4x, 2x, or 1x mode only) '1' for all other cases	
4–5	SorRGMII	***SGMII or RGMII Mode two bits***. If MSC8156 loads RCW from I^2C the bits set correct initialize for appropriate peripheral. **High** means SGMII Mode, **low**—RGMII. The bits state together with BPL define PHY configuration mode according to ***Table 2-28***	SW5.5-6	R,W
6	BPL	***Backplane Mode***. The bit is indicates if the ADS is plugged in microTCA backplane or AMC-x-Over card. Actually the active low bit reflects nAMC_EN level.	nAMC_EN signal	R,W
7	SPIEN	***SPI Buffer Enable***. **Low** enables SPI buffers to access MSC8156 to SPI peripherals, if **high,** the SPI buffers are disabled and the FPGA SPI controller/Shift ctrl may access the SPI peripherals.	'0'	R,W

Table 2-26. SERDES Multiplex Select

S2P(hex)	S1P(hex)	SEL1(SW5.2), SEL2(SW5.3)	Remarks
5-7,A,B,E,14,16	5-8,A,B,E	1	SGMII mode presents
1-4,D	1-4,9,10	0	Only SerDes Interface

Table 2-27. Spread Spectrum Selection for SerDes2 PEX Mode

SS	Spread Mode
'0'	Disable
'1'	Down 0.5%

Table 2-28. GETH Phy Configuration Modes

SorRGMII	BPL		PHY Mode
'0'	'0'	microTCA or AMC-X-Over	SerDes-to-COP
'1'	'0'		RGMII-to-SGMII
'0'	'1'	Stand-Alone	SerDes-to-COP
'1'	'1'		RGMII-to-COP

2.16.6.12 BCSR11 As Shift Register

On the board, the BCSR11 acts as a shift register to support programming of the Clock Synthesizer part. Seventeen consecutive writes into the register shift out 132 bits of configuration. The BCSR11 byte is described below in **Table 2-29**.

Table 2-29. BCSR11 Shift Register (Offset 0xB)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-7	DataS	***Shift Data.*** Byte of data to shift into Clock Synthesizer.	'11111111'	W

2.16.6.13 BCSR12 Board Control Miscellaneous Register 4

On the board, the BCSR12 acts as a board control register. The BCSR12, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR12 fields are described below in **Table 2-30**.

Table 2-30. BCSR12 LED Control (Offset 0xC)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	SIG0	***Signal LED 0***. A dedicated **Green** LED is illuminated when SIGNAL0 is **low** or when MSC8156. The LED is unlit when in its inactive (default) state **(high)**. During the MSC8156 Reset Configuration sequence the LED indicates the SRESET assertion. The user may utilize the LED for s/w signalling purposes.	1	R,W
1	SIG1	***Signal LED 1***. A dedicated **Red** LED is illuminated when SIGNAL1 is **low** or when MSC8156 GPIO24,GPIO25,GPIO27 = 3'b010. The LED is unlit when in its inactive (default) state **(high)**. During the Reset Configuration sequence the LED indicates the HRESET assertion.	1	R,W
2	SIG2	***Signal LED 2***. A dedicated **Green** LED is illuminated when SIGNAL2 is **low** or when MSC8156 GPIO24,GPIO25,GPIO27 = 3'b101. The LED is unlit when in its inactive (default) state **(high)**. The user may utilize the LED for s/w signalling purposes.	1	R,W
3	SIG3	***Signal LED 3.*** A dedicated **Green** LED is illuminated when SIGNAL3 is **low** or when MSC8156. The LED is unlit when in its inactive (default) state **(high)**. The user may utilize the LED for s/w signalling purposes.	1	R,W
4	WP	***BOOT Memory Protect***. When asserted (**low**) the BOOT EEPROM and SPI FLASH write operations are disabled, when deasserted (**high**) the regular access is available.	0	R,W

Table 2-30. BCSR12 LED Control (Offset 0xC) (Continued)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
6	TSENSE	***Die Temperature Sense***. When bit is **low** the FPGA I2C Master Controller polls the MSC8156 die Temperature Sense and the temperature is shown on the LED Display. The same occurs when the SCROLL push button is depressed once. If the bit is **high** the I2C bus is released for other operations and the LED Display indicates the DSP configuration mode.	'1'	R,W
7	RSRV12	Not Implemented.	'1'	-

2.16.6.14 BCSR13 Board Control Miscellaneous Register 3

On the board, the BCSR13 acts as a board control register. The BCSR13, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR13 fields are described below in **Table 2-40**

Table 2-31. BCSR13 Description Miscellaneous Function 3 (Offset 0xD)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	PRST	***Power-on-Reset.*** Writing **low** generates a PORESET pulse for MSC8156ADS to reconfigure it. Read out the nHRTS signal level.	'1' after reset	R,W
1	SRST	***Soft Reset.*** **Low** asserts ***MSC8156*** Soft Reset. When **high**, the MSC8144 operates normally. Read out the nSRTS signal level.	'1' after reset	R,W
2-4	TDMDIV	***TDM Clock Divider.*** Three bits set TDM clock divider. See coding in **Table 2-32**.	'000'	R,W
5	FPGA_PRG1	***Select FPGA program*****.** Writing **low** into this bit together with bit BCSR13.4 links FPGA ISP port to the JTAG programming source. When **high** the JTAG multiplex selects debug source.	1	R,W
6	NMI	***Non-maskable interrupt.*** Writing **low** generates an NMI low pulse to the ***MSC8156*** to interrupt code execution. Read samples nNMI signal line.	1	R,W
7	CNFLOCK	***Configuration Lock.*** Allows locking of the values of control registers until power down. The bit is activated when **low. High** is a default mode when configuration bits are rewritten from the DIP-switches.	1	R,W

Table 2-32. TDM Clock Divider

TDMDIV[0:2]	Frequency
1	16 MHZ
2	8 MHZ
3	4 MHZ
4	2 MHZ
0,5–7	Disabled

2.16.6.15 BCSR14 Board Control Miscellaneous Register 4

On the board, the BCSR14 acts as a MSC8156 programming mode. The BCSR14, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR14 fields are described in **Table 2-33**.

Table 2-33. BCSR14 Description Miscellaneous Function 4(Offset 0xE)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-2	RSRV14-1	Not Implemented.	'0'	R
3	RSRV14-2	Not Implemented.	'1'	R
4	FPGA_PRG2	***Select FPGA program.*** Writing **low** into this bit together with bit BCSR12.5 links FPGA ISP port to the JTAG programming source. When **high** the JTAG multiplex selects debug source.	1	R,W
5	RSRV14-3	Not Implemented.	Assembly depended	R
6	RSRV14-4	Not Implemented.	'0'	R
7	BSEN	***Boot Sequencer Enable***. Boot Sequencer (BS) allows to configure external peripherals like GETH phy or Switch prior boot code starting. BS enables with **low**, when the bit is **high** the Command RAM may be updated over BCSR15.	Depend on RCW	R,W

2.16.6.16 BCSR15 CMD RAM Data Register

On the board, the BCSR15 allows access to CMD RAM (command RAM) in debug mode. When BSEN bit 7 of BCSR14 is high the RAM Data may be read or write over BCSR15. The address pointer uses a zero offset after the ADS HRST assertion. Each access read or write increments the pointer.

Table 2-34. BCSR15 Description CMD RAM Data (Offset 0xE)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-7	RAMDATA	***Command RAM Data.*** Access to the RAM is available when BSEN BCSR14.7 bit is high. The address is auto-incremented after write/read operation.	'00000000'	R,W

2.16.6.17 BCSR17 Board Status Register 1

The BCSR17 Register is a status register (read only). The BCSR17 fields are described in **Table 2-35**.

Table 2-35. BCSR17 Status Register Description (Offset 0x11)

BIT	MNEMONIC	Function	Read At
0-5	EE2	***EE2 Four Pins.*** MSC8156 Event signals EE2_0, EE2_1, EE2_2, EE2_3,EE2_4, EE2_5	MSC8156 EE2 Pins
6	EE1	***EE1 Pin.*** MSC8156 Debug Acknowledge signal. **High** value means MSC8156 stands in debug. When this bit is **low** the chip is running	MSC8156 EE1 Pin
7	RSRV17	Not Implemented.	'1'

2.16.6.18 BCSR18–BCSR19 Reserved

2.16.6.19 BCSR20 Display Control Register

The BCSR20 Register is LED display control register. The BCSR20 fields are described below in **Table 2-36**.

Table 2-36. BCSR20 Display Control Register (Offset 0x14)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	DUM	***Display User Mode***. When **high** display indicates the ADS configuration modes. If **low** user may write the desired code in the display register.	'1' after reset	R,W
1	SCROLL	***Display Scroll***. Depress Scroll push button and the bit goes **high** till writing **low** to the bit.	'0' after reset	R,W
2-7	RSRV20	Not Implemented.	'111111'	-

2.16.6.20 BCSR21 Displayed Code 1 Register

The BCSR21 Register is LED display code register. The BCSR21 fields are described below in **Table 2-37**.

Table 2-37. BCSR21 Displayed Code Digit 1 (Offset 0x15)

BIT	MNEMONIC	Function	ATT.
0	DOT1C	Bit of dot LED, digit 1. **High** is on.	Read
1-7	SEG1C	Indicated symbol in ASCII.	Read

2.16.6.21 BCSR22 Displayed Code 2 Register

The BCSR22 Register is LED display code register 2. The BCSR22 fields are described below in **Table 2-38**.

Table 2-38. BCSR22 Displayed Code Digit 1 (Offset 0x16)

BIT	MNEMONIC	Function	ATT.
0	DOT2C	Bit of dot LED, digit 2. **High** is on.	Read
1-7	SEG2C	Indicated symbol in ASCII.	Read

2.16.6.22 BCSR23 Display Buffer Digit 1 Register

The BCSR23 Register is LED display data register, using for user's display mode DUM = 0. The BCSR23 fields are described below in **Table 2-39**.

Table 2-39. BCSR23 Display Digit 1 (Offset 0x17)

BIT	MNEMONIC	Function	ATT.
0	DOT1U	Bit of dot LED, digit 1. **High** is on.	R/W
1-7	SEG1U	Indicated symbol in ASCII in User's Mode.	R/W

2.16.6.23 BCSR24 Display Buffer Digit 2 Register

The BCSR24 Register is LED display data register 2, using for user's display mode DUM = 0. The BCSR24 fields are described below in **Table 2-40**.

Table 2-40. BCSR24 Display Digit 1 (Offset 0x18)

BIT	MNEMONIC	Function	ATT.
0	DOT2U	Bit of dot LED, digit 2. **High** is on.	R/W
1-7	SEG2U	Indicated symbol in ASCII in User's Mode	R/W

2.16.6.24 BCSR25 Clock-in Measurement Register 1

The BCSR25 Register is a status register (read only) The BCSR25 fields are described below in **Table 2-41**.

Table 2-41. BCSR25 Frequency Counter High Byte (Offset 0x19)

BIT	MNEMONIC	Function	Read At
0-7	COUNT1	MSB of Clock-in frequency counter in 1/2ms	Calculated

2.16.6.25 BCSR26 Clock-in Measurement Register 2

The BCSR26 Register is a status register (read only) The BCSR26 fields are described below in **Table 2-42**.

Table 2-42. BCSR26 Frequency Counter Low Byte (Offset 0x1A)

BIT	MNEMONIC	Function	Read At
0-7	COUNT2	LSB of Clock-in frequency counter in 1/2ms	Calculated

Input clock frequency may be calculated as follow:

Fclkin = COUNT1_COUNT2 x 8 [kHz];

2.16.6.26 BCSR27 Board Firmware Date 1

The BCSR27 Register is a status register (read only). The BCSR27 fields are described below in **Table 2-43**.

Table 2-43. BCSR27 Time Stamp 1 (Offset 0x1B)

BIT	MNEMONIC	Function	Read At
0-7	TIMED	Firmware Creation Day.	Programmed

2.16.6.27 BCSR28 Board Firmware Date 2

The BCSR28 Register is a status register (read only). The BCSR28 fields are described below in **Table 2-44**

Table 2-44. BCSR28 Time Stamp 2 (Offset 0x1C)

BIT	MNEMONIC	Function	Read At
0-7	TIMEM	Firmware Creation Month.	Programmed

2.16.6.28 BCSR29 Board Firmware Date 3

The BCSR29 Register is a status register (read only). The BCSR29 fields are described below in **Table 2-45**

Table 2-45. BCSR29 Time Stamp 3 (Offset 0x1D)

BIT	MNEMONIC	Function	Read At
0-7	TIMEY	Firmware Creation Year.	Programmed

2.16.6.29 BCSR30 Board Firmware Date 4

The BCSR30 Register is a status register (read only). The BCSR30 fields are described below in **Table 2-46**

Table 2-46. BCSR30 Time Stamp 4 (Offset 0x1E)

BIT	MNEMONIC	Function	Read At
0-7	TIMEH	Firmware Creation Hour.	Programmed

2.16.6.30 BCSR31 Board Firmware Revision Number

The BCSR31 Register is a status register (read only). The BCSR31 fields are described below in **Table 2-47**

Table 2-47. BCSR31 Firmware Revision (Offset 0x1F)

BIT	MNEMONIC	Function	Read At
0–3	REV	***BCSR Revision***. Four bits revision coding. See **Table 2-48**	Programmed value
4–7	SubREV	***BCSR Sub Revision.*** Four additional bits revision coding. See **Table 2-49**	Programmed value

Table 2-48. BCSR Rev Coding

REV Value	Board PCB rev
0	Proto,Proto1
1	Pilot
2	RevA

Table 2-49. BCSR Rev Coding

SubREV Value	Board Assembly
0xxx	Regular Board
1xxx	Board Bring-Up Version (with RGMII switch)

2.16.7 Test Page Registers TR

The Test Page registers are located on the second page of BCSR memory map.

The registers have name TR with index and offset like BCSR registers.The switch between pages the main and the test is made with writing 1 to TSTPG bit BCSR14.6. The internal mapping comes back to the main BCSR page with writing low TSPG bit.

All register TRx getting high value after PON reset. This page registers allow to test GPIO signals of the MSC8156. To set GPIO input level the appropriate TR register bit should be loaded with the desired value. Reading back the GPIO output level is possible while the bit set high.

Table 2-50. Map of Test Registers

815x GPIO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	28	29
TR REG	TR7[3:0]				TR6[4:3]		TR6[1]	TR4[6:4]			TR3[7:4]				TR1[6], TR1[0:1]			TR16[5:0]					

In addition, the Test Page includes timer/counters allowing validation of the MSC8156 internal timers TMR0 to TMR4 that include one control register TR24 and four 8-bit counter registers TR25–TR28 combined into 32-bit word. The default sampling time is 1 s. The count is started by writing high to the bit GO/EXP bit in TR24.3. Writing to the bit prior to the timer expiring expands the sampling window to more one period of 1 s. This feature allows measurement of very slow signals. The service program should poll the GO/EXP bit to verify when the count has been finished. The TR25–TR28 registers accumulate the measurement frequency in GHz units. See **Table 2-51** for the TR24 bit descriptions.

Table 2-51. TR24 Timer Count Control Register

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0–2	TMRSEL	***Timer Select.*** The three bits define number of timer under testing from TMR0 to TMR4.	'000'	R,W
3	GO/EXP	***GO.*** Write **high** starts the counter or continue to count.	0	W
		EXPIRED. When the bit is high the count is finished and result is ready may be given as: FREQ[31:0] = {TR25,TR26,TR27,TR28}	0	R

2.17 Power Supply System

2.17.1 Primary Power Supply

There are two possible sources of power, depending on the working mode:

- Stand-alone Mode—external 12VDC @ 4A Power Supply with Power Switch S1 is “ON”.
- AMC Mode—12V from microTCA backplane when Power Switch S1 is “OFF”.

The External 12V Power Supply is a standard power supply. Its parameters are:

- Vin = 100V—240V AC @ 50-60Hz
- Vout = 12VDC±5% @ 5.5A

2.17.2 Power Supply Operation

The secondary power system is built on the MAXYZ family of power supplies, produced by Power-One. The power supply includes the ZM308G Power Manager-DPM and several POL converters for each power rail. The ZM308G is a fully programmable digital power manager that utilizes the industry-standard I^2C communication bus interface to control, manage, program and monitor up to 8 Z-series POL converters. The ZM308G completely eliminates the need for external components for power management and POL converters programming, monitoring, and reporting. Parameters of the ZM308G are programmable via the I^2C bus and can be changed by a user at any time during product development and service.

MSC8156 Power-UP sequence is programmed into the Power Manager device’s non-volatile memory. **Figure 2-17** shows power distribution.

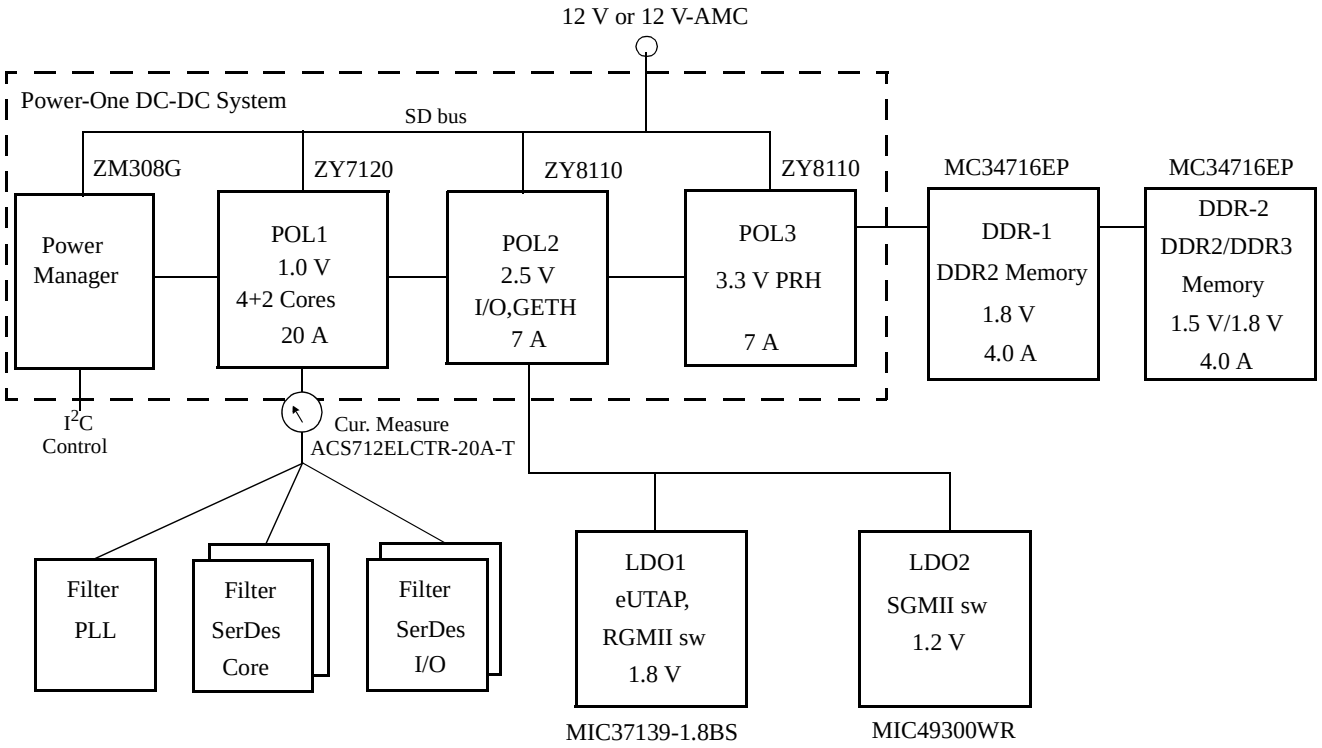


Figure 2-17. Power Distribution Scheme

The POL1 providing core voltage for MSC8156 has jumpers on 1.0 V power rail to isolate two cores from six, for better power save. The Hall effect part in series with cores load is intend for current measurement. The existing FPGA I^2C master controller adjusts the core power supply to the programming voltage. The DDR-2 port power supply is self-adjusted according to the type of DDR parts inserted in the SODIMM. A DDR3 module requires a 1.5 V power supply, while the DDR2 module uses a DDR3-DDR2 interposer card and the power supply applies 1.8 V. Vtt and Vref voltages are set accordingly.

The U51 Hall current sensor device measures current consumption of the MSC8156 1.0V power supply.

Note: Supporting one/two/four-core DSPs requires that J2002-J2003 and J2004-J2005 power jumpers be opened as shown in **Figure 2-18**.

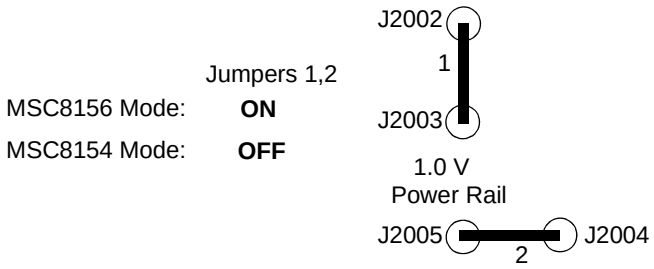


Figure 2-18. Power Rails Disconnect Scheme

2.17.3 Power-Up Sequence

MSC8156 family DSPs require the following power-up sequence:

- 1.0 V supplies should rise before any other supplies in any sequence: VCORE,VPLL,VMAPLE, VM3,VSXP, VSXC.
- After the 1.0 V supplies rise to 90% of their nominal value, the other DSP 2.5 V I/O supply rise.

The Power-One Power Manager program setting provides the required power-up sequence.

2.18 Separate LEDs

MSC8156ADS LEDs are described in **Table 2-52**.

Table 2-52. LED Descriptions

Ref.	Name	Color	LED On	LED Blinking	LED Off[a]
LEDs in J8	1G	Green	RGMII phy -1 has Link at 1Gbps	Activity	No link on Port1
	100M	Orange	RGMII phy -1 has Link at 100Mbps		
LEDs in J11	1G	Green	RGMII phy -2 has Link at 1Gbps	Activity	No link on Port2
	100M	Orange	RGMII phy -2 has Link at 100Mbps		
LD3	HOST	Multicolor	eUTAP mode indication[b].	—	—
LD4	TARGET	Multicolor	eUTAP mode indication[c].	—	—
LD5	BOOT	Green	Boot is from I2C or Serial Flash	—	Regular operation
LD6	SIG2	Green	BCSR12.2 is low.	Internal JTAG controller is active	BCSR12.2 is high.
LD7	SIG0	Green	BCSR12.0 is low, or SRESET is asserted	—	BCSR12.0 is high, and SRESET is not asserted.
LD8	DEBUG	Green	MSC8156 in Debug mode	—	MSC8156 not in Debug mode
LD9	SIG3	Green	BCSR12.3 is low.	—	BCSR12.3 is high.
LD10	SIG1	Red	BCSR12.1 is low, or HRESET is asserted	—	BCSR12.1 is high, or HRESET is asserted.
LD11	PRG	Green	FPGA Programming	—	FPGA firmware is ready
LD12	2-digit ABC Display	-	Controlled by FPGA. See description in *Two-Digit LED Display*	—	—
LD13	12V	Green	Indicates external power is ON(*) or AMC 12V Power	—	The ADS is power off
LD14	PG	Green	Power Good	—	Internal power supply fail(*)
(*) Critical indicator					

a. If LEDDIS bit in BCSR12.5 is high all LEDs are OFF except RJ45 built-in LEDS, POWER, PG and eUTAP.
b. Like Transmit/Receive indicator on USB TAP device:
The LED LD3 flashes **red** when the eUTAP is powered but has not been configured
The LED LD3 flashes **green** when the eUTAP is properly configured
The LED LD3 flashes **orange** when data is being transferred.

c. Like Run/Pause Indicator indicator on USB TAP device:
The LED LD4 is **green** when the target is running.
The LED LD4 is **red** when the target is paused.
The LED LD4 is **orange** when the target is in mixed mode.
The LED LD4 is initially unlit and remains so until the debugger is connected to the eUTAP.

2.19 Two-Digit LED Display

The KCPDA04-102 is Kingbright Super Bright Green two-digit alphanumeric display. Each of the two 14-segment displays is accompanied, to the right, by a single dot-digit point. The scroll display LED connects to a 16-bit LED driver via a parallel interface. The FPGA supplies data to the 16-bit LED driver via a serial interface; this method saves FPGA I/O pins. The serial interface includes four control signals, CLOCK, SIN, LATCH and BLANK. The main FPGA generates different scroll displays that indicate MSC8156 configuration modes. The asterisk (*) symbol separates, for easier reading, between the header name and the mode value. Scroll display banner readings include the following:

- **RCW** source values:
  - **4CYC** indicates multiplexed external RCW loading where the RCW is driven by external logic on RC[15–0].
  - **RDUC** is Reduced Configuration word from RC[21-0].
  - **I2CS** shows RCW is loading from an I2C (small) EEPROM with less than 4KB of memory.
  - **I2CB** shows RCW is loading from an I2C (big) EEPROM with more than 16KB of memory.
  - **HDC1** or **HDC2** means RCW source is an internal hardcoded option for 1 or 2, respectively.
- **GE/TDM** denotes a selected function on the MSC8156 MUX port:
  - **GE** indicates an active RGMII Ethernet I/F.
  - **TDM** indicates selection of TDM ports 0 to 3.
- **ETH** indicates that DIP-switches SW5.5-5.6 permit the selection of varying RGMII and SGMII mode combinations for both GE ports. The display shows **RGMII1.SGMII2**.
- **BOOT** defines a selected boot source.
  - **I2C:** I^2C EEPROM
  - **SPI:** SPI serial flash
  - **SRIO:** Serial RapidIO port over AMC edge connector
  - **RGMII1** or **RGMII2:** Boot from appropriate Ethernet RGMII port.
  - **SGMII1** or **SGMII2:** Boot from appropriate Ethernet SGMII port.

2.20 Push-Buttons

Table 2-53 below describes the push-button functionality.

Table 2-53. The MSC8156ADS Push Buttons

Name and Description	Depiction	Function
SW11 Soft Reset	 SRESET	Pressing button SW11results in a Soft Reset for the MSC8156. Despite the reset, clock and chip-select data contents are retained.
SW9 Hard Reset	 HRESET	Pressing button SW9 results in a Hard Reset for the MSC8156.
SW8 Power-on-Reset	 PRESET	Pressing button SW8 results in Power-On-Reset for ***all components*** on the MSC8156ADS.
SW10 NMI (Abort)	 NMI	Pressing button SW10 results in aborting program execution by issuing a level 0 interrupt to the MSC8156. Sets pin EE0 to high.
SW12 Scroll	 SCROLL	The Display scrolling. Pressing button SW12 results invoking the next indication row.

2.21 Jumpers

MSC8156ADS jumpers settings are described in **Table 2-54**.

Table 2-54. Jumpers

Jumper	Name	Description
JP1	AMC EXP	AMC JTAG expansion: • When **CLOSED.** The JTAG chain expands over AMC-X-Over card. GA value define order in JTAG chain. • When **OPEN**. No JTAG chain outside the board. Default setting: OPEN
JP2	PRESET	Power-ON-Reset: • When **CLOSED**. Board stays in continuos reset • When **OPEN.** Normal mode. Default setting is OPEN
JP3	CLK SEL	Selects MSC8156 CLOCKIN source: • When 1-2 is **CLOSED.** Source is in-socket clock oscillator • When 2-3 is **CLOSED**. Source is external (pulse generator) • When the jumper is **OPEN**. Source is clock synthesizer Default setting is 1-2
JP1000	PRG	Force FPGA programming mode: • When 1-2 **CLOSED,** the FPGA is chosen for reprogramming over the eUTAP. • When 2-3 **CLOSED**, the FPGA is chosen for reprogramming over the J1000 ISP connector with the Lattice programmer. • When the jumper is **OPEN**, normal mode is selected. Default setting is **OPEN.**

2.22 Socket with Heatsink

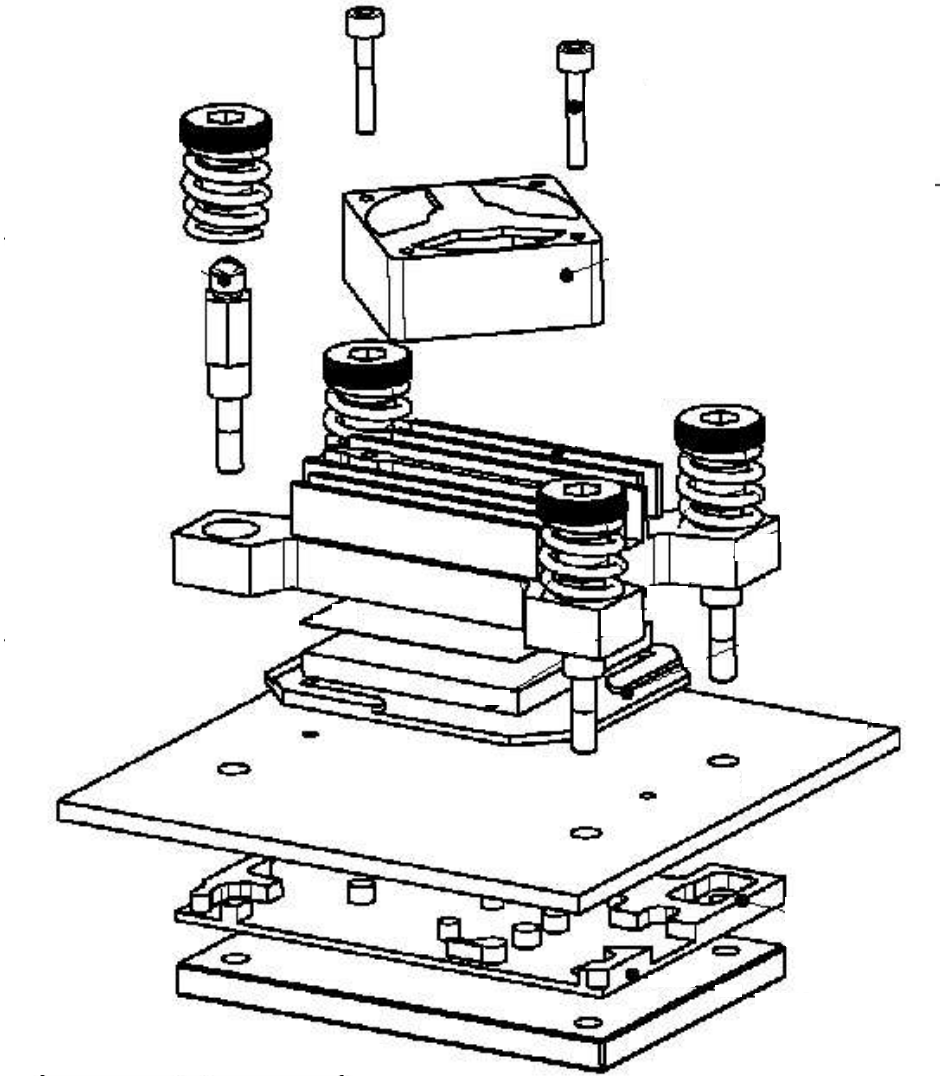


Figure 2-19. MSC8156 Solderless Socket with Heatsink and Fan

The MSC8156 socket is a solderless type. The socket vendor is Tyco.Typical socket is shown on **Figure 2-19**. A fan assembled on top of the heat sink improves thermal parameters. The socket can dissipate at least 15 W of power.

Expansion Options 3

The MSC8156ADS has two options for expansion: a connection for a PTMC expansion card, and an AMC edge connector. Modules for these connections are supplied by third-party vendors, not Freescale Semiconductor.

The PTMC expansion connection (with appropriate third-party card) allows expanded Ethernet and video capabilities and can serve as a verification tool.

The AMC edge connector (with the appropriate third-party connecting device) allows two MSC8156ADS boards to be connected back-to-back, or alternatively, allows a MSC8156ADS to be connected to a TUNDRA device or any other ATCA system.

3.1 PMC Expansion Connection

The PTMC expansion connection (with appropriate third-party card) allows expanded ethernet and video capabilities and can serve as a verification tool for the MSC8156ADS.

Its feature list is following:

- Compliance with PT3MC PMC configuration pinout and form-factor. Includes clock sources for four MSC8156 TDM ports.
- All PTMC signals on test headers are visible with a 0.1” separation between them.n

Table 3-1. PMC Pinout

PT3MC standard definition[a]		MSC815x Signal	MSC815x Port	Comment/Power
CON	Pin Name			
J1-1	*TCK*	-	-	
J1-2	*-12V*	-	-	
J1-3	*GND*	GND	-	
J1-4	*INTA#*	GPIO14	GPIO	**2.5 V**
J1-5	*INTB#*	GPIO15	GPIO	**2.5 V**
J1-6	*INTC#*	GPIO16	GPIO	**2.5 V**
J1-7	*BUSMODE1#*	-	-	“Card Present”, Pull-Up on the ADS, GND on PMC
J1-8	*+5 V*	-	-	-
J1-9	*INTD#*	GPIO17	GPIO	**2.5 V**
J1-10	*RSRV*	-	-	

Table 3-1. PMC Pinout (Continued)

PT3MC standard definition[a]		MSC815x Signal	MSC815x Port	Comment/Power
CON	Pin Name			
J1-11	*GND*	GND	-	
J1-12	*3.3Vaux*	-	-	
J1-13	*CLK*	GPIO18	GPIO	**2.5 V**
J1-14	*GND*	GND	-	
J1-15	*GND*	GND	-	
J1-16	*GNT#*	GPIO19	GPIO	**2.5 V**
J1-17	*REQ#*	GPIO20	GPIO	**2.5 V**
J1-18	*+5V*	-	-	**-**
J1-19	*V(I/O)*	-	-	**+2.5 V DC**
J1-20	*AD31*	GPIO21	GPIO	**2.5 V**
J1-21	*AD28*	GPIO22	GPIO	**2.5 V**
J1-22	*AD27*	GPIO23	GPIO	**2.5 V**
J1-23	*AD25*	GPIO24	GPIO	**2.5 V**
J1-24	*GND*	GND	-	
J1-25	*GND*	GND	-	
J1-26	*C/BE3#*	GPIO25	GPIO	**2.5 V**
J1-27	*AD22*	GPIO26	GPIO	**2.5 V**
J1-28	*AD21*	GPIO27	GPIO	**2.5 V**
J1-29	*AD19*	GPIO30	GPIO	**2.5 V**
J1-30	*+5V*	-	-	**-**
J1-31	*V(I/O)*	-	-	**+2.5 V DC**
J1-32	*AD17*	GPIO31	GPIO	**2.5 V**
J1-33	*FRAME#*	nNMI_OUT	Interrupt	**-**
J1-34	*GND*	GND	-	
J1-35	*GND*	GND	-	
J1-36	*IRDY#*	-	-	**-**
J1-37	*DEV_SEL*	nINT_OUT	Interrupt	**-**
J1-38	*+5V*	-	-	**-**
J1-39	*GND*	GND	-	
J1-40	*LOCK#*	-	-	**-**
J1-41	*RSRV*	-	-	**-**
J1-42	*RSRV*	-	-	**-**
J1-43	*PAR*	-	-	**-**
J1-44	*GND*	GND	-	
J1-45	*V(I/O)*	-	-	**+2.5 V DC**

Table 3-1. PMC Pinout (Continued)

PT3MC standard definition[a]		MSC815x Signal	MSC815x Port	Comment/Power
CON	Pin Name			
J1-46	*AD15*	-	-	-
J1-47	*AD12*	-	-	-
J1-48	*AD11*	-	-	-
J1-49	*AD09*	-	-	-
J1-50	*+5V*	-	-	-
J1-51	*GND*	GND	-	
J1-52	*C/BE0#*	-	-	-
J1-53	*AD06*	-	-	-
J1-54	*AD05*	-	-	-
J1-55	*AD04*	-	-	-
J1-56	*GND*	GND	-	
J1-57	*V(I/O)*	-	-	**+2.5 V DC**
J1-58	*AD03*	-	-	-
J1-59	*AD02*	-	-	-
J1-60	*AD01*	-	-	-
J1-61	*AD00*	-	-	-
J1-62	*+5V*	-	-	-
J1-63	*GND*	GND	-	
J1-64	*REQ64#*	-	-	-
J3-1	*MDIO*	GPIO0	GPIO	**2.5 V**
J3-2	*GND*	GND	-	
J3-3	*GND*	GND	-	
J3-4	*STX*	UTXD/GPIO29	UART	**2.5 V**
J3-5	*MDC*	GPIO1	GPIO	**2.5 V**
J3-6	*SRX*	URXD/GPIO28	UART	Set on-board RS-232 transc. disable for GPIO mode/ **2.5 V**
J3-7	*RxER*	GPIO2	GPIO	**2.5 V**
J3-8	*GND*	GND	-	
J3-9	*PTID2*	-	-	PTMC ID Pull-Down
J3-10	*TxD0*	GPIO3	GPIO	**2.5 V**
J3-11	*PTGNDZ*	-	-	Special Purpose GND
J3-12	*TxD1*	GPIO4	GPIO	**2.5 V**
J3-13	*REFCLK*	GPIO5	GPIO	**2.5 V**
J3-14	*GND*	GND	-	

Table 3-1. PMC Pinout (Continued)

PT3MC standard definition[a]		MSC815x Signal	MSC815x Port	Comment/Power
CON	Pin Name			
J3-15	*GND*	GND	-	
J3-16	*RxD0*	GPIO6	GPIO	-
J3-17	*CT_FA*	TDM0TSN	TDM0	Main TDM SYNC[b]/ **3.3 V**
J3-18	*RxD1*	GPIO7	GPIO	**2.5 V**
J3-19	*CT_FB*	TDM1TSN	TDM1	Add. SYNC1[c]/ **3.3 V**
J3-20	*GND*	GND	-	
J3-21	*PTID0*	-	-	PTMC ID Pull-Down
J3-22	*TXEN*	GPIO8	GPIO	**2.5 V**
J3-23	*PTGNDZ*	-	-	Special Purpose GND
J3-24	*CAS_DV*	GPIO9	GPIO	**2.5 V**
J3-25	*CT_C8A*	TDM0TCK	TDM0	Main TDM CLOCK/ **3.3 V**
J3-26	*GND*	GND	-	
J3-27	*GND*	GND	-	
J3-28	*CT_D19*	GPIO10	GPIO	**2.5 V**
J3-29	*CT_D18*	GPIO11	GPIO	**2.5 V**
J3-30	*CT_D17*	GPIO12	GPIO	**2.5 V**
J3-31	*CT_D16*	GPIO13	GPIO	-
J3-32	*GND*	GND	-	
J3-33	*GND*	GND	-	
J3-34	*NETREF2*	TDM2TSN	TDM2	Misc. Master SYNC[d]/ **3.3 V**
J3-35	*CT_D14*	TDM3RCK	TDM3	Any Mode/ **3.3 V**
J3-36	*USER1Z*	TDM3TSN	TDM3	Any Mode/ **3.3 V**
J3-37	*CT_D12*	TDM3RDT	TDM3	Any Mode/ **3.3 V**
J3-38	*GND*	GND	-	
J3-39	*PTENB#*[e]	-	-	PTMC Enable (low) BCSR bit Pull-Up 47k
J3-40	*USER2Z*	TDM3TCK	TDM3	Any Mode/ **3.3 V**
J3-41	*PTGNDZ*	-	-	Special Purpose GND
J3-42	*NETREF1*	TDM2TCK	TDM2	Misc. Master CLOCK[d]/ **3.3 V**

Table 3-1. PMC Pinout (Continued)

PT3MC standard definition[a]		MSC815x Signal	MSC815x Port	Comment/Power
CON	Pin Name			
J3-43	*CT_C8B*	TDM1TCK	TDM1	Secondary Master Clock[f]/ **3.3 V**
J3-44	*GND*	GND	-	
J3-45	*GND*	GND	-	
J3-46	*CT_D15*	TDM3TDT	TDM3	Any Mode/ **3.3 V**
J3-47	*CT_D10*	TDM2RCK	TDM2	Any Mode/ **3.3 V**
J3-48	*CT_D13*	TDM3RSN	TDM3	Any Mode/ **3.3 V**
J3-49	*CT_D8*	TDM2RDT	TDM2	Any Mode/ **3.3 V**
J3-50	*CT_D11*	TDM2TDT	TDM2	Any Mode/ **3.3 V**
J3-51	*GND*	GND	-	
J3-52	*CT_D9*	TDM2RSN	TDM2	Any Mode/ **3.3 V**
J3-53	*CT_D6*	TDM1RCK	TDM1	Any Mode/ **3.3 V**
J3-54	*CT_D7*	TDM1TDT	TDM1	Any Mode/ **3.3 V**
J3-55	*CT_D4*	TDM1RDT	TDM1	Any Mode/ **3.3 V**
J3-56	*GND*	GND	-	
J3-57	*PTID1*	-	-	PTMC ID Pull-Down
J3-58	*CT_D5*	TDM1RSN	TDM1	Any Mode/ **3.3 V**
J3-59	*CT_D2*	TDM0RCK	TDM0	Any Mode/ **3.3 V**
J3-60	*CT_D3*	TDM0TDT	TDM0	Any Mode/ **3.3 V**
J3-61	*CT_D0*	TDM0RDT	TDM0	Any Mode/ **3.3 V**
J3-62	*GND*	GND	-	
J3-63	*GND*	GND	-	
J3-64	*CT_D1*	TDM0RSN	TDM0	Any Mode/ **3.3 V**

a. Correct for TDM signals only.
b. To support CT-bus over PTMC MSC815x TDM ports 0 to 3 should be configured in “Shared Frame Sync, Clock, and Data Links” Mode. TDM signal are 2.5 V domain, friendly to 3.3 V environment.
c. Acts as Rxsync for Shared Modes

d. Use for TDM Independent Mode
e. PCI Telecom Enable PTENB#. This signal should prevent available circuit damage for combinations with PTCC cards.
f. Acts as Rxclk for Shared Modes

3.2 AMC in ATCA Environment

The card may be plugged into AMC carrier via a 170 pin edge B+ connector. That allows MSC8156ADS to connect to a TUNDRA device on the TUNDRA backplane, or any other ATCA system. Using proprietary AMC back-to- back adaptor card two MSC8156ADS boards may be tested together.

Table 3-2 describes the signals that are routed to the AMC edge connector.

Table 3-2. AMC Edge Connector Assignment

Pin #	AMC Name	Connection to MSC815x	ATCA Carrier Board Signal
3	PS1	-	Power Sense 1 Connect to 83 on the ADS
4	3V3MP	-	3 V power to AMC
6	RSRV	nAMC_HRST from/to FPGA	Enable for AMC B2B expander only
11,12	TX0+/-	GE1 through SGMII Switch Port x	
14,15	RX0+/-		
29,30	TX2+/-	GE2 through SGMII Switch Port x	
32,33	RX2+/-		
41	ENABLE#	-	PU. To MMC on ADS
44,45	TX4+/-	SerDes2_TX0+/-	Serial RapidIO/PCI-e 1x
47,48	RX4+/-	SerDes2_RX0+/-	
50,51	TX5+/-	SerDes2_TX1+/-	Serial RapidIO/PCI-e 4x
53,54	RX5+/-	SerDes2_RX1+/-	
56	SCL_L	-	I^2C to ADS MMC (optional)
59,60	TX6+/-	SerDes2_TX2+/-	Serial RapidIO/PCI-e 4x
62,63	RX6+/-	SerDes2_RX2+/-	
65,66	TX7+/-	SerDes2_TX3+/-	
68,69	RX7+/-	SerDes2_RX3+/-	
71	SCA_L	-	I^2C to ADS MMC (optional)
80,81	CLK3+/-	Diff clock	PCI-E clock
83	PS0		Power Sense 0 Connect to 3 on the ADS

Table 3-2. AMC Edge Connector Assignment (Continued)

Pin #	AMC Name	Connection to MSC815x	ATCA Carrier Board Signal
87,88	RX8+/-	SerDes1_RX0+/-	Serial RapidIO 1/4x
90,91	TX8+/-	SerDes1_TX0+/-	
93,94	RX9+/-	SerDes1_RX1+/-	
96,97	TX9+/-	SerDes1_TX1+/-	
99,100	RX10+/-	SerDes1_RX2+/-	
102,103	TX10+/-	SerDes1_TX2+/-	
105,106	RX11+/-	SerDes1_RX3+/-	
108,109	TX11+/-	SerDes1_TX3+/-	
111	RX12-	Fxdata0(TDM0RDT)	ST_D00
112	RX12+	Fxdata1(TDM0RSN)	ST_D01
114	TX12-	Fxdata2(TDM0RCK)	ST_D02
115	TX12+	Fxdata3(TDM0TDT)	ST_D03
117	RX13-	Fxdata4(TDM1RDT)	ST_D04
118	RX13+	Fxdata5(TDM1RSN)	ST_D05
120	TX13-	Fxdata6(TDM1RCK)	ST_D06
121	TX13+	Fxdata7(TDM1TDT)	ST_D07
123	RX14-	Fxdata8(TDM2RDT)	ST_D08
124	RX14+	Fxdata9(TDM2RSN)	ST_D09
126	TX14-	Fxdata10(TDM2RCK)	ST_D10
127	TX14+	Fxdata11(TDM2TDT)	ST_D11
129	RX15-	Fxdata12(TDM3RDT)	ST_D12
130	RX15+	Fxdata13(TDM3RSN)	ST_D13
132	TX15-	Fxdata14(TDM3RCK)	ST_D14
133	TX15+	Fxdata15(TDM3TDT)	ST_D15
...	-	-	-
162	TX20-	Fxsync (TDM0TSN)	ST_FA
163	TX20+	Fxclk (TDM0TCK)[a]	ST_8A
165	TCLK	TCKamc	The AMC B2B expander allows to link two ADS boars over JTAG ports. If GA = 0 the ADS is JTAG source and the second board with GA=1 is JTAG destination
166	TMS	TMSamc	
167	nTRST	nTRSTamc	
168	TDO	TDOamc	
169	TDI	TDIamc	

a. MSC8144 TDM ports is in “Shared Frame,Sync,Clock and Data Link” mode

Boot Code A

A.1 Boot Sequencer Assembler Code

The Boot Sequencer has three functions:

- GETH PHY is configured from RGMII to MSC815x Boot-over-Ethernet mode immediately following ADS Power-on-Reset.
- Isolates GETH PHY for TDM port testing.
- Displays die temperature by polling the Temperature Sense.

Achieve GETH PHY functions by programming the GETH PHYs over the MII bus when the RCW corresponds to the following: GE-enabled in RGMII configuration or TDM selected (instead of RGMII).

Temperature Sense polling is done over an I^2C bus with an initialized FPGAs I^2C Master Controller. When polling, other common I^2C bus options become unavailable such as boot over I^2C, DDR SPD read, I^2C EEPROM programming, and so forth.

There are two ways to activate Temperature Sense polling:

- Press the “SCROLL” push button twice to set the default mode; there will be no polling.
- Clear the BCSR12.6 TSENSE bit.

The FPGA RAM block, EBR, hold the Boot Sequencer code. The code is loaded from the FPGA internal Flash during Power-ON and begins to run when triggered from the BCSR_main module.

The Boot Sequencer stops when the fetched command code is zero. See the BSA (Boot Sequencer Assembler) file in Section A.2, **Boot Sequencer Assembler File**.. Commands are described in **Table 2-11** on page 2-23. The compiler, using the Perl programming language, applies binary parsing to the source code.

A.2 Boot Sequencer Assembler File

```
//  Boot seq assembler
//  for 8156ADS rev Pilot
//
// Configure RGMII phys 0x1 and 0xa when SRESET asserted
//  According to SDOS initialize :
//      ads_phy_write 0xfee02000 0x1 0x0 0x0940
//      ads_phy_write 0xfee02000 0x1 0x14 0x0ce2
//      ads_phy_write 0xfee02000 0x1 0x1b 0x800b
//      ads_phy_write 0xfee02000 0x1 0x9 0x0300
//      ads_phy_write 0xfee02000 0x1 0x4 0x051e
//      ads_phy_write 0xfee02000 0x1 0x0 0x8140
//      ads_phy_write 0xfee02000 0x1 0x0 0x0140
```

```
//              09.06.09
     JMP  1                 // Phy N1 is in RGMII mode - add delay for clock
     JMP  2                 // Phy N2 is in RGMII mode - add delay for clock
     JMP  3                 // Two phys are in RGMII mode - add delay for clock
     JMP  4                 // Need to insert phys into isolate mode because TDM mode
   LJMP 5                 // Read die Temperature Sensor
   LJMP 6                 // Read ambient Temperature Sensor
1:   WR BCSR,130x87       // Set SRESET continuously
     WR MII,10x80       // Enable to MII controller
B:   WR MII,20x01       // Phy1 address
A:   WR MII,3   0x1b       // Reg address
     WR MII,40x0b       // LSB
     WR MII,50x80       // MSB
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
                    WR MII,3   0x09
     WR MII,40x00
     WR MII,50x03
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
   WR MII,3   0x04
     WR MII,40x1e
     WR MII,50x50
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
     WR MII,30x14
     WR MII,40xe2
     WR MII,50x0c
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010 // Wait for Ready
   WR MII,3   0x00
     WR MII,40x40
     WR MII,50x81
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
   WR MII,3   0x00
     WR MII,40x40
     WR MII,50x01
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
C:   WR MII,10          // Disable to MII controller
     WR BCSR,130xC7       // Release SRESET
     END
2:   WR BCSR,130x87       // Set SRESET continuously
     WR MII,10x80       // Enable to MII controller
     WR MII,20x0a       // Phy2 address
     JMP A
3:   WR BCSR,130x87       // Set SRESET continuously
     WR MII,10x80       // Enable to MII controller
   WR MII,20x0a       // Phy2 address
     WR MII,3   0x1b       // Reg address
```

```
     WR MII,40x0b       // LSB
     WR MII,50x80       // MSB
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
   WR MII,3   0x09
     WR MII,40x00
     WR MII,50x03
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
   WR MII,3   0x04
     WR MII,40x1e
     WR MII,50x05
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
     WR MII,30x14
     WR MII,40xe2
     WR MII,50x0c
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
   WR MII,3   0x00
     WR MII,40x40
     WR MII,50x81
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
   WR MII,3   0x00
     WR MII,40x40
     WR MII,50x01
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
   JMP B                 // To phy 1 init

4:   WR BCSR,130x87       // Set SRESET continuously
     WR BCSR,9  0x3b       // Disable reset to RGMII1,2 phy
     WR MII,10x80       // Enable to MII controller
   WR MII,20x01       // Phy1 address
     WR MII,30x0        // Reg address
     WR MII,40x00       // LSB
     WR MII,50x04       // MSB set bit 10 for isolate mode
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
   WR MII,20x0a       // Phy2 address
     WR MII,10x82       // Start write transaction over MII
     RD MII,80x010  // Wait for Ready
     WR BCSR,8  0x1E       // Disable to Clock Buffer
   WR BCSR,9  0x7b       // Enable TDM Framer
     JMP C
// Read die temperature sensor
5:   WR  I2CM,2  0x80       // Enable to I2C Master Controller
     WR  I2CM,0  0x3f       //
     WR  I2CM,1  0x00       // Set I2C speed 100kHz
//  Configure the sensor
```

```
   WR  I2CM,3  0x4c       // Temp Sensor addr on I2C bus
   WR  I2CM,4  0x90       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,3  0x0a       // Thermal_Diode_Conversion_Rate_Write_Addr
   WR  I2CM,4  0x10       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,3  0x07       // Write 0x7
   WR  I2CM,4  0x58       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
// Read from sensor
   WR  I2CM,3  0x4c       // Temp Sensor addr on I2C bus
   WR  I2CM,4  0x90       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,3  0x01       // Thermal_Diode_External_Temperature_Value_High_Byte_Read_Addr
   WR  I2CM,4  0x10       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,3  0x4d       // Read command
   WR  I2CM,4  0x90       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,4  0x68       // Command to write
   RD  I2CM,4  0x81  0x81 // Wait to finish
   RTA I2CM,3             // Read temperature value into accumulator
   WR  I2CM,2  0x00       // Disable to I2C Master Controller
   WFA BCSR,21            // Write to the User's Display Register
// Read ambient temperature sensor
6:   WR  I2CM,2  0x80       // Enable to I2C Master Controller
     WR  I2CM,0  0x3f       //
     WR  I2CM,1  0x00       // Set I2C speed 100kHz
//  Configure the sensor
   WR  I2CM,3  0x4c       // Temp Sensor addr on I2C bus
   WR  I2CM,4  0x90       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,3  0x0a       // Thermal_Diode_Conversion_Rate_Write_Addr
   WR  I2CM,4  0x10       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,3  0x07       // Write 0x7
   WR  I2CM,4  0x58       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
// Read from sensor
   WR  I2CM,3  0x4c       // Temp Sensor addr on I2C bus
   WR  I2CM,4  0x90       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,3  0x00       // Thermal_Diode_Local_Temperature_Value_Read_Addr
   WR  I2CM,4  0x10       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,3  0x4d       // Read command
   WR  I2CM,4  0x90       // Command to write
   RD  I2CM,4  0x41  0x41 // Wait to finish
   WR  I2CM,4  0x68       // Command to write
   RD  I2CM,4  0x81  0x81 // Wait to finish
   RTA I2CM,3             // Read temperature value into accumulator
```

```
   WR  I2CM,2  0x00       // Disable to I2C Master Controller
     WFA BCSR,21            // Write to the User's Display Register
   END
// End of boot
```