REVISIONS

LTR	DESCRIPTION	DATE (YR MO DAY)	APPROVED
A	Add one vendor, CAGE 65786. Add device types 03 and 04. Add margin test, programming procedure, waveform, and flowchart for method B. Add case outline letter K.	88-10-25	M. A. Frye
B	Add "Changes in accordance with NOR 5962-R103-92."	91-12-24	M. A. Frye
C	Redraw with changes. Add device type 05 for vendor CAGE 65786. Changes to margin methods A and B. Add vendor CAGE 66759 as a source of supply for device types 01JX, 01LX, and 013X with vendor similar part number changes. Editorial changes throughout.	93-03-23	M. A. Frye
D	Made correction to paragraph 1.2.2 for case outline 3, under package style change rectangular to square. Updated drawing to the latest format. Redrew entire document. -sld	02-10-30	Raymond Monnin
E	Made correction to paragraph 1.2.1 and added additional vendor similar PIN numbers for device types 03 and 05 on the Standard Microcircuit Drawing Bulletin. -sld	02-12-16	Raymond Monnin
F	Boilerplate update and part of five year review. tcr	07-11-01	Robert M. Heber

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS															
REV	F	F	F	F	F	F	F	F	F	F	F			
SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY
Rick Officer

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Charles Reusing

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

APPROVED BY
Michael. A. Frye

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K x 8 UV ERASABLE PROM, MONOLITHIC SILICON

DRAWING APPROVAL DATE
88-01-04

AMSC N/A

REVISION LEVEL
F

SIZE	CAGE CODE	
A	**67268**	**5962-87650**

SHEET
1 OF 11

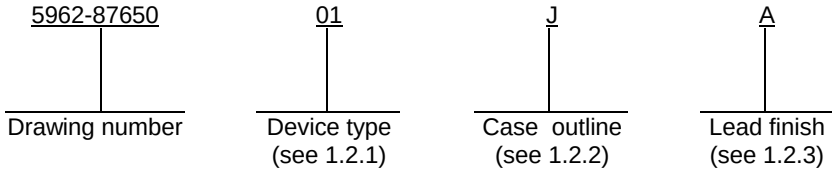
DSCC FORM 2233
APR 97

5962-E035-08

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WS57C191-50, CY7C291-50	2K x 8 UV EPROM	50 ns
02	WS57C191-55	2K x 8 UV EPROM	55 ns
03	7C291-35, CY7C291-35, WS57C291C-35	2K x 8 UV EPROM	35 ns
04	WS57C191B-45	2K x 8 UV EPROM	45 ns
05	7C291A-25, WS57C291C-25	2K x 8 UV EPROM	25 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style 1/
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	Flat package
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Voltages on any pin with respect to ground	-0.6 V dc to +7.0 V dc
V_{PP} with respect to ground	-0.6 V dc to +14.0 V dc
Power dissipation (P_D)	550 mW 2/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Endurance	50 cycles/byte, minimum
Data retention	10 years, minimum

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). See 3.2.3.1 and 3.2.3.2.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.6.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroups 7 and 8) to verify that all bits are in proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing

3.10 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	-0.5 2/	0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	2.0	V_{CC} +0.5 2/	V
Output low voltage 3/	V_{OL}	I_{OL} = 16 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All		0.45	V
Output high voltage 3/	V_{OH}	I_{OH} = -4 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All	2.4		V
Output short circuit current 2/	I_{OS}	V_{CC} = 4.5 V and 5.5 V, V_{OUT} = GND	1,2,3	All		200	mA
Input load current 4/	I_{LI}	V_{IN} = 5.5 V and GND	1,2,3	All		±10	µA
Output leakage	I_{LO}	V_{OUT} = 5.5 V and GND	1,2,3	All		±10	µA
Operating current, TTL inputs 5/ 6/ 7/	I_{CC} TTL	$\overline{CS1}$ = V_{IL}, V_{CC} = 5.5 V, O_0 to O_7 = 0 mA, CS2 = CS3 = V_{IH}, addresses cycling between 0 V and 3 V	1,2,3	All		120	mA
Operating current , CMOS inputs 2/ 7/ 8/	I_{CC} CMOS	$\overline{CS1}$ = V_{IL}, V_{CC} = 5.5 V, O_0 to O_7 = 0 mA, CS2 = CS3 = V_{IH}	1,2,3	All		120	mA
Input capacitance	C_{IN}	V_{IN} = 0, see 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT}	V_{OUT} = 0, see 4.3.1c	4	All		12	pF
Address to output delay	t_{ACC}	$\overline{CS1}$ = V_{IL}, CS2 = CS3 = V_{IH}, See figures 4 and 5	9,10,11	01		50	ns
				02		55	
				03		35	
				04		45	
				05		25	
All chip selects to output delay	t_{CS}	Either $\overline{CS1}$, CS2 or CS3 9/ See figures 4 and 5	9,10,11	01,03, 04		25	ns
				02		30	
				05		20	
All chip selects high to output float 2/	t_{DF}	Either $\overline{CS1}$, CS2 or CS3 9/ See figures 4 and 5	9,10,11	01,02, 03,04		25	ns
				05		20	
Address to output hold 2/	t_{OH}	$\overline{CS1}$ = V_{IL}, CS2 = CS3 = V_{IH}, See figures 4 and 5	9,10,11	All	0		ns

See footnotes at top of next page.

TABLE I. Electrical performance characteristics -Continued.

1/ All electrical performance characteristics are 100 percent tested unless otherwise specified.

2/ May not be tested, but shall be guaranteed to the limits specified in table I.

3/ These are absolute voltages with respect to device ground pin and include all over shoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4/ Output shall be loaded in accordance with figure 4.

5/ TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.

6/ The frequency equals $1/t_{ACC}$ (maximum).

7/ The addresses, (A_0 - A_{10} pins), are toggling between V_{IL} and V_{IH}.

8/ CMOS inputs: V_{IL} = GND $\pm$0.3 V, $V_{IH} = V_{CC} \pm$0.3 V.

9/ Worst case of output control signal lines $\overline{CS1}$, CS2, or CS3.

Device types	All	
Case outlines	J, K, L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	CS3	O_5
19	CS2	O_6
20	$\overline{CS1}/V_{PP}$	O_7
21	A_{10}	NC
22	A_9	CS3
23	A_8	CS2
24	V_{CC}	$\overline{CS1}/V_{PP}$
25	---	A10
26	---	A9
27	---	A8
28	---	V_{CC}

FIGURE 1. Terminal connections.

Mode	$\overline{CS1}$ /V_{PP}	CS2	CS3	I/O pins
Program	V_{PP}	X	X	Data in
Read	V_{IL}	V_{IH}	V_{IH}	Data out
Deselect	V_{IH}	X	X	High-Z
Deselect	X	V_{IL}	X	High-Z
Deselect	X	X	V_{IL}	High-Z

NOTE: X means the input is a "don't care".

FIGURE 2. Truth table for unprogrammed devices.

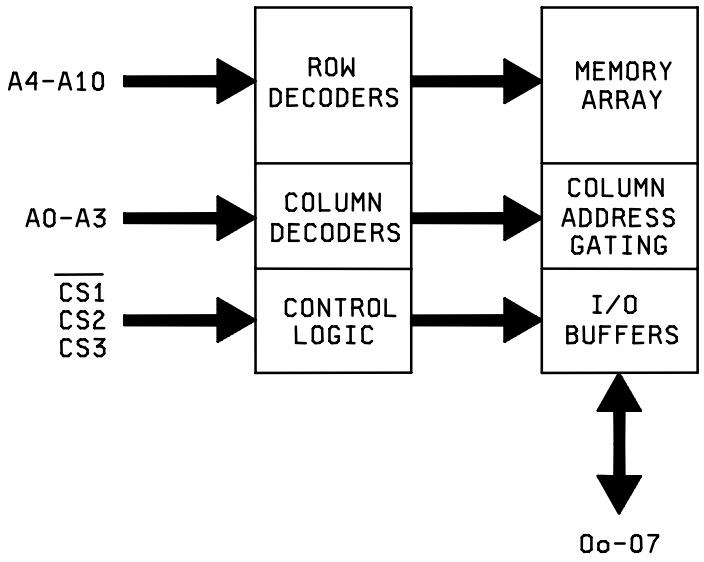
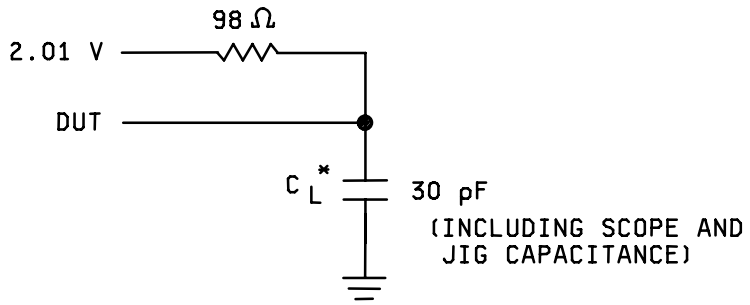


FIGURE 3. Block diagram.

High impedance test systems only



* t_{DF} is tested with C_L = 5 pF.

FIGURE 4. Output load (suggested).

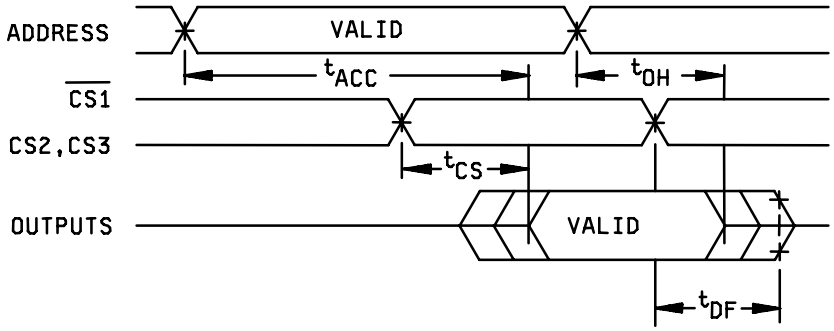


FIGURE 5. AC read timing diagram.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure. Margin methods shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of five (5) devices with zero failures shall be required.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedure. The device is erased by exposure to high intensity shortwave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the model S52 shortwave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about one inch from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * PDA applies to subgroup 1 and 7.
2/ ** See 4.3.1c.
3/ Any or all subgroup may be combined when using a high speed tester.
4/ Subgroup 7, 8A, and 8B shall consist of verifying the pattern specified.
5/ For all electrical tests, the device shall be programmed to the pattern specified.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-11-01

Approved sources of supply for SMD 5962-87650 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8765001JA	0C7V7	WS57C191C-50DMB
	0C7V7	QP7C292A-50WMB
5962-8765001KA	0C7V7	WS57C291C-50FMB
	0C7V7	QP7C291A-50TMB
5962-8765001LA	3/	CY7C291-50WMB
	0C7V7	WS57C291C-50TMB
	0C7V7	QP7C291A-50WMB
	0C7V7	7C291A-50/LA
5962-87650013A	0C7V7	WS57C291C-50CMB
	0C7V7	QP7C291A-50QMB
5962-87650013C	0C7V7	WS57C291C-50CMB
5962-8765002JA	0C7V7	WS57C191C-55DMB
	0C7V7	QP7C292A-55WMB
5962-8765002KA	0C7V7	WS57C291C-55FMB
	0C7V7	QP7C291A-55TMB
5962-8765002LA	0C7V7	WS57C291C-55TMB
	0C7V7	QP7C291A-55WMB
5962-87650023A	0C7V7	WS57C291C-55CMB
	0C7V7	QP7C291A-55QMB
5962-87650023C	0C7V7	WS57C291C-55CMB
5962-8765003KA	0C7V7	WS57C291C-35FMB
	0C7V7	7C291-35/KA
	0C7V7	QP7C291A-35TMB
5962-8765003LA	0C7V7	WS57C291C-35TMB
	0C7V7	7C291A-35/LA
	0C7V7	QP7C291A-35WMB
	65786	CY7C291-35WMB
5962-87650033A	0C7V7	WS57C291C-35CMB
	0C7V7	7C291-35/3A
	0C7V7	QP7C291A-35QMB
5962-87650033C	0C7V7	WS57C291C-35CMB
5962-8765003JA	0C7V7	QP7C292A-35WMB
5962-8765004JA	0C7V7	WS57C191C-45DMB
	0C7V7	QP7C292A-45WMB
5962-8765004KA	0C7V7	WS57C291C-45FMB
	0C7V7	QP7C291A-45TMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8765004LA	0C7V7	WS57C291C-45TMB
	0C7V7	QP7C291A-45WMB
5962-87650043A	0C7V7	WS57C291C-45CMB
	0C7V7	7C291A-45/3A
	0C7V7	QP7C291A-45QMB
5962-87650043C	0C7V7	WS57C291C-45CMB
5962-8765005KA	0C7V7	WS57C291C-25FMB
	0C7V7	7C291A-25/KA
	0C7V7	QP7C291A-25TMB
5962-8765005LA	0C7V7	WS57C291C-25TMB
	0C7V7	7C291A-25/LA
	0C7V7	QP7C291A-25WMB
5962-87650053A	0C7V7	WS57C291C-25CMB
	0C7V7	7C291A-25/3A
	0C7V7	QP7C291A-25QMB
5962-87650053C	0C7V7	WS57C291C-25CMB
5962-8765005JA	0C7V7	QP7C292A-25WMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134