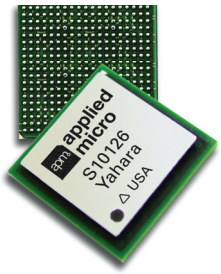
applied micro



Yahara - S10123, S10124, S10126

10G LAN/WAN/OTN Framer/Mapper/Phy with FEC

Supports 10GBase-R/10GBase-W, OC-192/STM64, 8G/10G FC, OTU-2 (Standard and Overclocked) Client Signals

Extensive Client Mapping Solutions into WIS and OTU-2 Line signals, including Bit Transparency, GFP-T/F, and WIS

Optical Line / Client Interfaces

- Two 10G Serial Interfaces supporting specific Line/Client baud rates from 8.5Gb/s to 11.32Gb/s
- SFI4.1 (16 x 622Mb/s to 708 Mb/s) Interface shared with Optical Client Interace
- Glue-less Interface to pluggable XFP/SFP+/MSA modules

Backplane Interface

- XAUI (3.125Gb/s or 3.1875Gb/s)
- SFI4.2 (2.19Gb/s to 2.94Gb/s)
- SFI-5s (2.125Gb/s to 2.85Gb/s)

Fully Compliant to IEEE802.3-2005, ITU G.709, and XFP4.0 Standards

On-Chip Fractional Clock Management Unit - only one reference clock required to generate all line rates for Metro/Carrier Ethernet Applications

Client Pass through support for LAN Phy and WAN Phy applications.

10GbE and fibre channel mapping modes support both fixed and non-fixed stuff bytes

OTN and TOH line overhead drop/insert support

Full OTN and SONET/SDH (WIS compliant) overhead monitoring

On-Chip 10GbE MAC for 10GbE overhead status monitoring

16-bit, 66MHz microprocessor interface for control and status monitoring

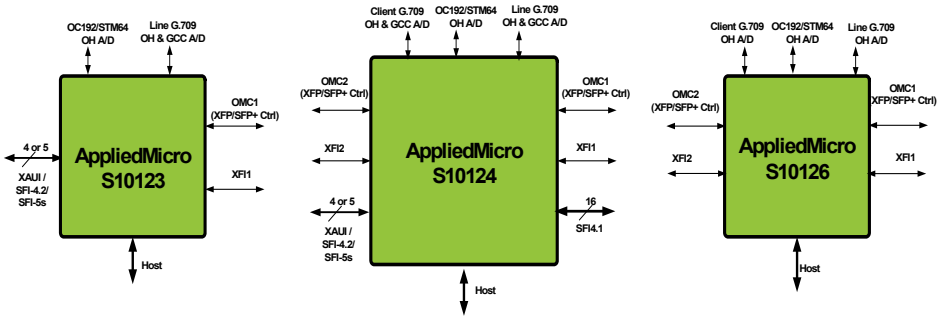
Integrated Optical Module 2-wire control Interface for XFP/SFP+ (compatible with I^2C)

Description

The Yahara S10123/S10124/S10126 is a 10G Framer/Mapper/PHY device for 10GbE/8G/10G Fibre Channel (LAN), OC-192/STM-64 (WIS/WAN), and OTU2 network applications. It is ideal for DWDM, Multi-Service Transport Platforms, and Metro-Ethernet Switch/Routers. The highly integrated device supports pure 10GbE LAN Metro-Ethernet networks, as well as WAN and OTN networks via its rich suite of 10GbE over WAN and OTN mapping modes. With integrated 10G XFI interfaces on both the client and line side interfaces, an OIF compliant SFI-4.1 interface for either the client or line Interface, flexible SFI-4.2/SFI-5s/XAUI system interface, and provisional G.709 standard and enhanced FEC features, it provides a highly integrated solution with seamless interfaces to XFP, SFP+, and tunable laser MSA optical modules. Yahara is available in a 25x25 footprint (S10124), with all interfaces bonded out, as well as in two smaller 19x19 footprint packages. The S10123 device includes the serial 10G line interface and system interface bonded out, while the S10126 includes two serial 10G line interfaces bonded out.

Applications

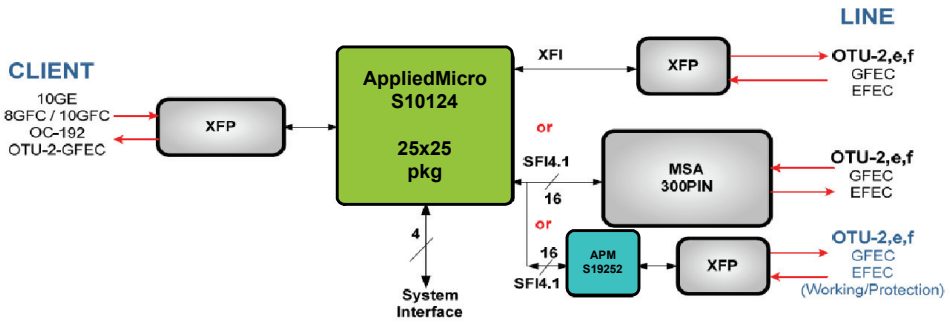
- Super-Framer/Mapper/Phy for LAN, WAN and OTN platforms and networks
- DWDM Equipment, Packet Optical Transport Systems (POTS), Multi-Service Transport Platforms (MSTPs), Switch/Routers
- Single chip 10G Transponder Applications
- 10GbE / OC-192 MSTP client tributary and line cards
- 10G "AnyRate" Line Card Applications
- 10GbE IEEE802.ae-ER/ZR uplink line card for enterprise switch applications
- OTU2 DWDM Client tributary/Line cards
- 10G Client Mapper Applications
- 10x10G to 100G Muxponder Application



System Block Diagram with the S10123/24/26

Yahara - S10123, S10124, S10126

Figure 1. S10124 in a Single Chip Full-Duplex Transponder FEC Regenerator Application



Technology, Package and Power

- Technology: 0.13 Micron CMOS
- Package: Two Options
  - S10123/S10126: 324 pin FC-BGA (Flip Chip Ball Grid Array), 19x19 mm body, 1.0 mm ball pitch
  - S10124: 576 pin FC-BGA, 25x25mm, 1.0 mm ball pitch
- Power supply Voltages: 1.2 V Core, 2.5 V CMOS I/O (3.3 V tolerant) and 1.8V for Analog I/O macros
- Power dissipation:
  - S10123: 1.93 - 3.05 Watts (Typical)
  - S10124: 3.28 - 4.31 Watts (Typical)
  - S10126: 2.65 - 3.40 Watts (Typical)
  - Power varies with operation modes and interfaces used
- S10123PBI (Leaded); S10123PSI (LeadFree)
- S10124PBI (Leaded); S10124PSI (LeadFree)
- S10126PBI (Leaded); S10126PSI (LeadFree)

The YAHARA Integrated Circuit is a highly integrated 10G Framer/Mapper with two on-chip serial 10G interfaces, making it ideal for 10G Client to Line Mapper, and GFEC to eFEC regenerator applications. Its serial interfaces enable 10GbE LAN, 8G/10G Fibre Channel, WIS (OC-192/STM-64), and ODU-2/OTU-2 network connections. The YAHARA is targeted towards Dense Wave Division Multiplexors, Packet Optical Transport Systems (POTs), Core Switch Routers, and Multi-Service-Transport-System (MSTP) applications.

The YAHARA device is offered in three bond-out options, a 19x19 sqmm package (S10123) for 10G Line Card Applications, a 25x25 sqmm package (S10124) for 10G Transponder applications and a second 19x19 sqmm package (S10126) for 10x10G to 100G muxponder applications.

The S10123 device provides a XAUI/SFI4.2/SFI-5s system/backplane interface and a 10Gb/s High Speed Serial Line Interface. Via its rich suite of mapping modes, the S10123 device can provisionally map 10GbE or 10G Fibre Channel into OTN and WIS Compliant signals. The mapped 10GbE or 10G Fibre Channel traffic can be transported over OTN, WIS (SONET/SDH) networks. Additionally, 8G Fibre Channel can be GFP-T mapped and transported over OTN networks. S10123 also supports OTN and WIS bypass modes to enable pure LAN Phy applications for 10GbE and 10G Fibre Channel signals.

S10123 also sports two 10G MACs for full 10GbE traffic monitoring on both the Transmit and Receive datapaths of the device.

S10123 also provides SONET/SDH Line/Section monitoring of OC-192/STM-64 signals, OTN overhead monitoring of OTU-2/ODU-2 signals, and PCS monitoring of 10GbE and 10G/8G Fibre Channel client signals.

The S10123 also supports OTU-2 and WIS (OC-192/STM-64) Drop/Insert ports for out-of-band overhead monitoring and provisioing capability.

All major blocks within S10123 can be provisionally bypassed, including the GFP-T and GFP-F mappers, the WIS Frame Generation/Termination blocks, the GFEC/EFEC Encoder/Decoder, and the OTU/ODU Frame Generation/Termination blocks.

The S10124 device provides dedicated serial 10G Client and Line interaces. In addition, the S10124 device also supports a parallel 16-bit SFI4.1 interface that is shared between the Client and Line interfaces. In addition, the S10124 also sports a XAUI/SFI4.2/SFI-5s system/backplane interface. Due to its rich I/O, and built in Client GFEC Termination/Regeneration and Line GFEC/EFEC Termination/Regeneration features, the S10124 device is ideal for transponder and FEC regenerator applications. With the system/backplane interface, the S10124 device offers the utmost in application flexiblity. As with S10123, the S10124 can also be used for 10G Client Line Card and 10G Mapper applications.

Yahara - S10123, S10124, S10126

As with the S10123 device, the S10124 also supports two 10G MACs for full 10GbE traffic monitoring on both the Transmit and Receive datapaths of the device. In addition, the S10124 device also provides OTU-2 and WIS (OC-192/STM-64) Drop/Insert ports for out-of-band overhead monitoring and provisioing capability.

As with the S10123 device, all major blocks within S10124 device can be provisionally bypassed, including the GFP-T and GFP-F mappers, the WIS Frame Generator/Termination blocks, and the GFEC/EFEC Frame Generators/Termination and Encoder/Decoder blocks.

The S10126 device supports a dedicated serial 10G Client inteface and a dedicated serial 10G Line inteface. It is ideal for 10x10G to 100G muxponder applications, as the GMP mapping mode allows for the synchronizing of asynchronous ODU-2s to a common OTU-4 clock, resulting in a dramatically reduced number of external PLLs required. In addition, the S10126 supports all of the other mapping modes of the S10123 and S10124 devices, as well as the two 10G MACs for full 10GbE traffic monitoring, and OTU-2 and WIS Drop/Insert ports for out-of-band overhead monitoring and provisioning capability.

One of the key features of the YAHARA device(s) is its Forward Error Correction capabilities. The YAHARA device(s) support the ITU G.790 (GFEC) standard and AMCC's widely adopted enhanced FEC (eFEC) to enable long haul transmission by compensating for the optical noise in the optical link. Also, YAHARA's XFI serial 10G interfaces have built in Electronic Dispersion Compensation (EDC) that mitigates chromatic dispersion to enable longer transmission distances.

With the S10123 device, G.709 FEC or eFEC can be provisionally appended to the outgoing ODU-2 line signal to produce a jitter compliant OTU-2 serial 10Gb/s output signal. In the reverse direction, the S10123 can receive a 10G OTU-2 signal on the serial 10Gb/s Line receive input, terminate the GFEC/eFEC, perform OTU-2 frame monitoring, and send the ODU-2 signal directly to the System output interface. The 10G MAC, GFP and WIS blocks can be bypassed in both the transmit/receive direction.

With the S10124 and S10126 device, in addition to terminating and generating G.709/eFEC OTU-2 signals on the Line side, the S10124 and S10126 devices can also generate G.709 FEC signals on the outgoing ODU-2 Client signal to produce a jitter compliant OTU-2 serial 10Gb/s output Client signal. In the reverse direction, the S10124/S10126's Client signal can receive a 10G OTU-2 signal on the serial 10Gb/s Line RX receive input, terminate the GFEC, perform OTU-2 frame monitoring, and send the ODU-2 signal directly to the Line Side for GFEC/GFEC or GFEC/eFEC regneration, or to the System output interface. Again, the 10G MAC, GFP and WIS blocks can be bypassed in both the transmit/receive direction.

The S10124 also supports an SFI4.1 interface that can be used on either the Client or Line interface. The SFI4.1 interface is ideal for supporting fully tuneable laser MSA Optic Modules.

Via the S10124/S10126's two serial 10G interfaces and SFI4.1 interface, the S10124/S10126 devices are also ideally suited for ODU-2 to OTU-2 regenerator applications.

Serial 10G Interface(s)

- YAHARA(s) 10G serial line interface(s) supports the following LAN/WAN/OTN Frequencies/Protocols
  - 8G Fibre Channel (8.5Gb/s)
  - 10GbE LAN (10.3Gb/s)
  - 10G Fibre Channel (10.51875 Gb/s)
  - OC-192/STM-64/WAN (9.954 Gb/s)
  - Standard OTU-2 (10.709Gb/s)
  - Overclocked 10GbE to OTU-2 (11.096Gb/s and 11.049Gb/s)
  - Overclocked 10G FC to OTU-2 (11.32Gb/s and 11.27Gb/s)
  - Fully integrated CMU, CDR and SERDES

The lower Line Rates modes are associated with the fixed stuff byte columns being used for user data.

XAUI/SFI4.2/SFI-5s System/Backplane Interface

- YAHARA's System/Backplane Interface is XAUI/SFI4.2/SFI-5s compliant
- In the XAUI mode, it supports 4 x [3.125Gb/s] in 10GbE operation] or 4 x [3.1875 in 10G Fibre Channel operation]
- In the SFI4.2 mode it supports 4 x [2.19Gb/s] to [2.94Gb/s]
- In the SFI-5s mode it supports 5 x [2.125Gb/s] to [2.85Gb/s]
- Fully XAUI and Fibre Channel SxI5 (SFI4.2 & SFI-5S) Jitter Compliant

Clocking

- Flexible clocking configurations for Carrier Ethernet and Transport applications.
- On chip fractional Clock Managment Unit (fracN) from one common reference clock input for all Baud rates for Metro/Carrier Ethernet applications
- For Transport applications the fracN can be used for backup AIS applications and for Receiver CDR reference
- Recovered clock reference outputs for Client/Line Interfaces
- Demapped clock reference outputs for Client/Line Interfaces

"Right Sized" Transport of 10GE-LAN signals through OTN Network

- GFP-F encapsulation used for packing 10GE-LAN signal into "Right Sized" OTU-2 signal resulting in channel rate of 10.7 GHz
- Two different flow-control options used on client to allow for 10GE-LAN signal to be packed into OTU-2
- Proprietary 10GE-LAN mapping into an OTU-2, via GFP-F, without transport rate increase or client flow control
- 10GE-LAN into WIS to allow for SONET/SDH grooming of 10GE client

G.709 ODU-2 Synchronous and Asynchronous Mapping

- 1 x OC192/STM-64 mapping (239,237) per G.709
- Direct map (239,238) into ODU-2

Yahara - S10123, S10124, S10126

G.709 Overhead Processing
- Insert/Drop Port for access to all of ODU-2 overhead
- Dedicated GCC ports

Ingress and Egress Client/Line Data Performance Monitoring
- 1 x OC192C TOH Add/Drop and processing
- 8B/10B PCS monitoring
- 10GbE L1/L2 Monitoring (PCS and MAC)
- SONET/SDH Section/Line Overhead Monitoring per GR-253 and IEEE802.3ae WIS standards

Industry Standard RS(255,239) Forward **E**rror **C**orrection **with 6.2 dB Coding Gain (at 10^{-15} CER)**
- G.709 Compliant Frame Structure

Enhanced Gain Forward Error Correction with G.709 ODU
- 10.71Gbps, 10.66Gbps, 11.1Gbps, and 11.27Gbps rates with enhanced FEC with >8dB coding gain
- G.709 overhead processing and nominal rate expansion
- Comprehensive channel statistics gathering
- Corrected bits, bytes
- Corrected zeros, ones (with outputs)
- Uncorrectable sub-frame count

System/Backplane and Line / Client side loopback
- System/Backplane side, Line side and Client side loopbacks

Support For System Test and Diagnostics
- Can synthesize WIS (SONET/SDH) frame
- Error injection capability for verification of remote error reporting
- Test-set compliant pseudo-random sequence generation/ analysis

General Purpose Processor Interface
- Glueless 16-bit interface to MPC860, 25 MHz to 66 MHz
- Dual mode interface also supports Intel processors
- Interrupt driven or Polled mode operation

Additional Protocol Support
- FEC Frame Synchronous scrambling
- Programmable sequence detection

Optical Module Control
- Two-wire serial interface compliant to the XFP/SFP+ specification
- Dedicated optical module control signals for XFP/SFP+ control

10GE-LAN MAPPING

The YAHARA device(s) support 7 distinct methods to map 10GE-LAN into either OTU-2 or WIS (OC-192/STM-64) signals for transport. Several of the mapping modes are similar to modes implemented in Rubicon and Pemaquid.

The first mode is the Bit Transparency Mode. In this mode, the Line rate operates at 7% above the PCS Encoded Rate. Specifically, the XAUI (Ethernet) data is transparently mapped into an OTU-2 frame and output at either 11.096 or 11.049Gbs, depending if fix stuff bytes are provisioned or not.

The second and third mapping methods are similar and involve GFP-F encapsulation directly into a standard rate 10.7GHz OTU-2 frame. The two methods employ different manners of system/backplane flow control to limit the system/backplane data rate so that correct encapsulation into the OTU-2 frame can take place. The first method of flow control is called "pre-emptive" flow control. In this mode the YAHARA device(s) assert flow control signals back to the system/backplane in regular intervals, thereby guaranteeing that the system/backplane does not overflow the capacity of the OTU-2 frame. The second method allows for the user to place a FIFO-fill line on the ingress system/backplane fifo inside the YAHARA device(s). When the FIFO-fill line is crossed the YAHARA device(s) assert flow control signals back to the system/backplane in order to bleed off the ingress system/backplane FIFO.

The fourth manner of 10E-LAN mapping also involves GFP mapping, and in addition, utilizes some of the OPU overhead bytes to enable full 10GbE preamble transparency and yield a G.709/OTU-2 compliant 10.7Gb/s signal. No back-pressure/flow control mechanism is required to rate limit the system/backplane in this mode of operation.

The fifth manner in which 10GE-LAN mapping is supported is the WIS mode. In this mode, 10GE-LAN traffic is directly encapsulated into a WIS frame and output at a 9.953 Gb/s rate.

Additionaly, in a similar sixth mode, the WIS frame can further be encapsulated into an OTU-2 frame and output at a G.709 compliant 10.7Gb/s signal.

Finally the YAHARA device(s) also supports a pure LAN SERDES mode, where the 10GbE LAN signal is passed through the YAHARA device(s) and output on the Line interface at a 10.3Gb/s rate.

10G FIBRE CHANNEL MAPPING

The YAHARA device(s) support a 10G Fibre Channel (FC) to OTU-2 mapping mode, where the 10G FC traffic entering the YAHARA device(s) via the SFI4.2 interface is mapped directly into an OTU-2 signal before being presented over the Line interface at a 11.32/11.27 Gb/s rate, pending the use/non-use of stuff byte columns. In the reverse direction an OTU-2 signal carrying a 10G FC signal can be OTU- 2 terminated and then directly presented over the SFI4.2 system interface.

The YAHARA device(s) also support a PCS PHY mode. In this mode the 10G FC traffic entering/exiting the XAUI interface can be 64B/66B encoded/decoded and then mapped/demapped into an OTU-2 signal before being transmitted/received off of the 10G Line interface.

The YAHARA device(s) also supports a SERDES pass-thru mode, where the 10G Fibre Channel LAN signal is passed through the YAHARA device(s) and output on the Line interface at a 10.51Gb/s rate.

8G FIBRE CHANNEL MAPPING

The YAHARA device(s) support a 8G Fibre Channel (FC) to OTU-2 mapping mode, where the 8G FC traffic entering the YAHARA device(s) via the SFI4.2 interface is mapped into a GFP-T signal, before then being mapped into an OTU-2 signal. In the reverse direction an OTU-2 signal carrying an 8G FC signal can be OTU-2 terminated and then demapped from the GFP-T frame before being presented over the SFI4.2 system interface.

The YAHARA device(s) also supports a SERDES pass-thru mode, where the 8G Fibre Channel LAN signal is passed through the YAHARA device(s) and output on the Line interface at a 8.5Gb/s rate.

OC-192/STM MAPPING

The YAHARA device(s) support a mode where OC-192/STM64 (10GBase-W) traffic entering via the Client XFI/SFI or SFI4.2 interfaces can be directly mapped into an OTU-2 signal before being output over the Line Interface at either a serial 9.954Gb/s rate or a parallel 16x622Mb/s rate.

The YAHARA device(s) also supports a pure SONET SERDES pass thru-mode, where the OC-192/STM-64 signal is passed through the YAHARA device(s) and output at either a serial 9.954Gb/s rate or a paralell 16x622Mb/s rate, with jitter compliance.

AIS SUPPORT

For applications in which the LINE signal is operating in the SONET/SDH (WIS) mode, the YAHARA device(s) can generate a SONET/SDH AIS on the Line egress.

For applications in which the Line signal is G.709 compliant or for OTN applications, Line Fail and un-equipped OTN AIS is supported. For OTN edge applications, the device can be provisioned to provide either a SONET/SDH AIS or a OTN Generic AIS to the Line Interface. This facilitates convergence of the SONET/SDH (WIS) and OTN functions into a single network element.

ODU MAPPING

ITU compliant system/backplane mapping of 10GbE and 10G/8G Fibre Channel signals into ODU-2 signals, via GFP and WIS frames, is supported whereby a stuff column is added to every G.709 sub-frame resulting in an ODU rate expansion of (239/237). The chip can be configured to insert the G.709 compliant stuff-byte value or to insert user data into this column. The values assigned to the stuff bytes can be defined from a register set on chip. Coverage of these stuff columns in the BIP calculation or in the FEC is optional and can be enabled via software. When the no-coverage option is enabled, the BIP and parity check values are calculated as if the standard stuff values were present.

A direct map mode is supported for ODU-2 with no stuff columns to enable mapping with a 239/238 rate expansion. Start-of-frame signals are provided at the input and output ports to enable synchronization to the ODU.

LOOPBACK FUNCTIONS

Near-end and far-end loopbacks are supported for the System/Backplane interface and for the line/client interfaces. This enables client/line and device testing and fault isolation. Each functional block may be bypassed as required to support the application.

Yahara - S10123, S10124, S10126

Figure 2. S10123 in a 10G Line Card Application

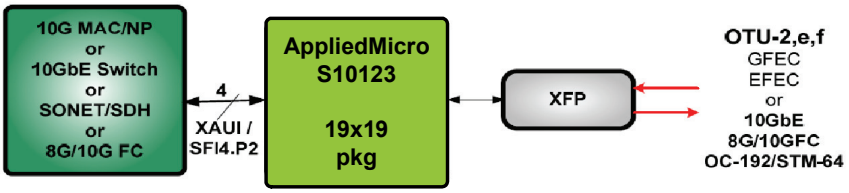
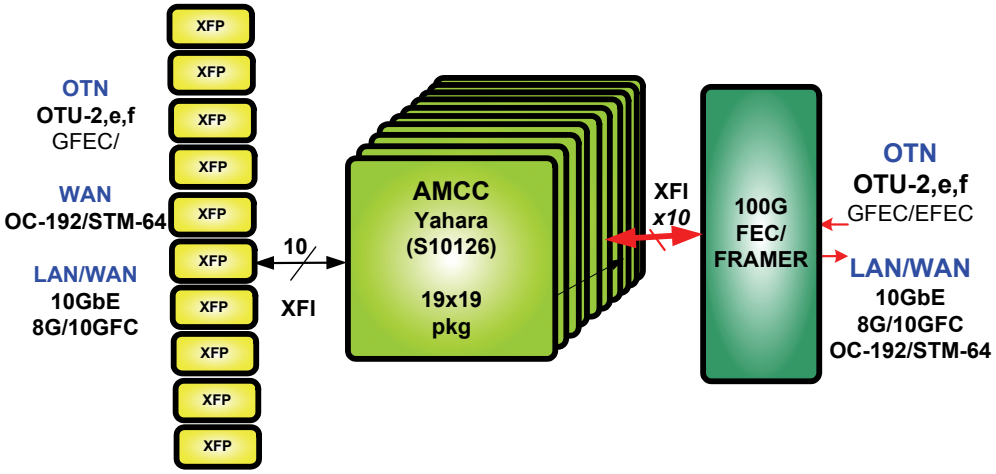


Figure 3. S10126 in a 10x10G to 100G Muxponder Card Application



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