CY62148E MoBL®

4-Mbit (512 K × 8) Static RAM

Features

- Very high speed: 45 ns
- Voltage range: 4.5 V to 5.5 V
- Pin compatible with CY62148B
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 2.0 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP) II and 32-pin small-outline integrated circuit (SOIC)[1] packages

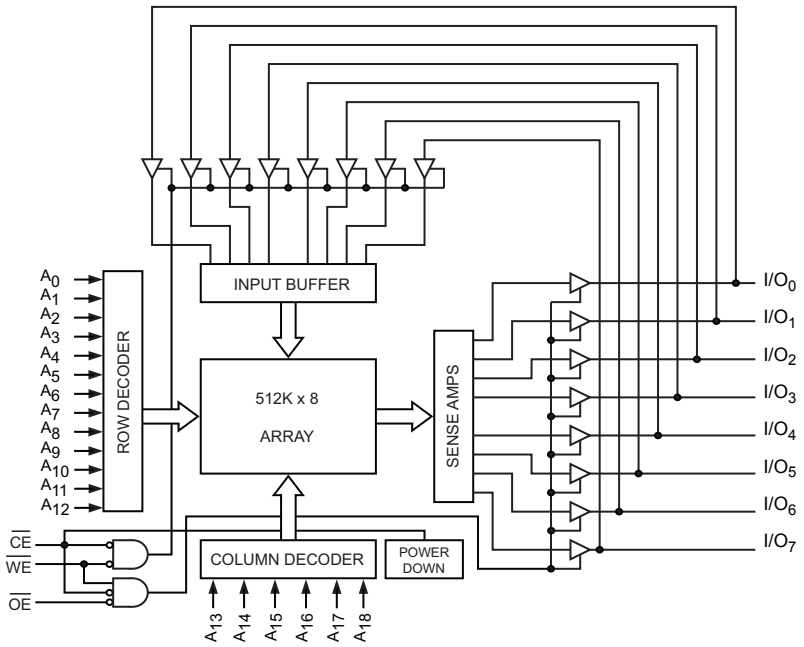
Functional Description

The CY62148E is a high performance CMOS static RAM organized as 512 K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), Outputs are disabled ($\overline{OE}$ HIGH), or during an active Write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW)

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

Logic Block Diagram



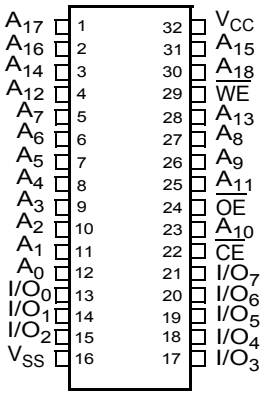
Note
1. SOIC package is available only in 55 ns speed bin.

Contents

Pin Configuration

Figure 1. 32-pin SOIC/TSOP II Pinout

Top View



Product Portfolio

Product		Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
							Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
							f = 1 MHz		f = f_{max}			
			Min	Typ[2]	Max		Typ[2]	Max	Typ[2]	Max	Typ[2]	Max
CY62148ELL	TSOP II	Industrial	4.5	5.0	5.5	45	2	2.5	15	20	1	7
CY62148ELL	SOIC	Industrial / Automotive-A	4.5	5.0	5.5	55	2	2.5	15	20	1	7

Note
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

DC voltage applied to outputs in high Z state [3, 4]..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

DC input voltage [3, 4]..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current.....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62148E	Industrial / Automotive-A	–40 °C to +85 °C	4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		45 ns			55 ns [6]			Unit
				Min	Typ[7]	Max	Min	Typ[7]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –1 mA		2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 2.1 mA		–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 4.5 V to 5.5 V		2.2	–	V_{CC} + 0.5	2.2	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage	V_{CC} = 4.5 V to 5.5 V	For TSOPII package	–0.5	–	0.8	–	–	–	V
			For SOIC package	–	–	–	–0.5	–	0.6[8]	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	15	20	–	15	20	mA
		f = 1 MHz		–	2	2.5	–	2	2.5	
I_{SB2} [9]	Automatic CE power-down current — CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	1	7	–	1	7	µA

Capacitance

Parameter[10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(Typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

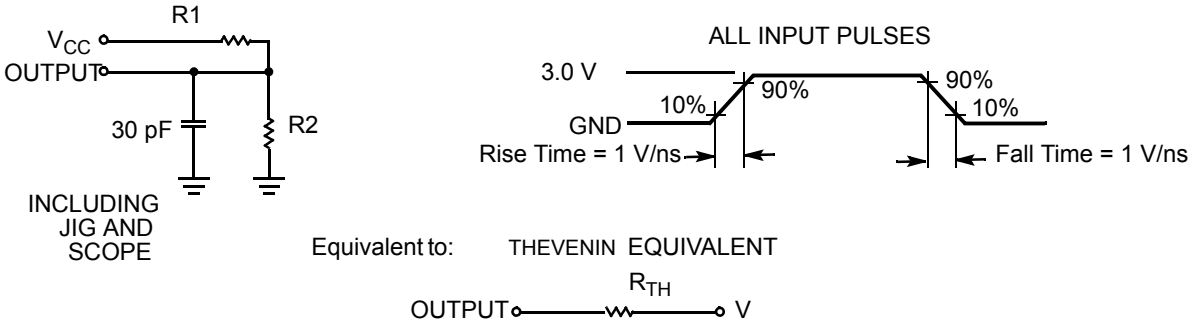
Notes

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns for I ≤ 30 mA.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
6. SOIC package is available only in 55 ns speed bin.
7. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
8. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.6 V. This is applicable to SOIC package only. Refer to AN13470 for details.
9. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter [11]	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C/W
Θ_{JC}	Thermal resistance (junction to case)		10	13	°C/W

Figure 2. AC Test Loads and Waveforms



Parameter [11]	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

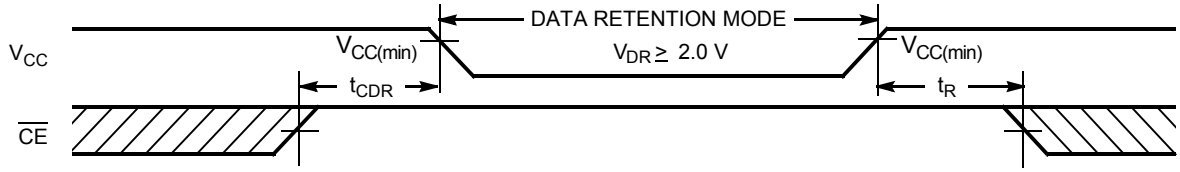
Note
11. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions		Min	Typ[12]	Max	Unit
V_{DR}	V_{CC} for data retention			2	–	–	V
I_{CCDR}[13]	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial / Automotive-A	–	1	7	µA
t_{CDR}	Chip deselect to data retention time			0	–	–	ns
t_R[14]	Operation recovery time		TSOP II	45	–	–	ns
			SOIC	55	–	–	ns

Figure 3. Data Retention Waveform



Notes
12. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
13. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) > 100 µs or stable at V_{CC}(min) > 100 µs.

Switching Characteristics

Over the operating range

Parameter [15]	Description	45 ns		55 ns[16]		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [17]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [17, 18]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [17]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [17, 18]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
Write Cycle[19]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [17, 18]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [17]	10	–	10	–	ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the AC Test Loads and Waveforms on page 5.
16. SOIC package is available only in 55 ns speed bin.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. The internal wre.ite time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

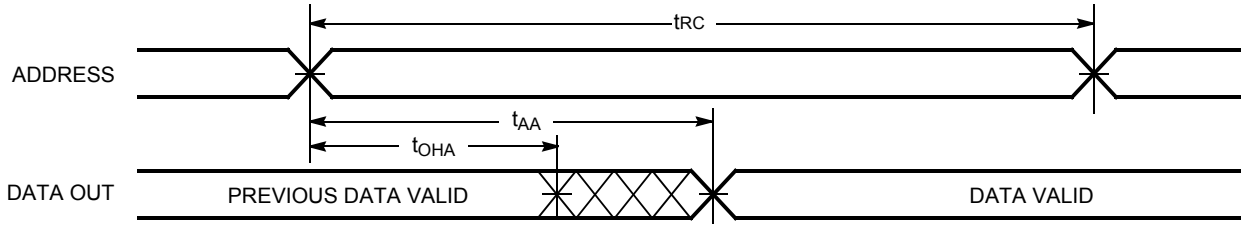


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]

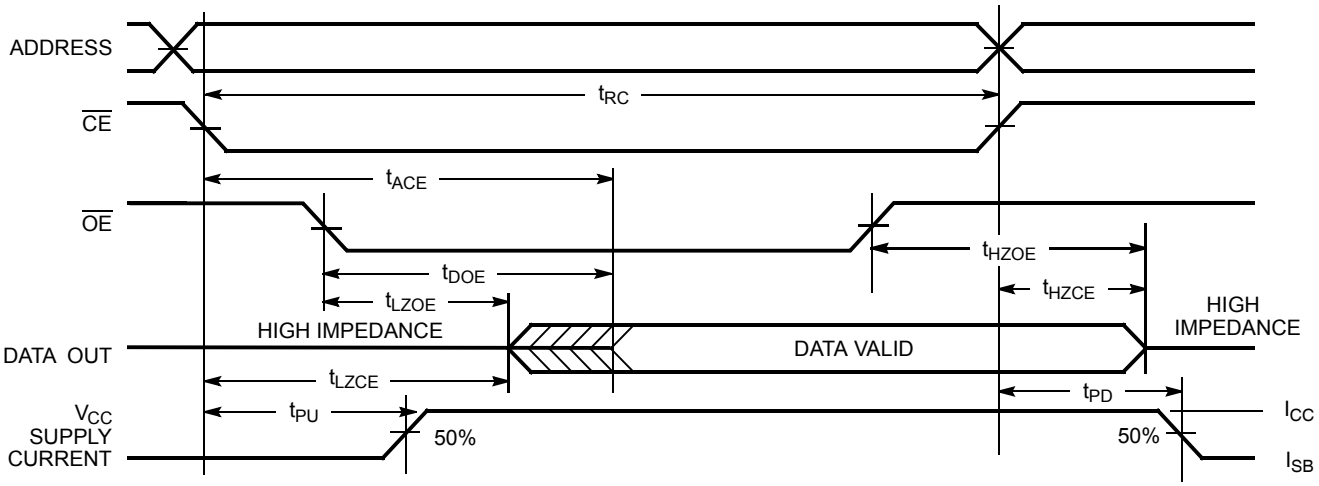
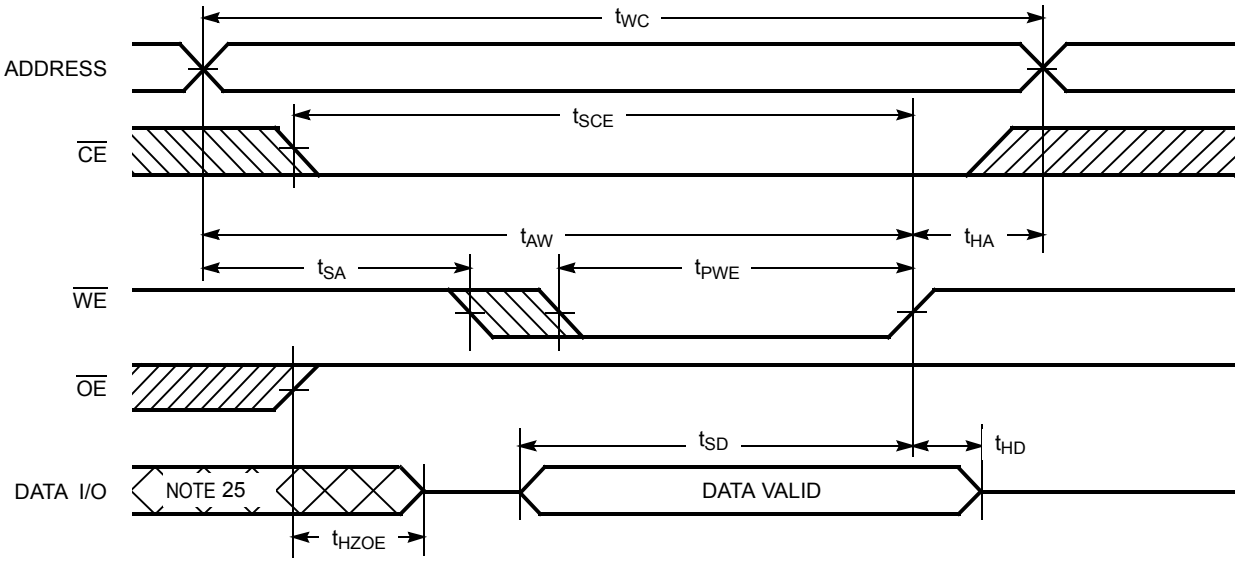


Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [23, 24]



Notes
20. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycles.
22. Address valid before or similar to $\overline{CE}$ transition LOW.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state and input signals must not be applied.

Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [26, 27]

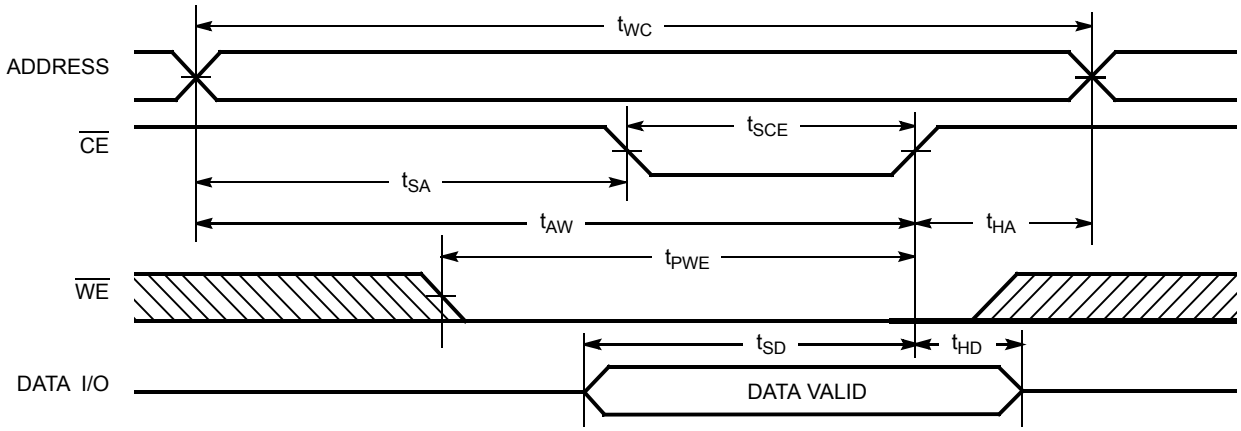
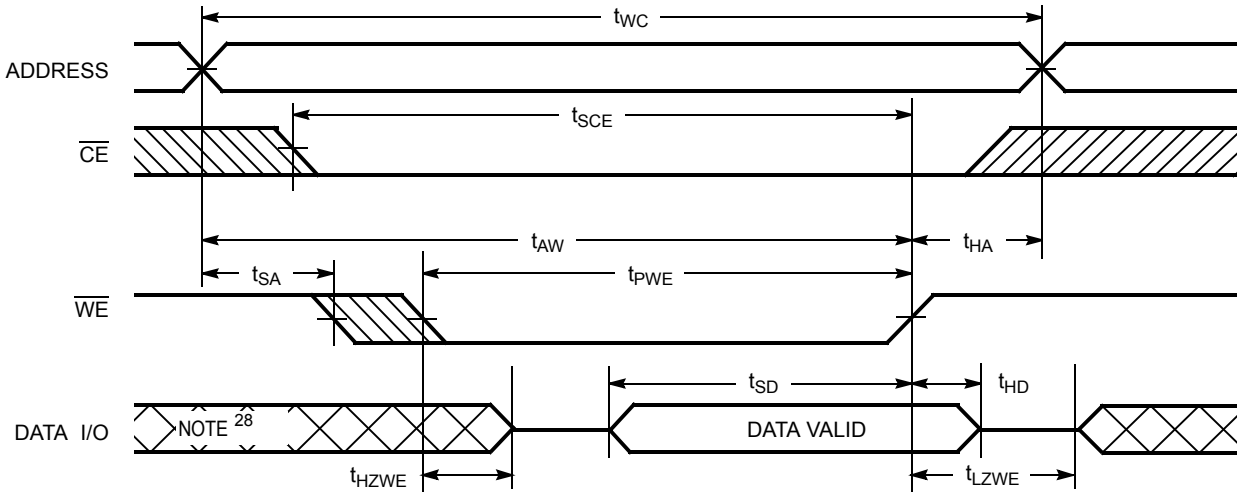


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [27]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H[29]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Notes
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
28. During this period, the I/Os are in output state and input signals must not be applied.
29. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Ordering Information

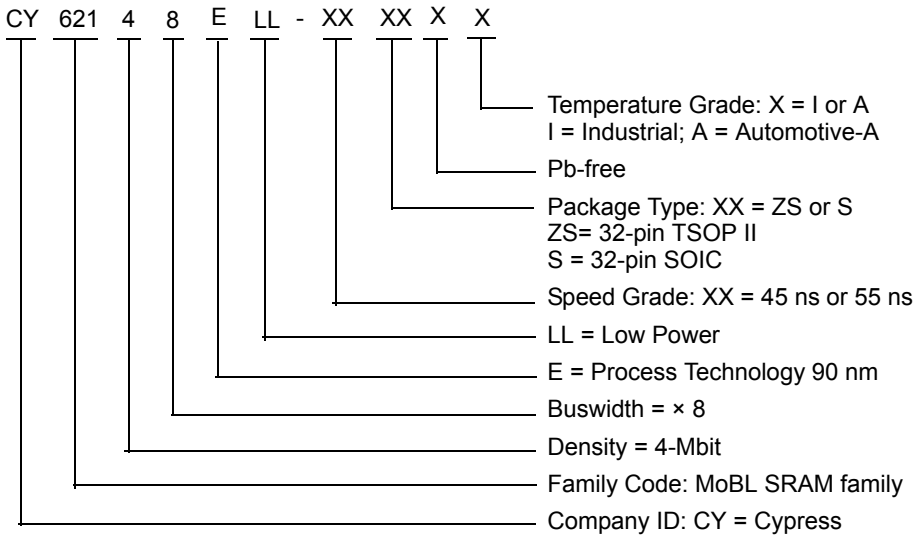
Table 1 lists the CY62148E MoBL® key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key features and Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148ELL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
	CY62148ELL-45ZSXA	51-85095	32-pin TSOP II (Pb-free)	Automotive-A
55	CY62148ELL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial
	CY62148ELL-55SXA	51-85081	32-pin SOIC (Pb-free)	Automotive-A

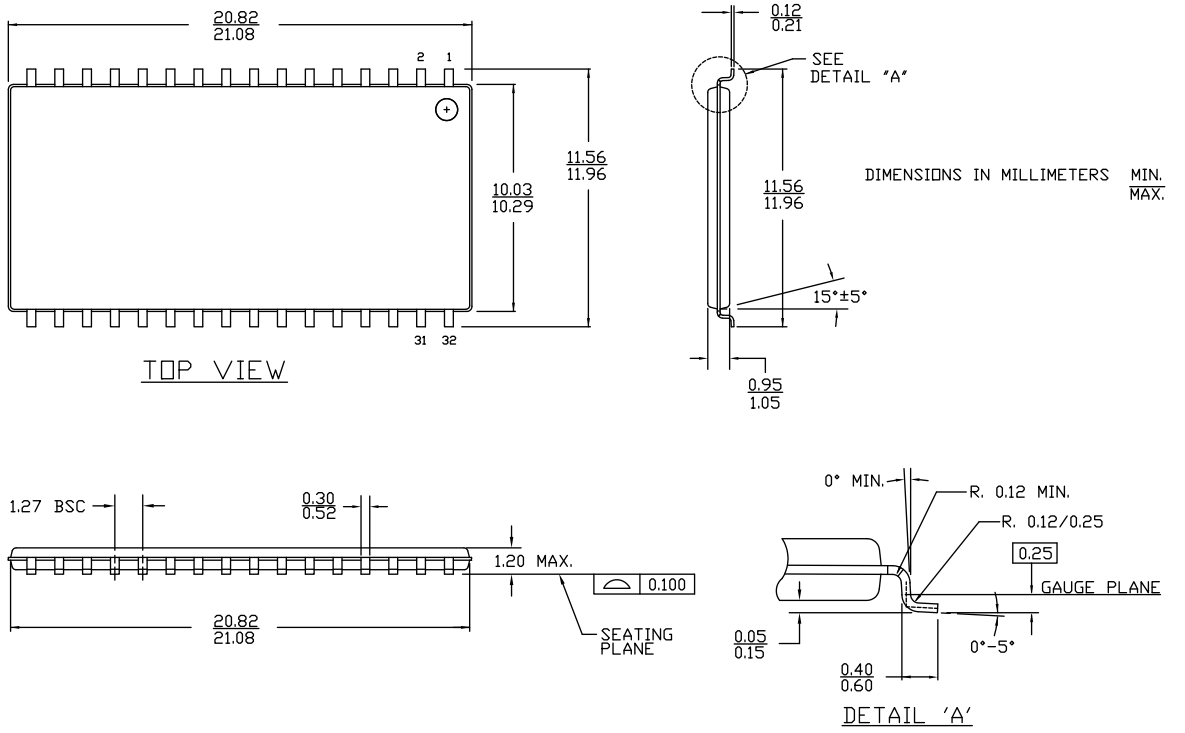
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



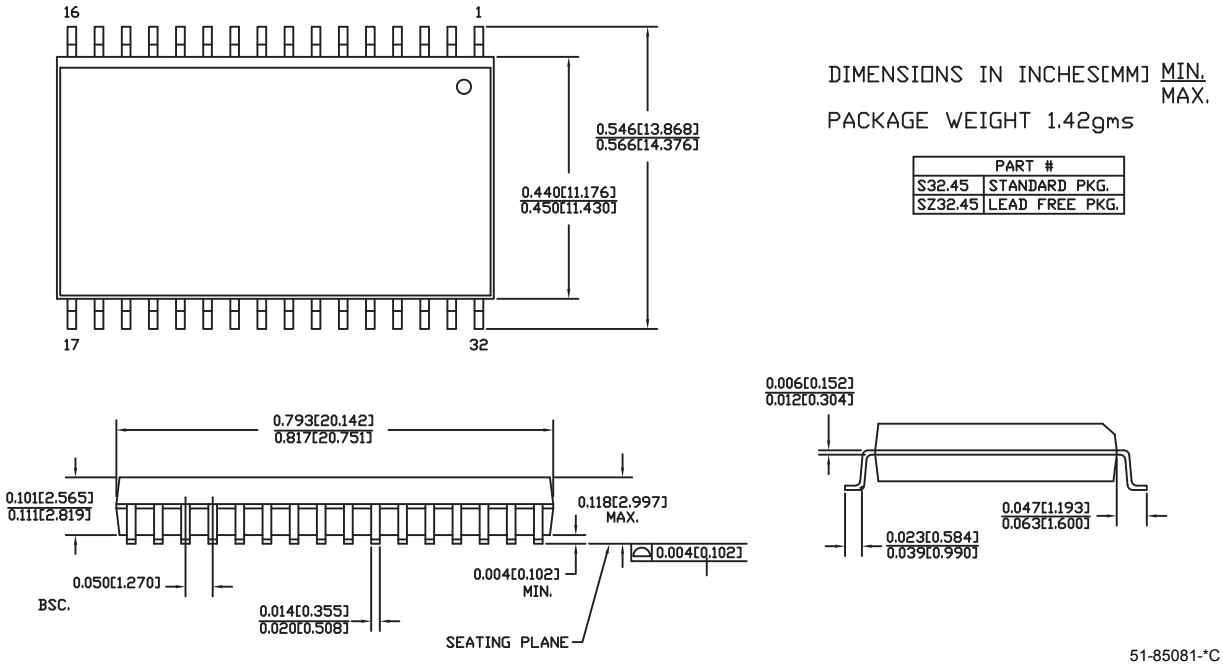
Package Diagrams

Figure 9. 32-pin TSOP II, 51-85095



51-85095 *B

Figure 10. 32-pin (450-Mil) Molded SOIC, 51-85081



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
MoBL	more battery life
SOIC	small-outline integrated circuit
SRAM	static random access memory
TSOP	thin small outline package
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
MHz	Mega Hertz
µA	micro Amperes
mA	milli Amperes
pF	pico Farads
Ω	ohms
°C	degree Celsius
W	Watts
%	percent

Document History Page

Document Title: CY62148E MoBL®, 4-Mbit (512 K × 8) Static RAM Document Number: 38-05442				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	201580	AJU	01/08/04	New datasheet
*A	249276	SYT	See ECN	Changed from Advance Information to Preliminary Moved Product Portfolio to Page 2 Added RTSOP II and Removed FBGA Package Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed I_{CCDR} from 2.0 μA to 2.5 μA Changed typo in Data Retention Characteristics(t_R) from 100 μs to t_{RC} ns Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed t_{HZOE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed t_{SCE} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed t_{HZCE} from 12 to18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Corrected typo in Package Name Changed Ordering Information to include Pb-free Packages
*B	414820	ZSD	See ECN	Changed from Preliminary to Final Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Removed 35ns Speed Bin Removed “L” version of CY62148E Changed I_{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I_{CC} (Max) value from 2 mA to 2.5 mA at f=1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f=f_{max} Removed I_{SB1} spec from the Electrical characteristics table Changed I_{SB2} Typ values from 0.7 μA to 1 μA and Max values from 2.5 μA to 7 μA Modified footnote #4 to include current limit Removed redundant footnote on DNU pins Changed the AC testload capacitance from 100 pF to 30 pF on page #4 Changed test load parameters R1, R2, R_{TH} and V_{TH} from 1838 Ω, 994 Ω, 645 Ω and 1.75 V to 1800 Ω, 990 Ω, 639 Ω and 1.77 V Changed I_{CCDR} from 2.5 μA to 7 μA Added I_{CCDR} typical value Changed t_{LZOE} from 3 ns to 5 ns Changed t_{LZCE} and t_{LZWE} from 6 ns to 10 ns Changed t_{HZCE} from 22 ns to 18 ns Changed t_{PWE} from 30 ns to 35 ns Changed t_{SD} from 22 ns to 25 ns Updated the ordering information table and replaced Package Name column with Package Diagram
*C	464503	NXR	See ECN	Included Automotive Range in product offering Updated the Ordering Information
*D	485639	VKN	See ECN	Corrected the operating range to 4.5 V - 5.5 V on page# 3
*E	833080	VKN	See ECN	Added footnote #8 Added V_{IL}spec for SOIC package.

Document History Page (continued)

Document Title: CY62148E MoBL®, 4-Mbit (512 K × 8) Static RAM Document Number: 38-05442				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	890962	VKN	See ECN	Added Automotive-A part and its related information Removed Automotive-E part and its related information Added footnote #2 related to SOIC package Added footnote #9 related to I_{SB2} Added AC values for 55 ns Industrial-SOIC range Updated Ordering Information table
*G	2947039	VKN	06/10/2010	Added “CY62148ELL-45ZSXA” part in Ordering information. Added footnote related to chip enable in Truth Table Updated Package Diagrams Added Contents, PSoC Solutions, and Sales, Solutions, and Legal Information.
*H	3006318	AJU	08/23/10	Template update. Updated table of contents. Added acronyms, units of measure and ordering code definitions. Added reference to note 12 to parameter I_{CCDR} on page 5.
*I	3235744	RAME	04/20/2011	Updated Functional Description (Removed the line “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines”). Updated Package Diagrams.

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