PRELIMINARY DATA SHEET

General Description

Using the IDT CMOS oscillator technology, originally developed by Mobius Microsytems, the 3C02 replaces quartz crystal based resonators and oscillators with a monolithic CMOS IC at the thinnest possible form factors without the use of any mechanical frequency source or PLL. The product is specially designed to work with the next generation USB 3.0 Super Speed, PCIe® Gen1/2 and S-ATA interface controller ICs and systems.

Features

- All-CMOS Temperature Compensated Oscillator
- Excellent Frequency Accuracy: +/- 100ppm total
- Ultra-low power operation (2mA typical at 1.8V supply)
- No quartz or PLL used: very low jitter performance leading to low link Bit Error Rates (BER)
- Excellent reliability: Shock and vibration resistant
- Many frequencies are supported
- Factory programmable from 6 to 133MHz

Ordering Information

3C	P	0	C	02	-	FFF	NSG	X	8
1	2	3	4	5		6	7	8	9

1) IDT Base Part Number for 100ppm CMOS Oscillator

2) Supply Voltage Configuration

- P: 1.8V to 3.3V continuous operation

3) Output Signal Type

- 0: LVCMOS Output

4) “C” indicates integrated CMOS Oscillator

5) “XX” is product specific code that indicated product sequence

6) FFF: Factory Programmed Frequency in MHz

7) Package Options*

- NSG: 5x3.2, 4-Pin Package
- NVG: 2.5x2.0, 4-Pin Package[2]
- M: SOIC, 8-pin Package[2]

8) Temperature Grade

- “E” -20 to 70°C Extended Commercial Temperature Range
- “ “ 0 to 70oC Commercial Temperature Range,ie. default is blank[2]
- “R” -20 to 85oC Restricted Industrial Temperature Range[2]

9) Tape & Reel Option

- “ “: Shipped in Tube i.e. default is blank
- 8: Shipped in Tape & Reel

[1] :This product is rated “Green”, please contact factory for environmental compliancy information

[2] : Future product. Not available for design-in. Please contact your IDT representative for details

Pin Assignment

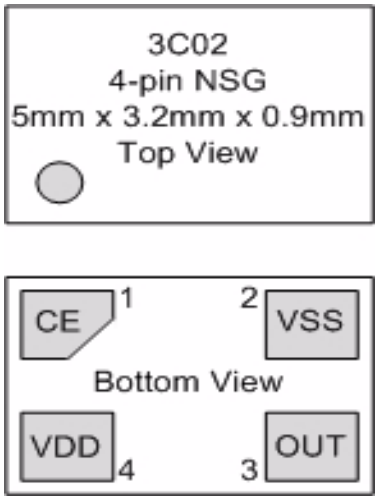


Table 1. Pin Descriptions

No	Name	Type	Description
1	CE	Input Pullup	Chip Enable. Internal Pullup. 3C02 is enabled when HIGH. When LOW, OUT has a weak pull-down to GND internally
2	VSS	Power	System Ground
3	OUT	Output	Frequency Output
4	VDD	Power	Power Supply. Use a 0.1µF decoupling capacitor between VDD and VSS

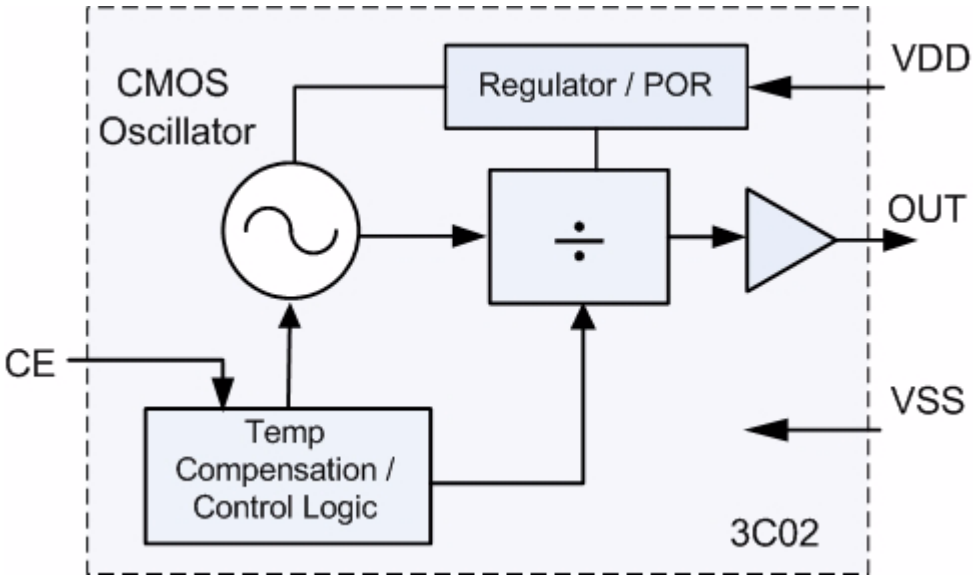
The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice

Table 2. Pin Descriptions

Below Pin Descriptions apply to SOIC-8 Package

No	Name	Type	Description
1	CE	Input Pullup	Chip Enable. Internal Pullup. 3C02 is enabled when HIGH.When LOW, OUT has a weak pull-down to GND internally
4	VSS	Power	System Ground
6	OUT	Output	Frequency Output
8	VDD	Power	Power Supply. Use a 0.1µF decoupling capacitor between VDD and VSS
2,3,5,7	NC		No Connect Pins. These pins may be left floating.

Block Diagram



Functional Description

3C02 is a monolithic all-CMOS frequency source. The internal CMOS Oscillator generates the factory-programmed frequencies with high accuracy and excellent phase noise and jitter. The device is a silicon alternative to quartz based crystal resonators and oscillators. Various programming and configuration options are supported as given in the Part Ordering Information section above. The easy-to-use device offers programmable frequencies and various supply voltage configurations. Offered in common crystal oscillator pin-outs, the 3C02 allows the designer to disable the oscillator via the CE pin to enter a very low current, quiescent state. The CMOS oscillator features very fast start-up time to enable rapid wake-up from the quiescent state. All required circuit elements other than those that are noted in the Pin Descriptions Table (Table.1) above are internal to the device.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, VDD	4.6V
Input, V_I (CE pin)	-0.5V to VDD + 0.5V
Output, V_O (OUT pin)	-0.5V to VDD + 0.5V
Storage Temperature	-65°C to 150°C

Electrical Characteristics[5] [3.3V]

VDD=3.0V to 3.6V, T_A=-20 to 70°C unless otherwise noted. Typical values are measured at VDD=3.3V, T_A=35°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ElectroStaticDischarge	ESD	Human Body Model, tested per JESD D22-A114	4000			V
Supply Voltage	VDD	Normal Operation[3]	3.0	3.3	3.6	V
Input LOW level	V_{IL}	CE pin	-0.3		VDD*0.3	V
Input HIGH level	V_{IH}	CE pin	VDD*0.7		VDD+0.3	V
Supply Current	IDD	Active supply current, VDD=3.3V, T=35oC, no output load		2.5	3.0	mA
Quiescent Current	IDDQ	CE=LOW, output disabled		0.2	1	µA
Output LOW level	V_{OL}	I_{OL} = -4mA			0.5	V
Output HIGH level	V_{OH}	I_{OH} = 4mA	VDD-0.5			V
Output Frequency	F_{OUT}	Factory Programmable.Contact IDT for frequencies not listed		12,48,75,125		MHz
Frequency Stability	F_{TOT}	Total Frequency Stability over temperature,supply variation,aging (1st year at 35oC),shock&vibration. “E” device option, over -20 to 70°C range			±100	ppm
Rise Time	RT	20% to 80% x VDD. Output load (C_L) =8pF, NSG-option			1.9	ns
Fall Time	FT	80% to 20% x VDD. Output load (C_L) =8pF, NSG-option			1.9	ns
Duty Cycle	DC	Clock output duty cycle. Measured under 80MHz, VDD/2, C_L=8pF	45		55	%
		Clock output duty cycle. Measured over 80MHz, VDD/2, C_L=8pF	40		60	%
Power-up time	t_{on}	Output valid time after VDD meets the specified range&CE transition	50	100	400	µs
Period Jitter	PJ_{RMS}	Total RMS Period Jitter (including random and deterministic)[1,2]		3.5		ps_{RMS}
Cycle-cycle Jitter	CJ	The absolute value of max change in the periods of any 2 adjacent cycles[1,2,4]			50	ps
Phase Noise	PN	1MHz offset from carrier[1,2]		-140	-135	dBc/Hz

Notes 1. Measured with a 50Ω to GND termination

2: Measured at 48MHz output frequency

3. The 3C02 will support continuous VDD operation from 1.62 to 3.6V. The device can be powered up with a supply voltage at any of the 3 main supply rails of 1.8V, 2.5V or 3.3V.

4. Measured over 1000 cycles per JEDEC standard 65

5. Electrical parameters are guaranteed by design and characterization over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Electrical Characteristics[5] [2.5V]

VDD=2.25V to 2.75V, T_A=-20 to 70°C unless otherwise noted. Typical values are measured at VDD=2.5V, T_A=35°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ElectroStaticDischarge	ESD	Human Body Model, tested per JESD D22-A114	4000			V
Supply Voltage	VDD	Normal Operation[3]	2.25	2.5	2.75	V
Input LOW level	V_{IL}	CE pin	-0.3		VDD*0.3	V
Input HIGH level	V_{IH}	CE pin	VDD*0.7		VDD+0.3	V
Supply Current	IDD	Active supply current, VDD=2.5V, T=35oC, no output load		2.25	2.75	mA
Quiescent Current	IDDQ	CE=LOW, output disabled		0.2	1	µA
Output LOW level	V_{OL}	I_{OL} = -3mA			0.4	V
Output HIGH level	V_{OH}	I_{OH} = 3mA	VDD-0.4			V
Output Frequency	F_{OUT}	Factory Programmable.Contact IDT for frequencies not listed		12,48,75,125		MHz
Frequency Stability	F_{TOT}	Total Frequency Stability over temperature,supply variation,aging (1st year at 35oC),shock&vibration. “E” device option, over -20 to 70°C range			±100	ppm
Rise Time	RT	20% to 80% x VDD. Output load (C_L) =7pF, NSG-option			2.3	ns
Fall Time	FT	80% to 20% x VDD. Output load (C_L) =7pF, NSG-option			2.3	ns
Duty Cycle	DC	Clock output duty cycle. Measured under 100MHz at VDD/2, C_L=7pF	45		55	%
		Clock output duty cycle. Measured over 100MHz at VDD/2, C_L=7pF	40		60	%
Power-up time	t_{on}	Output valid time after VDD meets the specified range&CE transition	50	100	400	µs
Period Jitter	PJ_{RMS}	Total RMS Period Jitter (including random and deterministic)[1,2]		3.5		ps_{RMS}
Cycle-cycle Jitter	CJ	The absolute value of max change in the periods of any 2 adjacent cycles[1,2,4]			50	ps
Phase Noise	PN	1MHz offset from carrier[1,2]		-140	-135	dBc/Hz

Notes 1. Measured with a 50Ω to GND termination

2: Measured at 48MHz output frequency

3. The 3C02 will support continuous VDD operation from 1.62 to 3.6V. The device can be powered up with a supply voltage at any of the 3 main supply rails of 1.8V, 2.5V or 3.3V.

4. Measured over 1000 cycles per JEDEC standard 65

5. Electrical parameters are guaranteed by design and characterization over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Electrical Characteristics[5] [1.8V]

VDD=1.62V to 1.98V, T_A=-20 to 70°C unless otherwise noted. Typical values are measured at VDD=1.8V, T_A=35°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ElectroStaticDischarge	ESD	Human Body Model, tested per JESD D22-A114	4000			V
Supply Voltage	VDD	Normal Operation[3]	1.62	1.8	1.98	V
Input LOW level	V_{IL}	CE pin	-0.3		VDD*0.3	V
Input HIGH level	V_{IH}	CE pin	VDD*0.7		VDD+0.3	V
Supply Current	IDD	Active supply current, VDD=1.8V, T=35oC, no output load		2.0	2.5	mA
Quiescent Current	IDDQ	CE=LOW, output disabled		0.2	1	µA
Output LOW level	V_{OL}	I_{OL} = -1.8mA			0.3	V
Output HIGH level	V_{OH}	I_{OH} = 1.8mA	VDD-0.3			V
Output Frequency	F_{OUT}	Factory Programmable.Contact IDT for frequencies not listed		12,48,75,125		MHz
Frequency Stability	F_{TOT}	Total Frequency Stability over temperature,supply variation,aging (1st year at 35oC),shock&vibration. “E” device option, over -20 to 70°C range			±100	ppm
Rise Time	RT	20% to 80% x VDD. Output load (C_L) =4pF, NSG-option			2.75	ns
Fall Time	FT	80% to 20% x VDD. Output load (C_L) =4pF, NSG-option			2.75	ns
Duty Cycle	DC	Clock output duty cycle. Measured at VDD/2, C_L=4pF	45		55	%
Power-up time	t_{on}	Output valid time after VDD meets the specified range&CE transition	50	100	400	µs
Period Jitter	PJ_{RMS}	Total RMS Period Jitter (including random and deterministic)[1,2]		3.5		ps_{RMS}
Cycle-cycle Jitter	CJ	The absolute value of max change in the periods of any 2 adjacent cycles[1,2,4]			50	ps
Phase Noise	PN	1MHz offset from carrier[1,2]		-140	-135	dBc/Hz

Notes 1. Measured with a 50Ω to GND termination

2: Measured at 48MHz output frequency

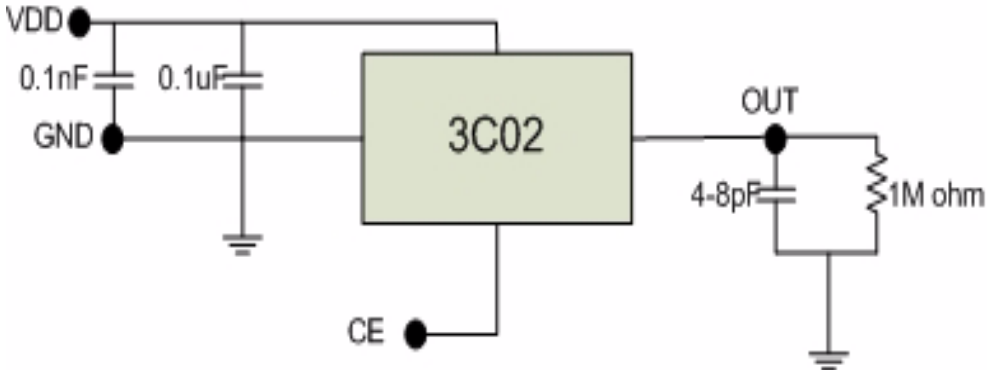
3. The 3C02 will support continuous VDD operation from 1.62 to 3.6V. The device can be powered up with a supply voltage at any of the 3 main supply rails of 1.8V, 2.5V or 3.3V.

4. Measured over 1000 cycles per JEDEC standard 65

5. Electrical parameters are guaranteed by design and characterization over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

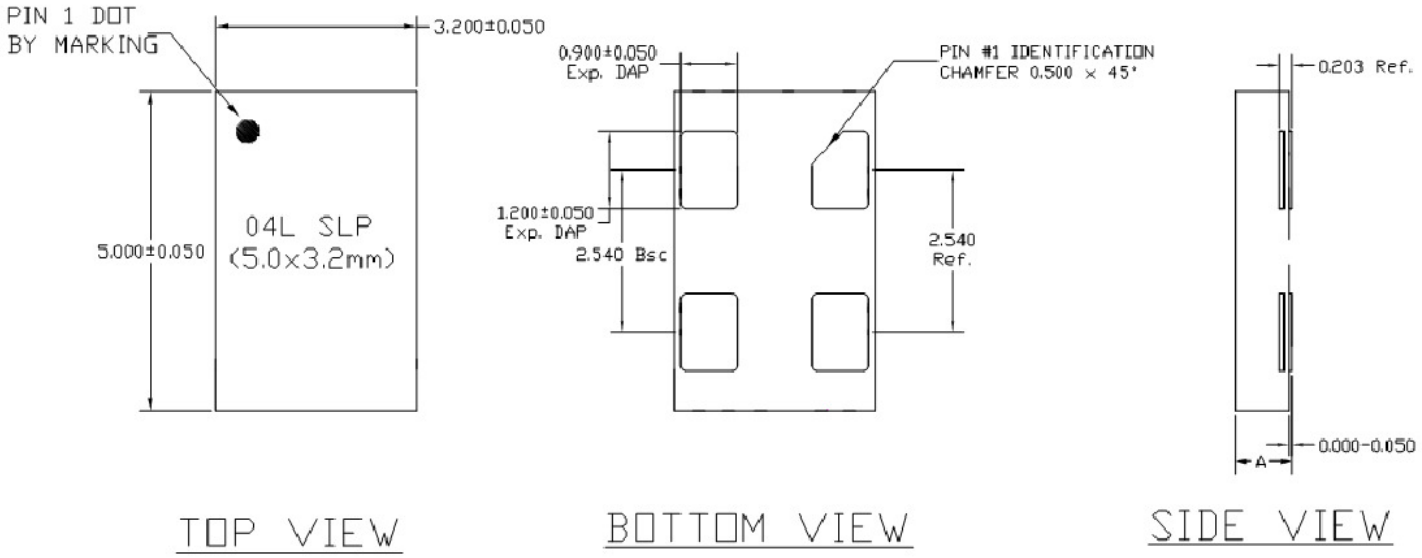
Application Diagram

Below is a representative application diagram to evaluate the 3C02. For 50Ohm terminated measurements, a balun is necessary to provide proper impedance matching



Package Outline and Package Dimensions

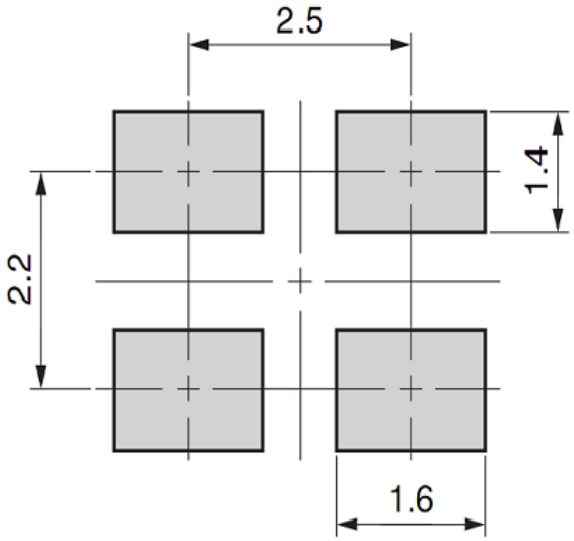
Package Outline for NSG -5.0x3.2x0.9mm, 4-pin package:



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS

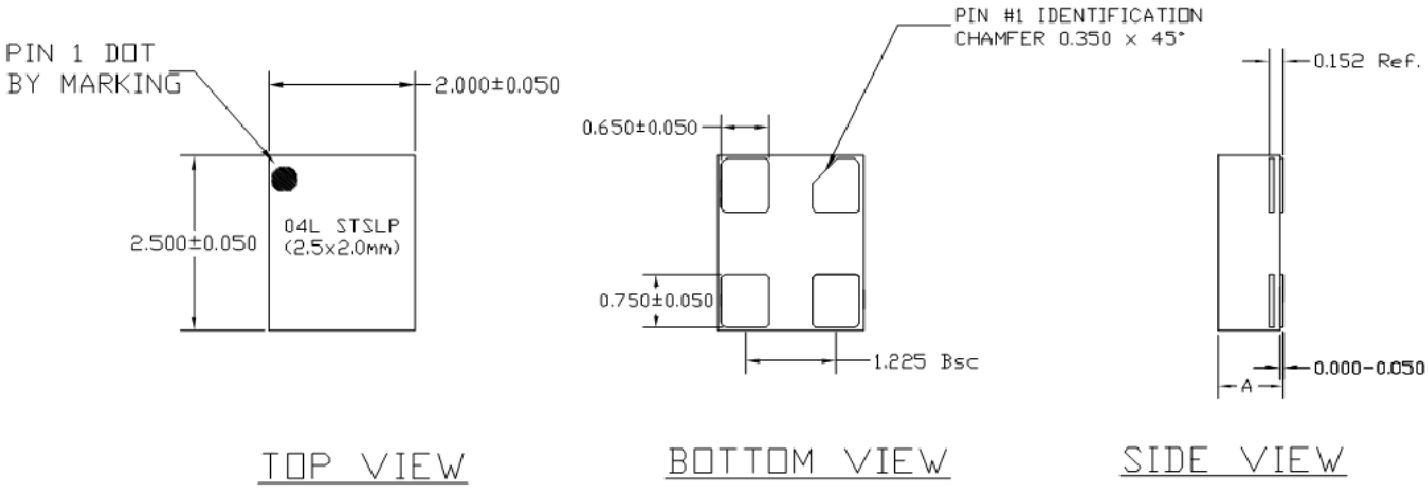
		SLP
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800

Below is the recommended PCB land pattern for the 3C02 NSG package:



Package Outline and Package Dimensions

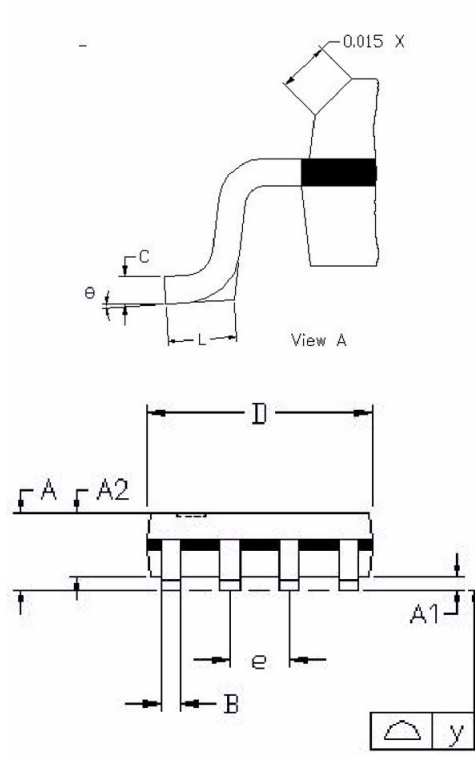
Package Outline for NVG -2.5x2.0x0.55mm, 4-pin package:



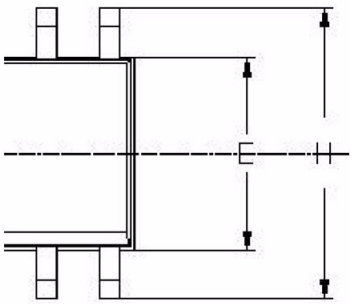
NOTE:

		STSLP
A	MAX.	0.600
	NOM.	0.550
	MIN.	0.500

Package Outline for SOIC, 8-pin package:



DIMS.	MILLIMETERS		
	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	----	0.25
A2	----	1.45	----
B	0.33	----	0.51
C	0.19	----	0.25
D	4.80	----	5.00
E	3.80	----	4.00
e	----	1.27	----
H	5.80	----	6.20
L	0.40	----	1.27
y	----	----	0.10
θ	0 Degree	----	8 degrees



NOTES:
1. ALL DIMENSIONS IN MILLIMETER. (see Table for mils equivalent)
2. PACKAGE SURFACE FINISH: MATTE, CHARMILLES #24~27.
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURRS.
4. DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
5. TOLERANCE : +/- 0.1mm UNLESS OTHERWISE SPECIFIED.
6. OTHER DIMENSIONS FOLLOW ACCEPTABLE SPEC.

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