High-Voltage Switchmode Controllers

DESCRIPTION

The Si9110/9111 are BiC/DMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10 to 120 VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

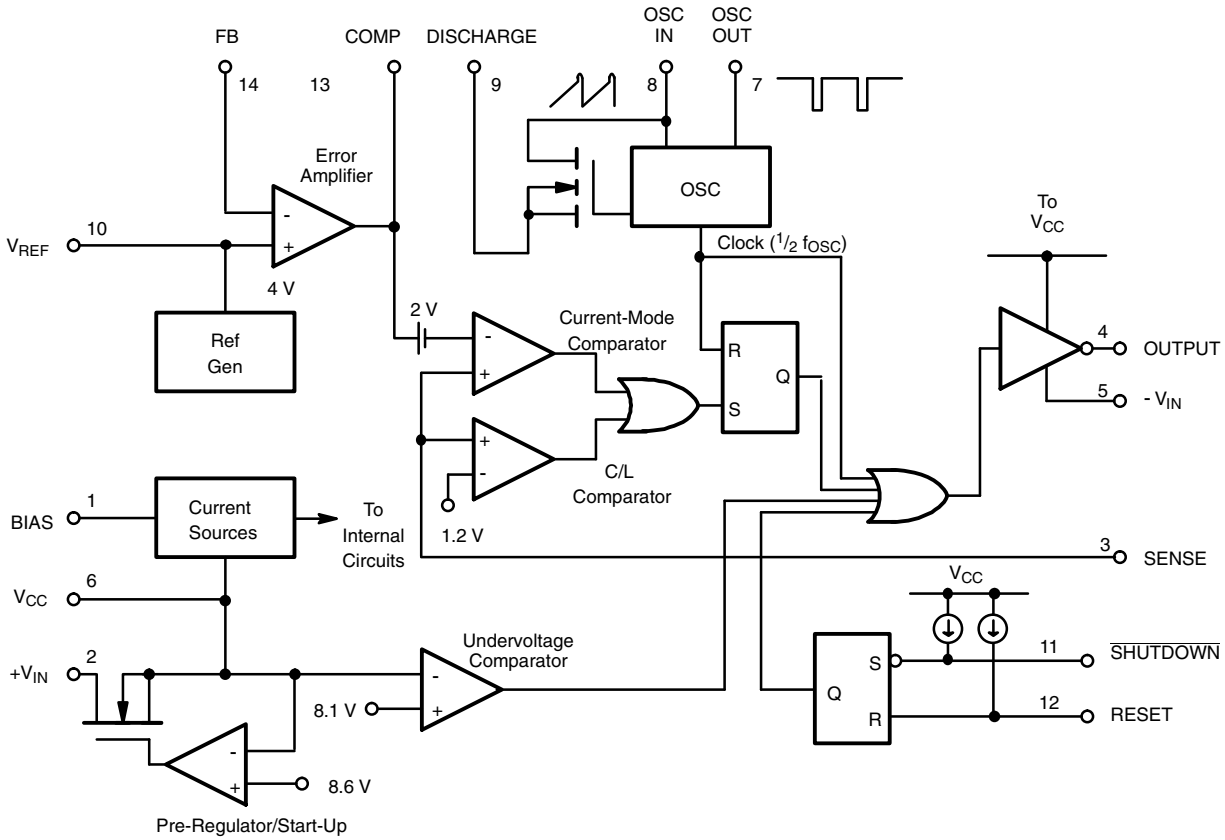
A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9110/9111 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9110/9111 are available in both standard and lead (Pb)-free 14-pin plastic DIP and SOIC packages which are specified to operate over the industrial temperature range of - 40 °C to 85 °C.

FEATURES

- 10 V to 120 V Input Range
- Current-Mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation (> 80 %)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET
- Reference Selection
  Si9110 - ± 1 %
  Si9111 - ± 10 %

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Voltages Referenced to - V_{IN} (Note: V_{CC} < + V_{IN} + 0.3 V)			
V_{CC}		15	V
$+V_{IN}$		120	
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN, OSC OUT)		- 0.3 to V_{CC} + 0.3	
Linear Inputs (FEEDBACK, SENSE, BIAS, V_{REF})		- 0.3 to V_{CC} + 0.3	
HV Pre-Regulator Input Current (continuous)		5	mA
Storage Temperature		- 65 to 150	°C
Operating Temperature		- 40 to 85	
Junction Temperature (T_J)		150	
Power Dissipation (Package)[a]	14-Pin Plastic DIP (J Suffix)[b]	750	mW
	14-Pin SOIC (Y Suffix)[c]	900	
Thermal Impedance (Θ_{JA})	14-Pin Plastic DIP	167	°C/W
	14-Pin SOIC	140	

Notes:
a. Device Mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25 °C.
c. Derate 7.2 mW/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Voltages Referenced to - V_{IN}		
V_{CC}	9.5 to 13.5	V
+ V_{IN}	10 to 120	
f_{OSC}	40 kHz to 1 MHz	
R_{OSC}	25 kΩ to 1 MΩ	
Linear Inputs	0 to V_{CC} - 3	V
Digital Inputs	0 to V_{CC}	

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = - V_{IN} = 0 V, V_{CC} = 10 V, + V_{IN} = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ		Temp.[b]	D Suffix - 40 °C to 85 °C Min.[d]	Typ.[c]	Max.[d]	Unit
Reference								
Output Voltage	V_R	OSC IN = - V_{IN} (OSC Disabled) R_L = 10 MΩ	Si9110	Room	3.92	4.0	4.08	V
			Si9111	Room	3.60	4.0	4.40	
			Si9110	Full	3.86		4.14	
			Si9111	Full	3.52		4.46	
Output Impedance[e]	Z_{OUT}			Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	V_{REF} = - V_{IN}		Room	70	100	130	µA
Temperature Stability[e]	T_{REF}			Full		0.5	1.0	mV/°C
Oscillator								
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0		Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note f		Room	80	100	120	kHz
		R_{OSC} = 150 k, See Note f		Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) - f(9.5 V)/f(9.5 V)		Room		10	15	%
Temperature Coefficient[e]	T_{OSC}			Full		200	500	ppm/°C

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = - V_{IN} = 0 V, V_{CC} = 10 V, + V_{IN} = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ		Temp.[b]	D Suffix - 40 °C to 85 °C Min.[d]	Typ.[c]	Max.[d]	Unit
Error Amplifier								
Feedback Input Voltage	V_{FB}	FB Tied to COMP, OSC IN = - V_{IN}, (OSC Disabled)	Si9110	Room	3.96	4.00	4.04	V
			Si9111	Room	3.60	4.00	4.40	
Input BIAS Current	I_{FB}	OSC IN = - V_{IN}, V_{FB} = 4 V		Room		25	500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = - V_{IN} (OSC Disabled)		Room		± 15	± 40	mV
Open Loop Voltage Gain[e]	A_{VOL}			Room	60	80		dB
Unity Gain Bandwidth[e]	BW			Room	1	1.3		MHz
Dynamic Output Impedance[e]	Z_{OUT}			Room		1000	2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)		Room		- 2.0	- 1.4	mA
		Sink (V_{FB} = 4.5 V)		Room	0.12	0.15		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V		Room	50	70		dB
Current Limit								
Threshold Voltage	V_{SOURCE}	V_{FB} = 0		Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1		Room		100	150	ns
Pre-Regulator/Start-Up								
Input Voltage	+ V_{IN}	I_{IN} = 10 µA		Room	120			V
Input Leakage Current	+ I_{IN}	V_{CC} ≥ 9.4 V		Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = V_{ULVO}		Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA		Room	7.8	8.6	9.4	V
Undervoltage Lockout	V_{UVLO}			Room	7.0	8.1	8.9	
V_{REG} - V_{UVLO}	V_{DELTA}			Room	0.3	0.6		
Supply								
Supply Current	I_{CC}	V_{LOAD} ≤ 75 pF (Pin 4)		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}			Room	10	15	20	µA
Logic								
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	C_L = 500 pF, V_{SENSE} = - V_{IN}, See Figure 2		Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3		Room	50			
RESET Pulse Width[e]	t_{RW}			Room	50			
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low[e]	t_{LW}	See Figure 3		Room	25			
Input Low Voltage	V_{IL}			Room			2.0	V
Input High Voltage	V_{IH}			Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V		Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V		Room	- 35	- 25		
Output								
Output High Voltage	V_{OH}	I_{OUT} = - 10 mA		Room Full	9.7 9.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA		Room Full			0.30 0.50	
Output Resistance	R_{OUT}	I_{OUT} = 10 mA, Source or Sink		Room Full		20 25	30 50	Ω
Rise Time[e]	t_r	C_L = 500 pF		Room		40	75	ns
Fall Time[e]	t_f			Room		40	75	

Notes:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF.

TIMING WAVEFORMS

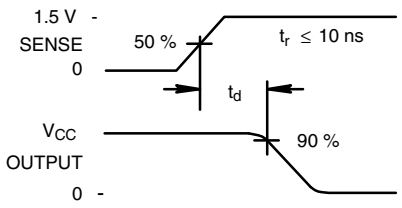


Figure 1.

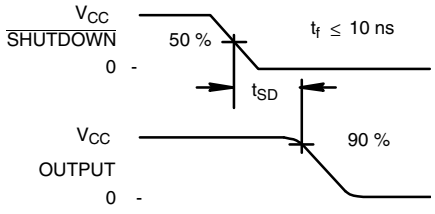


Figure 2.

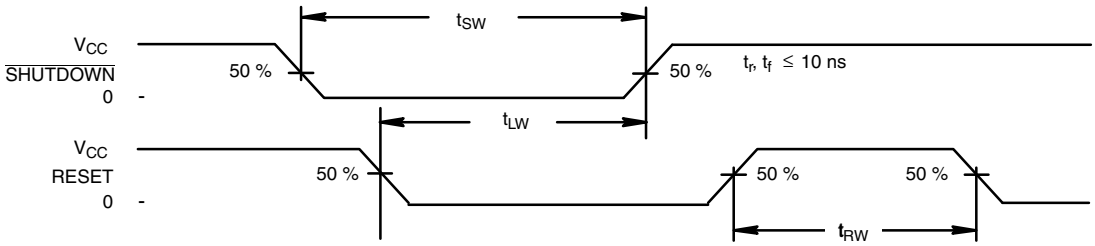


Figure 3.

TYPICAL CHARACTERISTICS

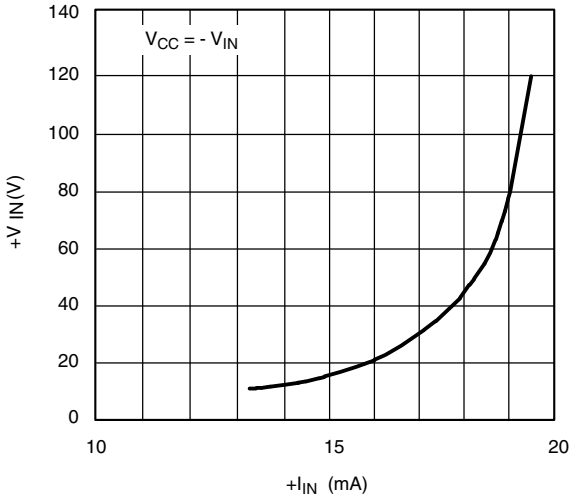


Figure 4. + V_{IN} vs. + I_{IN} at Start-Up

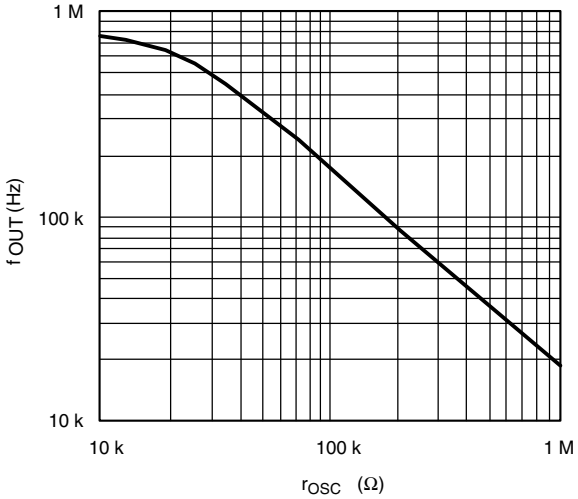


Figure 5. Output Switching Frequency vs. Oscillator Resistance

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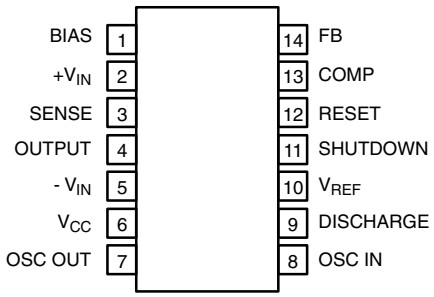
PIN CONFIGURATIONS AND ORDERING INFORMATION

Dual-In-Line and SOIC



Top View

ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9110DY	- 40 °C to 85 °C	SOIC-14
Si9110DY-T1		
Si9110DY-T1-E3		
Si9111DY		
Si9111DY-T1		
Si9111DY-T1-E3		
Si9110DJ		PDIP-14
Si9110DJ-E3		
Si9111DJ		
Si9111DJ-E3		

DETAILED DESCRIPTION

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9110/9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, + V_{IN} (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between + V_{IN} and V_{CC} (pin 6). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 8.6 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 6 gives the typical pre-regulator current at BiC/DMOS as a function of input voltage.

BIAS

To properly set the bias for the Si9110/9111, a 390 kΩ resistor should be tied from BIAS (pin 1) to - V_{IN} (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

Reference Section

The reference section of the Si9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ± 1 % of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1 % accuracy. The Si9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10 % accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

DETAILED DESCRIPTION (CONT'D)

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to - V_{IN} for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50 % by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude and 0.5 µs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	↑	Off (Not Latched)
L	L	Off (Latched)
↑	L	Off (Latched, No Change)

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Output Driver

The push-pull driver output has a typical on-resistance of 20 Ω . Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Vishay Siliconix D469A. The D469A can switch very large devices such as the SMM20N50 (500 V, 0.3 Ω) in approximately 100 ns.

APPLICATIONS

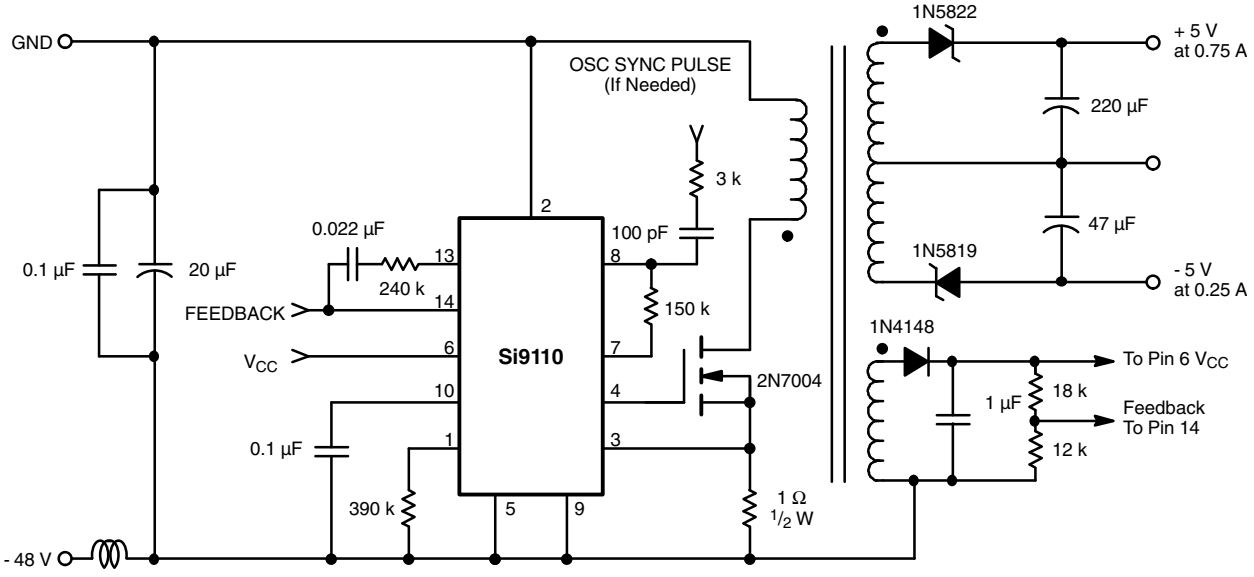
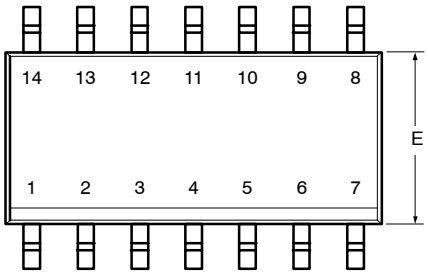
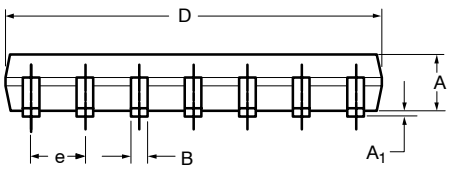


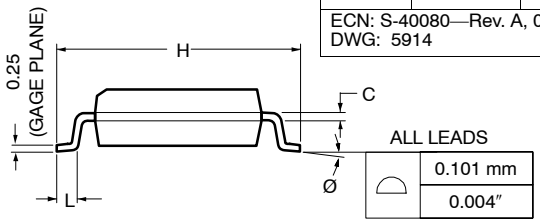
Figure 6. 5 Watt Power Supply for Telecom Applications

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70004.

SOIC (NARROW): 14-LEAD (POWER IC ONLY)



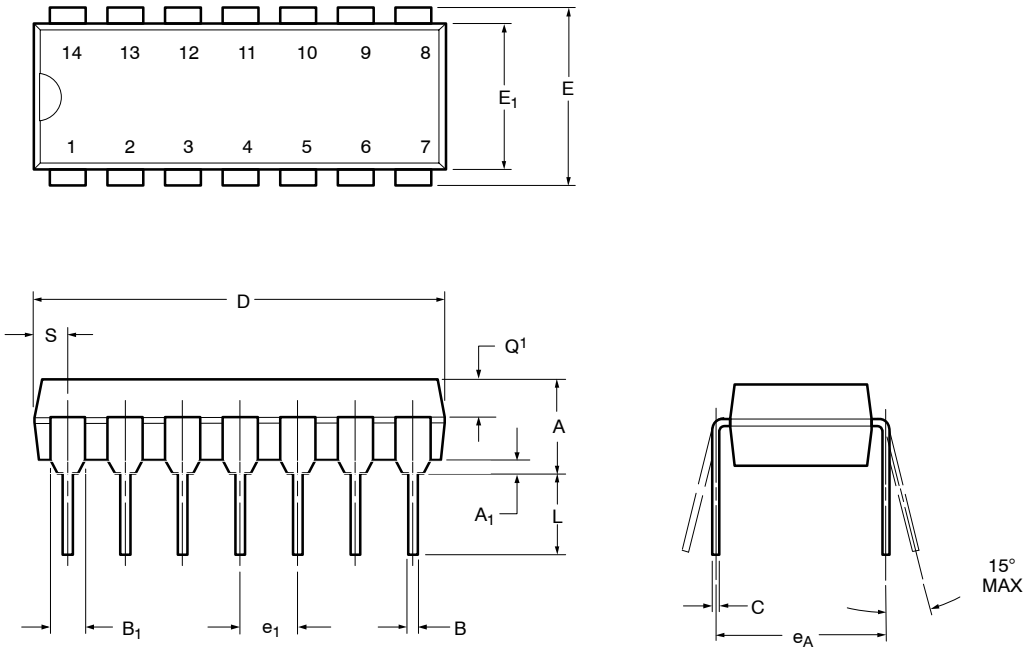




Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	8.55	8.75	0.336	0.344
E	3.8	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
Ø	0°	8°	0°	8°

ECN: S-40080—Rev. A, 02-Feb-04
DWG: 5914

PDIP: 14-LEAD (POWER IC ONLY)



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	17.27	19.30	0.680	0.760
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	1.02	2.03	0.040	0.080

ECN: S-40081—Rev. A, 02-Feb-04
DWG: 5919

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