PCA9506

40-bit I²C-bus I/O port with RESET, OE, and INT

Rev. 01 — 14 February 2006 Product data sheet

1. General description

The PCA9506 provides 40-bit parallel input/output (I/O) port expansion for I²C-bus applications organized in 5 banks of 8 I/Os. At 5 V supply voltage, the outputs are capable of sourcing 10 mA and sinking 25 mA with a total package load of 800 mA to allow direct driving of 40 LEDs. Any of the 40 I/O ports can be configured as an input or output. Output ports are totem-pole and their logic state changes at the Acknowledge (bank change).

The device can be configured to have each input port to be masked in order to prevent it from generating interrupts when its state changes and to have the I/O data logic state to be inverted when read by the system master.

An open-drain interrupt (INT) output pin allows monitoring of the input pins and is asserted each time a change occurs in one or several input ports (unless masked).

The Output Enable (OE) pin 3-states any I/O selected as output and can be used as an input signal to blink or dim LEDs (PWM with frequency > 80 Hz and change duty cycle).

The internal Power-On Reset (POR) or hardware reset (RESET) pin initializes the 40 I/Os as inputs. Three address select pins configure one of 8 slave addresses.

The PCA9506 is available in 56-pin TSSOP and HVQFN packages and is specified over the –40 °C to +85 °C industrial temperature range.

2. Features

- Standard mode (100 kHz) and Fast mode (400 kHz) compatible I²C-bus serial interface
- 2.3 V to 5.5 V operation with 5.5 V tolerant I/Os
- 40 configurable I/O pins that default to inputs at power-up
- Outputs:
  - Totem-pole (10 mA source, 25 mA sink) with controlled edge rate output structure
  - Active LOW output enable (OE) input pin 3-states all outputs
  - Output state change on Acknowledge
- Inputs:
  - Open-drain active LOW interrupt (INT) output pin allows monitoring of logic level change of pins programmed as inputs
  - Programmable Interrupt Mask Control for input pins that do not require an interrupt when their states change
  - Polarity Inversion register allows inversion of the polarity of the I/O pins when read
- Active LOW reset (RESET) input pin resets device to power-up default state
- 3 programmable address pins allowing 8 devices on the same bus

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- Designed for live insertion
  - Minimize line disturbance (I_{OFF} and power-up 3-state)
  - Signal transient rejection (50 ns noise filter and robust I^{2}C-bus state machine)
- Low standby current
- –40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA
- Offered in TSSOP56 and HVQFN56 packages

3. Applications

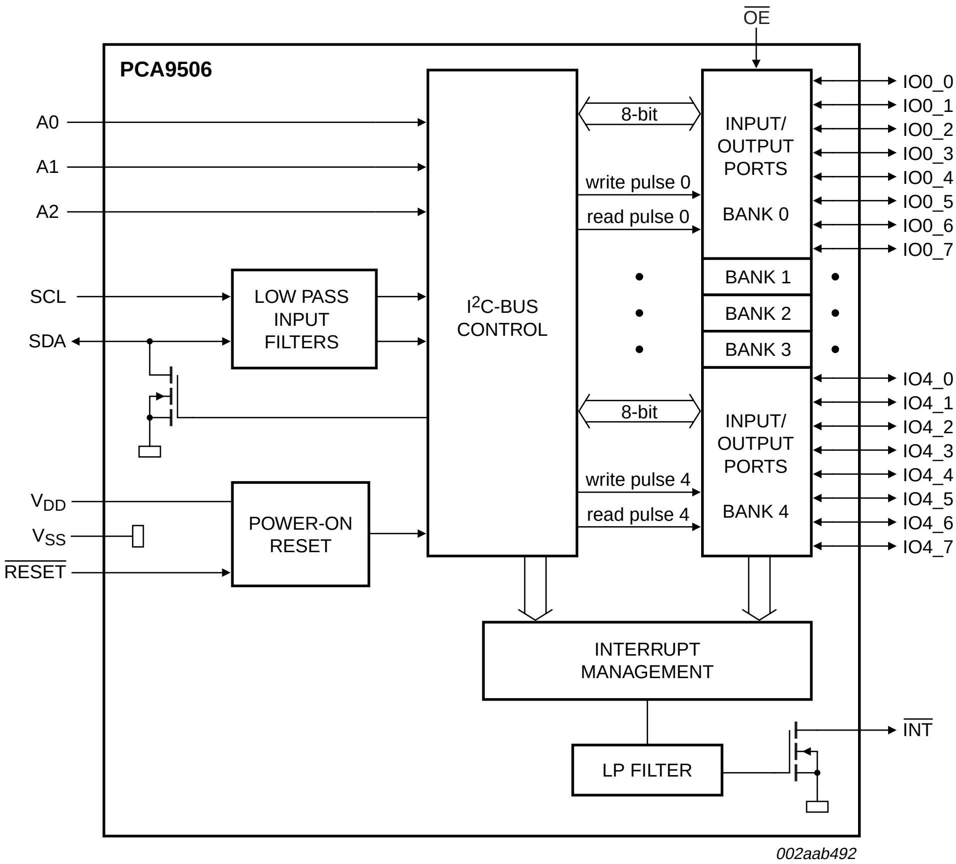
- Servers
- RAID systems
- Industrial control
- Medical equipment
- PLCs
- Cell phones
- Gaming machines
- Instrumentation and test measurement

4. Ordering information

Table 1: Ordering information

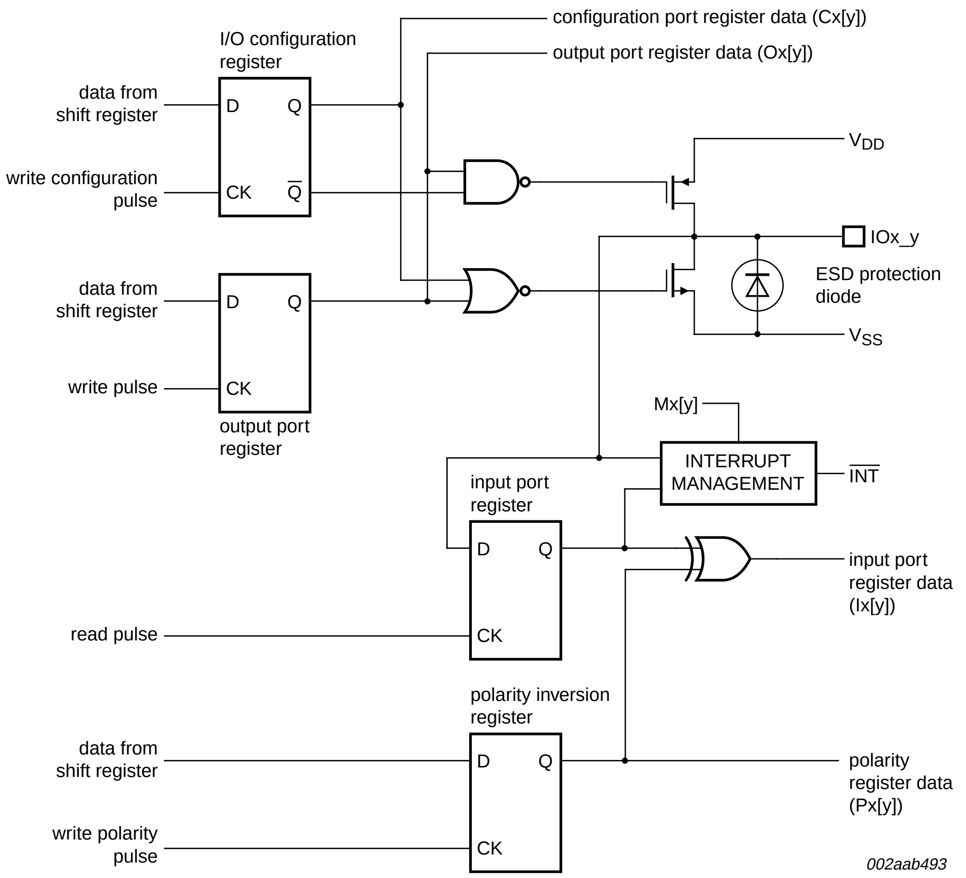
Type number	Topside mark	Package		
		Name	Description	Version
PCA9506DGG	PCA9506DGG	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
PCA9506BS	PCA9506BS	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-1

5. Block diagram



All I/Os are set to inputs at power-up and RESET.

Fig 1. Block diagram of PCA9506



On power-up or RESET, all registers return to default values.

Fig 2. Simplified schematic of IO0_0 to IO4_7

6. Pinning information

6.1 Pinning

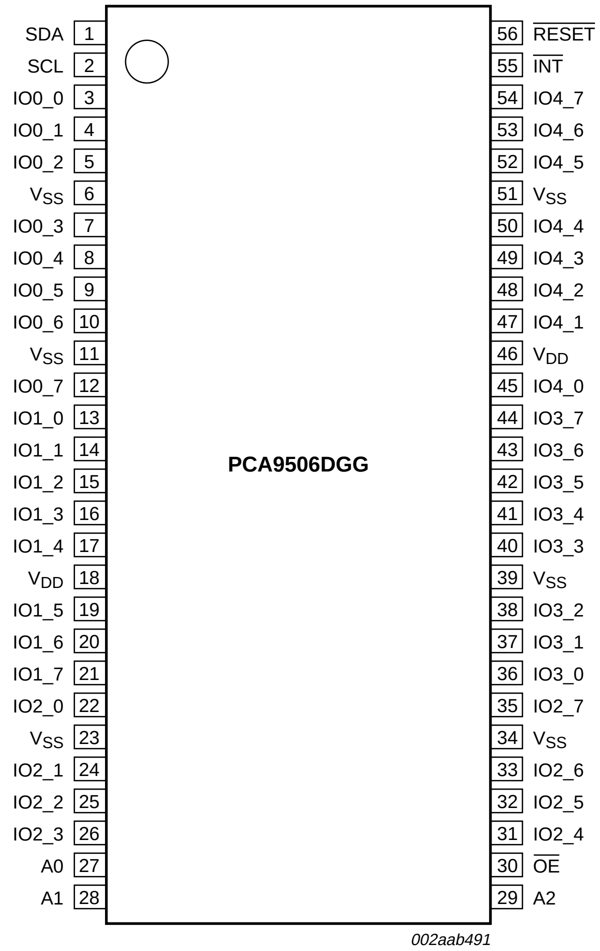


Fig 3. Pin configuration for TSSOP56

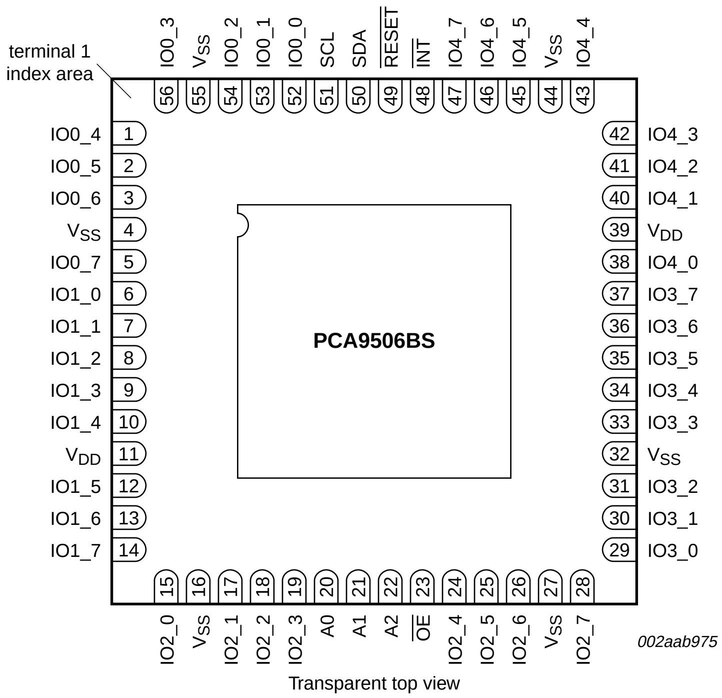


Fig 4. Pin configuration for HVQFN56

6.2 Pin description

Table 2: Pin description

Symbol	Pin		Type	Description
	TSSOP56	HVQFN56		
SDA	1	50	I/O	serial data line
SCL	2	51	I	serial clock line
IO0_0 to IO0_7	3, 4, 5, 7, 8, 9, 10, 12	52, 53, 54, 56, 1, 2, 3, 5	I/O	input/output bank 0
IO1_0 to IO1_7	13, 14, 15, 16, 17, 19, 20, 21	6, 7, 8, 9, 10, 12, 13, 14	I/O	input/output bank 1
IO2_0 to IO2_7	22, 24, 25, 26, 31, 32, 33, 35	15, 17, 18, 19, 24, 25, 26, 28	I/O	input/output bank 2
IO3_0 to IO3_7	36, 37, 38, 40, 41, 42, 43, 44	29, 30, 31, 33, 34, 35, 36, 37	I/O	input/output bank 3
IO4_0 to IO4_7	45, 47, 48, 49, 50, 52, 53, 54	38, 40, 41, 42, 43, 45, 46, 47	I/O	input/output bank 4
V_{SS}	6, 11, 23, 34, 39, 51	4, 16, 27, 32, 44, 55 [1]	power supply	ground supply voltage
V_{DD}	18, 46	11, 39	power supply	supply voltage
A0	27	20	I	address input 0
A1	28	21	I	address input 1
A2	29	22	I	address input 2

Table 2: Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP56	HVQFN56		
$\overline{\text{OE}}$	30	23	I	active LOW output enable input
$\overline{\text{INT}}$	55	48	O	active LOW interrupt output
$\overline{\text{RESET}}$	56	49	I	active LOW reset input

[1] HVQFN package die supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to Figure 1 "Block diagram of PCA9506" and Figure 2 "Simplified schematic of IO0_0 to IO4_7".

7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9506 is shown in Figure 5. Slave address pins A2, A1, and A0 choose 1 of 8 slave addresses and need to be connected to V_{DD} (1) or V_{SS} (0). To conserve power, no internal pull-up resistors are incorporated on A2, A1, and A0.

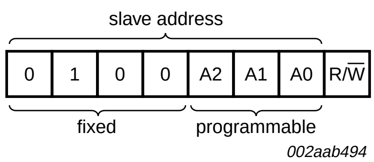


Fig 5. PCA9506 address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.2 Command register

Following the successful acknowledgement of the slave address + R/$\overline{\text{W}}$ bit, the bus master will send a byte to the PCA9506, which will be stored in the Command register.

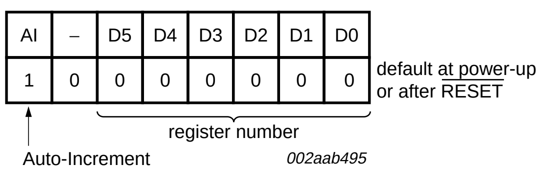


Fig 6. Command register

The lowest 6 bits are used as a pointer to determine which register will be accessed. The registers are:

- IP: Input Port registers (5 registers)
- OP: Output Port registers (5 registers)
- PI: Polarity Inversion registers (5 registers)
- IOC: I/O Configuration registers (5 registers)
- MSK: Mask interrupt registers (5 registers)

If the Auto-Increment flag is set (AI = 1), the 3 least significant bits are automatically incremented after a read or write. This allows the user to program and/or read the 5 register banks sequentially.

If more than 5 bytes of data are written and AI = 1, previous data in the selected registers will be overwritten. Reserved registers are skipped and not accessed (refer to Table 3).

If the Auto-Increment flag is cleared (AI = 0), the 3 least significant bits are not incremented after data is read or written. During a read operation, the same register bank is read each time. During a write operation, data is written to the same register bank each time.

Only a Command register code with the 5 least significant bits equal to the 25 allowable values as defined in Table 3 are valid. Reserved or undefined command codes must not be accessed for proper device functionality. At power-up, this register defaults to 0x80, with the AI bit set to logic 1, and the lowest 7 bits set to logic 0.

During a write operation, the PCA9506 will acknowledge a byte sent to OPx, PIx, and IOCx and MSKx registers, but will not acknowledge a byte sent to the IPx registers since these are read-only registers.

7.3 Register definitions

Table 3: Register summary

Register # (hex)	D5	D4	D3	D2	D1	D0	Symbol	Access	Description
Input Port registers									
00	0	0	0	0	0	0	IP0	read only	Input Port register bank 0
01	0	0	0	0	0	1	IP1	read only	Input Port register bank 1
02	0	0	0	0	1	0	IP2	read only	Input Port register bank 2
03	0	0	0	0	1	1	IP3	read only	Input Port register bank 3
04	0	0	0	1	0	0	IP4	read only	Input Port register bank 4
05	0	0	0	1	0	1	-	-	reserved for future use
06	0	0	0	1	1	0	-	-	reserved for future use
07	0	0	0	1	1	1	-	-	reserved for future use
Output Port registers									
08	0	0	1	0	0	0	OP0	read/write	Output Port register bank 0
09	0	0	1	0	0	1	OP1	read/write	Output Port register bank 1
0A	0	0	1	0	1	0	OP2	read/write	Output Port register bank 2
0B	0	0	1	0	1	1	OP3	read/write	Output Port register bank 3
0C	0	0	1	1	0	0	OP4	read/write	Output Port register bank 4
0D	0	0	1	1	0	1	-	-	reserved for future use
0E	0	0	1	1	1	0	-	-	reserved for future use
0F	0	0	1	1	1	1	-	-	reserved for future use
Polarity Inversion registers									
10	0	1	0	0	0	0	PI0	read/write	Polarity Inversion register bank 0
11	0	1	0	0	0	1	PI1	read/write	Polarity Inversion register bank 1
12	0	1	0	0	1	0	PI2	read/write	Polarity Inversion register bank 2
13	0	1	0	0	1	1	PI3	read/write	Polarity Inversion register bank 3
14	0	1	0	1	0	0	PI4	read/write	Polarity Inversion register bank 4
15	0	1	0	1	0	1	-	-	reserved for future use
16	0	1	0	1	1	0	-	-	reserved for future use
17	0	1	0	1	1	1	-	-	reserved for future use
I/O Configuration registers									
18	0	1	1	0	0	0	IOC0	read/write	I/O Configuration register bank 0
19	0	1	1	0	0	1	IOC1	read/write	I/O Configuration register bank 1
1A	0	1	1	0	1	0	IOC2	read/write	I/O Configuration register bank 2
1B	0	1	1	0	1	1	IOC3	read/write	I/O Configuration register bank 3
1C	0	1	1	1	0	0	IOC4	read/write	I/O Configuration register bank 4
1D	0	1	1	1	0	1	-	-	reserved for future use
1E	0	1	1	1	1	0	-	-	reserved for future use
1F	0	1	1	1	1	1	-	-	reserved for future use

Table 3: Register summary *…continued*

Register # (hex)	D5	D4	D3	D2	D1	D0	Symbol	Access	Description
Mask Interrupt registers									
20	1	0	0	0	0	0	MSK0	read/write	Mask Interrupt register bank 0
21	1	0	0	0	0	1	MSK1	read/write	Mask Interrupt register bank 1
22	1	0	0	0	1	0	MSK2	read/write	Mask Interrupt register bank 2
23	1	0	0	0	1	1	MSK3	read/write	Mask Interrupt register bank 3
24	1	0	0	1	0	0	MSK4	read/write	Mask Interrupt register bank 4
25	1	0	0	1	0	1	-	-	reserved for future use
26	1	0	0	1	1	0	-	-	reserved for future use
27	1	0	0	1	1	1	-	-	reserved for future use

7.3.1 IP0 to IP4 - Input Port registers

These registers are read-only. They reflect the incoming logic levels of the port pins regardless of whether the pin is defined as an input or an output by the I/O Configuration register. If the corresponding Px[y] bit in the PI registers is set to logic 0, or the inverted incoming logic levels if the corresponding Px[y] bit in the PI register is set to logic 1. Writes to these registers have no effect.

Table 4: IP0 to IP4 - Input Port registers (address 00h to 04h) bit description
*Legend: * default value 'X' determined by the externally applied logic level.*

Address	Register	Bit	Symbol	Access	Value	Description
00h	IP0	7 to 0	I0[7:0]	R	XXXX XXXX*	Input Port register bank 0
01h	IP1	7 to 0	I1[7:0]	R	XXXX XXXX*	Input Port register bank 1
02h	IP2	7 to 0	I2[7:0]	R	XXXX XXXX*	Input Port register bank 2
03h	IP3	7 to 0	I3[7:0]	R	XXXX XXXX*	Input Port register bank 3
04h	IP4	7 to 0	I4[7:0]	R	XXXX XXXX*	Input Port register bank 4

The Polarity Inversion register can invert the logic states of the port pins. The polarity of the corresponding bit is inverted when Px[y] bit in the PI register is set to logic 1. The polarity of the corresponding bit is not inverted when Px[y] bits in the PI register is set to logic 0.

7.3.2 OP0 to OP4 - Output Port registers

These registers reflect the outgoing logic levels of the pins defined as outputs by the I/O Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the values that are in the flip-flops controlling the output selection, **not** the actual pin values.

Ox[y] = 0: IOx_y = 0 if IOx_y defined as output (Cx[y] in IOC register = 0).

Ox[y] = 1: IOx_y = 1 if IOx_y defined as output (Cx[y] in IOC register = 0).

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

Table 5: OP0 to OP4 - Output Port registers (address 08h to 0Ch) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
08h	OP0	7 to 0	O0[7:0]	R/W	0000 0000*	Output Port register bank 0
09h	OP1	7 to 0	O1[7:0]	R/W	0000 0000*	Output Port register bank 1
0Ah	OP2	7 to 0	O2[7:0]	R/W	0000 0000*	Output Port register bank 2
0Bh	OP3	7 to 0	O3[7:0]	R/W	0000 0000*	Output Port register bank 3
0Ch	OP4	7 to 0	O4[7:0]	R/W	0000 0000*	Output Port register bank 4

7.3.3 PI0 to PI4 - Polarity Inversion registers

These registers allow inversion of the polarity of the corresponding Input Port register.

Px[y] = 0: The corresponding Input Port register data polarity is retained.

Px[y] = 1: The corresponding Input Port register data polarity is inverted.

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

Table 6: PI0 to PI4 - Polarity Inversion registers (address 10h to 14h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
10h	PI0	7 to 0	P0[7:0]	R/W	0000 0000*	Polarity Inversion register bank 0
11h	PI1	7 to 0	P1[7:0]	R/W	0000 0000*	Polarity Inversion register bank 1
12h	PI2	7 to 0	P2[7:0]	R/W	0000 0000*	Polarity Inversion register bank 2
13h	PI3	7 to 0	P3[7:0]	R/W	0000 0000*	Polarity Inversion register bank 3
14h	PI4	7 to 0	P4[7:0]	R/W	0000 0000*	Polarity Inversion register bank 4

7.3.4 IOC0 to IOC4 - I/O Configuration registers

These registers configure the direction of the I/O pins.

Cx[y] = 0: The corresponding port pin is an output.

Cx[y] = 1: The corresponding port pin is an input.

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

Table 7: IOC0 to IOC4 - I/O Configuration registers (address 18h to 1Ch) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
18h	IOC0	7 to 0	C0[7:0]	R/W	1111 1111*	I/O Configuration register bank 0
19h	IOC1	7 to 0	C1[7:0]	R/W	1111 1111*	I/O Configuration register bank 1
1Ah	IOC2	7 to 0	C2[7:0]	R/W	1111 1111*	I/O Configuration register bank 2
1Bh	IOC3	7 to 0	C3[7:0]	R/W	1111 1111*	I/O Configuration register bank 3
1Ch	IOC4	7 to 0	C4[7:0]	R/W	1111 1111*	I/O Configuration register bank 4

7.3.5 MSK0 to MSK4 - Mask interrupt registers

These registers mask the interrupt due to a change in the I/O pins configured as inputs. 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

Mx[y] = 0: A level change at the I/O will generate an interrupt if IOx_y defined as input (Cx[y] in IOC register = 1).

Mx[y] = 1: A level change in the input port will not generate an interrupt if IOx_y defined as input (Cx[y] in IOC register = 1).

Table 8: MSK0 to MSK4 - Mask interrupt registers (address 20h to 24h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
20h	MSK0	7 to 0	M0[7:0]	R/W	1111 1111*	Mask Interrupt register bank 0
21h	MSK1	7 to 0	M1[7:0]	R/W	1111 1111*	Mask Interrupt register bank 1
22h	MSK2	7 to 0	M2[7:0]	R/W	1111 1111*	Mask Interrupt register bank 2
23h	MSK3	7 to 0	M3[7:0]	R/W	1111 1111*	Mask Interrupt register bank 3
24h	MSK4	7 to 0	M4[7:0]	R/W	1111 1111*	Mask Interrupt register bank 4

7.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9506 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9506 registers and I²C-bus state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.5 RESET input

A reset can be accomplished by holding the RESET pin LOW for a minimum of $t_{w(rst)}$. The PCA9506 registers and I²C-bus state machine will be held in their default states until the RESET input is once again HIGH.

7.6 Interrupt output ($\overline{\text{INT}}$)

The open-drain active LOW interrupt is activated when one of the port pins changes state and the port pin is configured as an input and the interrupt on it is not masked. The interrupt is deactivated when the port pin input returns to its previous state or the Input Port register is read.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

Only a Read of the Input Port register that contains the bit(s) image of the input(s) that generated the interrupt clears the interrupt condition.

If more than one input register changed state before a read of the Input Port register is initiated, the interrupt is cleared when all the input registers containing all the inputs that changed are read.

Example: If IO0_5, IO2_3, and IO3_7 change state at the same time, the interrupt is cleared only when INREG0, INREG2, and INREG3 are read.

7.7 Output enable input ($\overline{\text{OE}}$)

The active LOW output enable pin allows to enable or disable all the I/Os at the same time. When a LOW level is applied to the $\overline{\text{OE}}$ pin, all the I/Os configured as outputs are enabled and the logic value programmed in their respective OP registers is applied to the pins. When a HIGH level is applied to the $\overline{\text{OE}}$ pin, all the I/Os configured as outputs are 3-stated.

For applications requiring LED blinking with brightness control, this pin can be used to control the brightness by applying a high frequency PWM signal on the $\overline{\text{OE}}$ pin. LEDs can be blinked using the Output Port registers and can be dimmed using the PWM signal on the $\overline{\text{OE}}$ pin thus controlling the brightness by adjusting the duty cycle.

7.8 Live insertion

The PCA9506 is fully specified for live insertion applications using I_{OFF}, power-up 3-states, robust state machine, and 50 ns noise filter. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state's circuitry places the outputs in the high-impedance state during power-up and power-down, which prevents driver conflict and bus contention.

The robust state machine does not respond until it sees a valid START condition and the 50 ns noise filter will filter out any insertion glitches. The PCA9506 will not cause corruption of active data on the bus, nor will the device be damaged or cause damage to devices already on the bus when similar featured devices are being used.

7.9 Standby

The PCA9506 goes into standby when the I^{2}C-bus is idle. Standby supply current is lower than 1 μA (typical).

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).

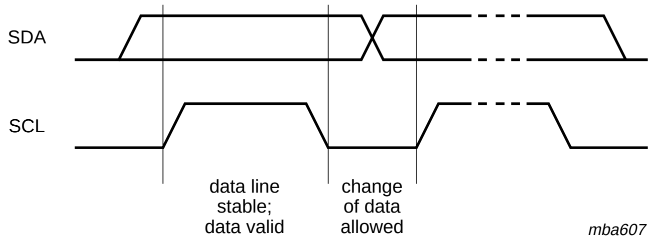


Fig 7. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 8).

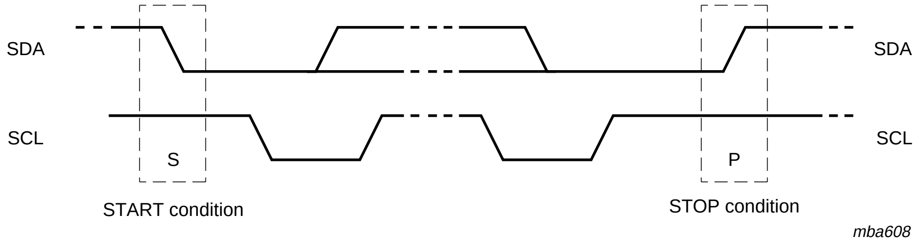


Fig 8. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 9).

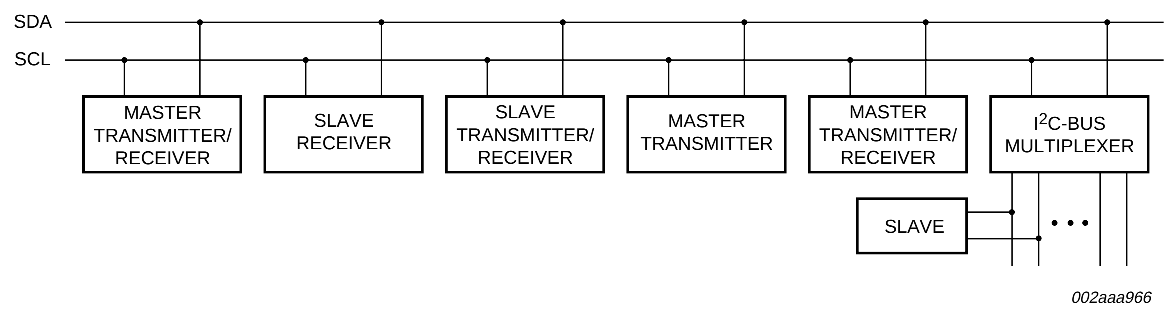


Fig 9. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

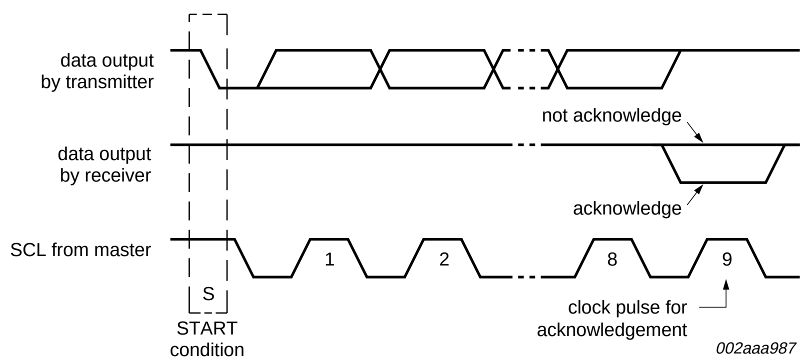
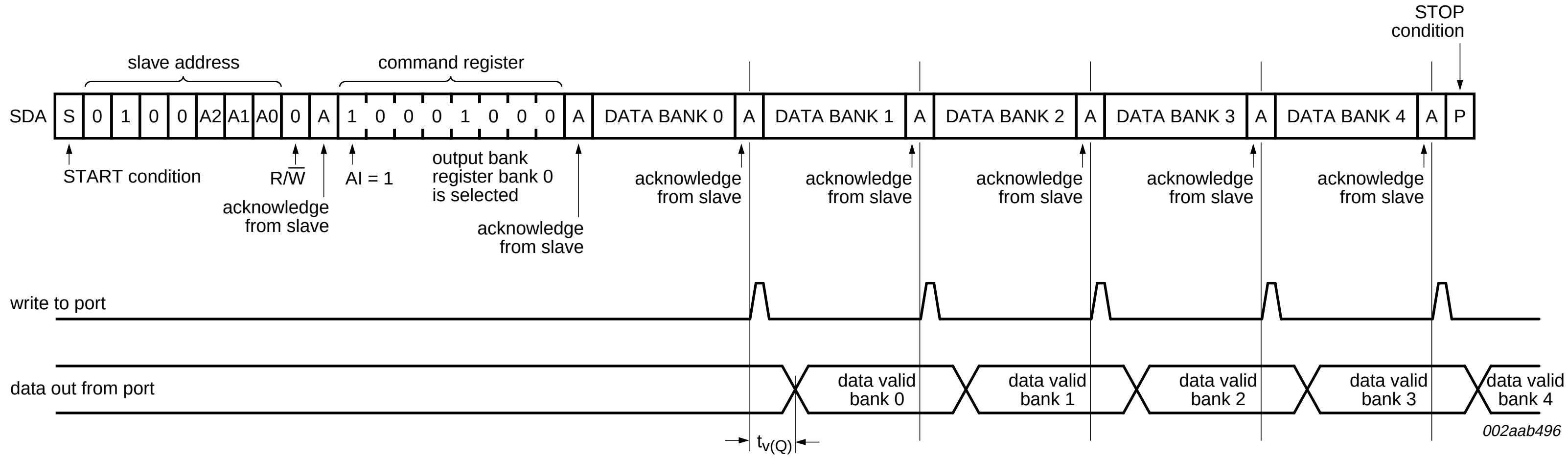


Fig 10. Acknowledgement on the I^2C-bus

8.4 Bus transactions

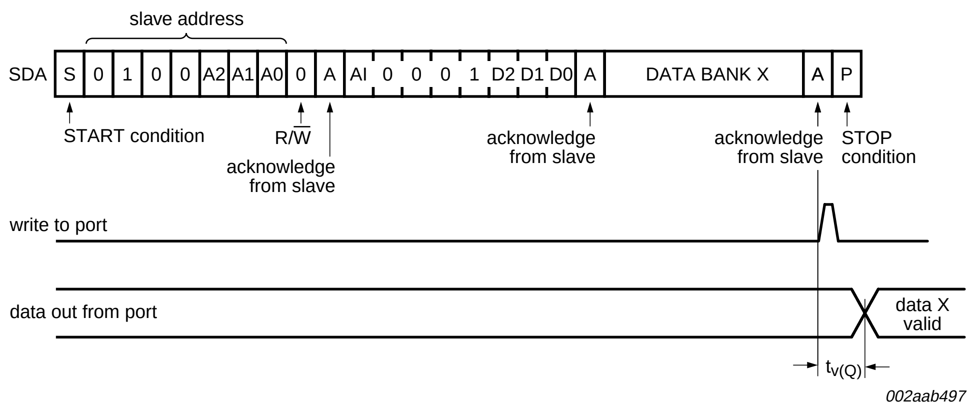
Data is transmitted to the PCA9506 registers using Write Byte transfers (see Figure 11, Figure 12, and Figure 13). Data is read from the PCA9506 registers using Read and Receive Byte transfers (see Figure 14).



$\overline{OE}$ is LOW to observe a change in the outputs.

If more than 5 bytes are written, previous data are overwritten.

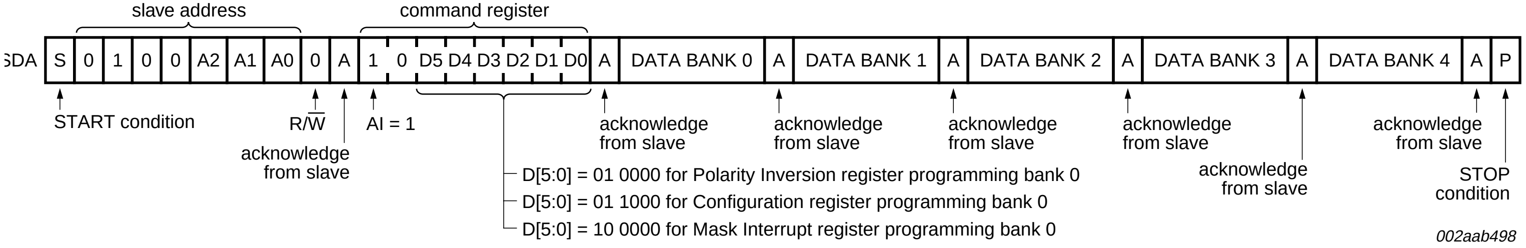
Fig 11. Write to the 5 output ports



$\overline{OE}$ is LOW to observe a change in the outputs.

Two, three, or four adjacent banks can be programmed by using the Auto-Increment feature (AI = 1) and change at the corresponding output port becomes effective at each acknowledgement.

Fig 12. Write to a specific output port

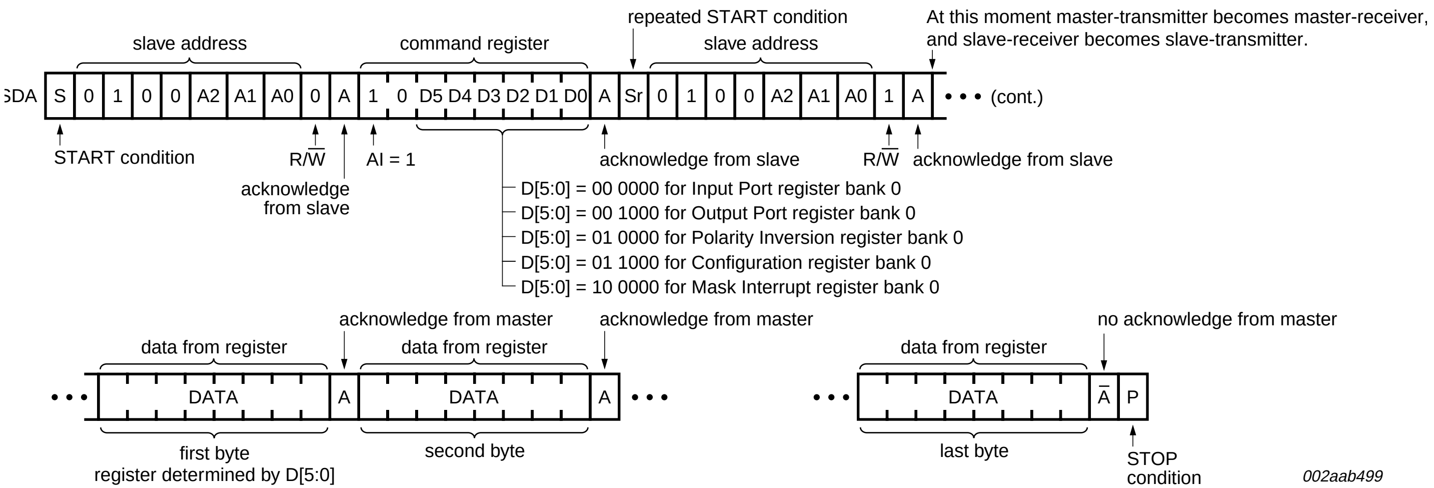


The programming becomes effective at the acknowledge.

Less than 5 bytes can be programmed by using this scheme. D5, D4, D3, D2, D1, D0 refers to the first register to be programmed.

If more than 5 bytes are written, previous data are overwritten (the sixth Configuration register will roll over to the first addressed Configuration register, the sixth Polarity Inversion register will roll over to the first addressed Polarity Inversion register and the sixth Mask Interrupt register will roll over to the first addressed Mask Interrupt register).

Fig 13. Write to the I/O Configuration, Polarity Inversion or Mask Interrupt registers



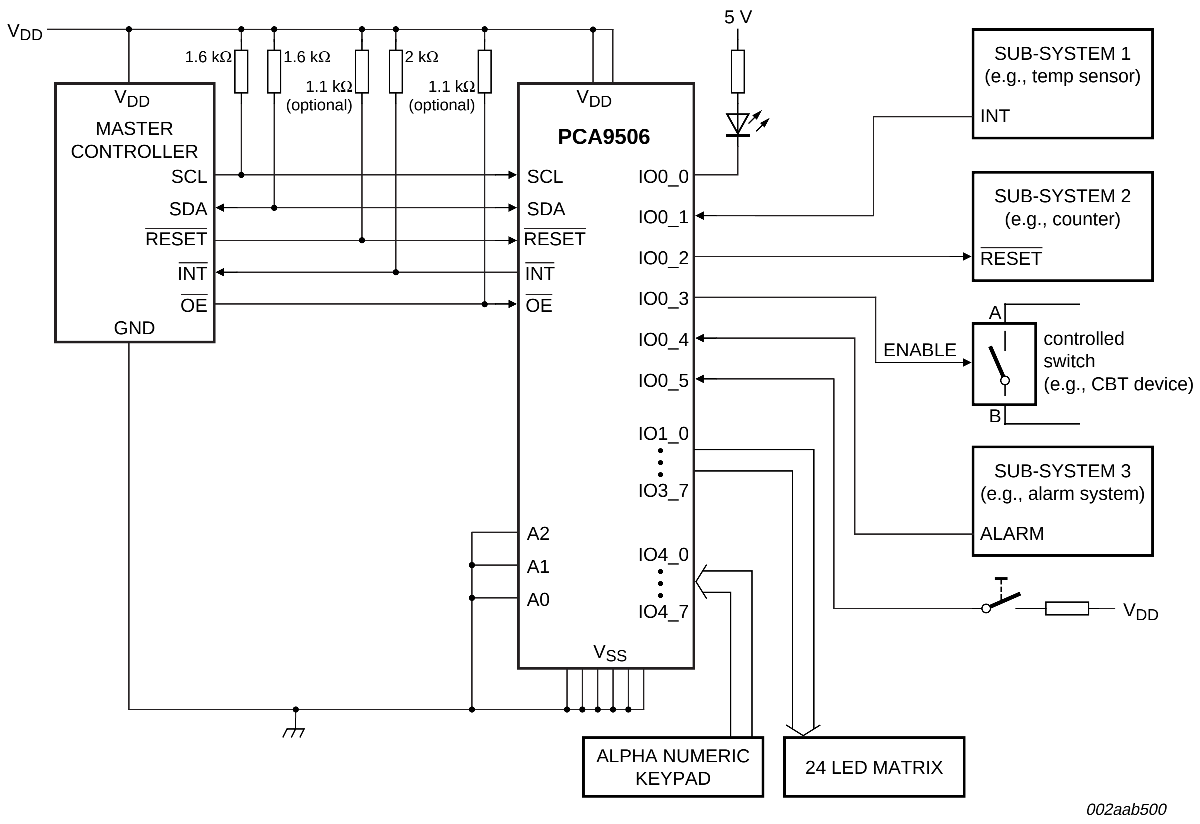
If AI = 0, the same register is read during the whole sequence.

If AI = 1, the register value is incremented after each read. When the last register bank is read, it rolls over to the first byte of the category (see category definition in Section 7.2 “Command register”).

The INT signal is released only when the last register containing an input that changed has been read. For example, when IO2_4 and IO4_7 change at the same time and an Input Port register’s read sequence is initiated, starting with IP0, INT is released after IP4 is read (and not after IP2 is read).

Fig 14. Read from Input Port, Output Port, I/O Configuration, Polarity Inversion or Mask Interrupt registers

9. Application design-in information



Device address configured as 0100 000X for this example.

IO0_0, IO0_2, IO0_3, IO1_0 to IO3_7 are configured as outputs.

IO0_1, IO0_4, IO4_0 to IO4_7 configured as inputs.

Fig 15. Typical application

10. Limiting values

Table 9: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6	V
V_I	input voltage		V_{SS} – 0.5	5.5	V
I_I	input current		-	±20	mA
$V_{I/O(n)}$	input/output voltage on any other pin		V_{SS} – 0.5	5.5	V
$V_{I/O(IO0n)}$	input/output voltage on pin IO0_n		V_{SS} – 0.5	5.5	V
$I_{O(I/On)}$	output current on an I/O pin		–20	+50	mA
I_{DD}	supply current		-	500	mA
I_{SS}	ground supply current		-	1100	mA
P_{tot}	total power dissipation		-	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	-	125	°C
		storage	-	150	°C

11. Static characteristics

Table 10: Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.3	-	5.5	V
I_{DD}	supply current	operating mode; no load; f_{SCL} = 400 kHz				
		V_{DD} = 2.3 V	-	56	95	µA
		V_{DD} = 3.3 V	-	98	150	µA
		V_{DD} = 5.5 V	-	225	300	µA
I_{stb}	standby current	no load; f_{SCL} = 0 kHz; I/O = inputs; $V_I = V_{DD}$				
		V_{DD} = 2.3 V	-	0.15	11	µA
		V_{DD} = 3.3 V	-	0.25	12	µA
		V_{DD} = 5.5 V	-	0.75	15.5	µA
V_{POR}	power-on reset voltage [1]	no load; $V_I = V_{DD}$ or V_{SS}	-	1.70	2.0	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		–0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	20	-	-	mA
I_L	leakage current	$V_I = V_{DD} = V_{SS}$	–1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	5	10	pF

Table 10: Static characteristics *...continued*

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I/Os						
V_{IL}	LOW-level input voltage		–0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V				
		V_{DD} = 2.3 V	10	-	-	mA
		V_{DD} = 3.0 V	12	-	-	mA
		V_{DD} = 4.5 V	15	-	-	mA
$I_{OL(tot)}$	total LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 4.5 V	-	-	0.6	A
V_{OH}	HIGH-level output voltage	I_{OH} = –10 mA				
		V_{DD} = 2.3 V	1.6	-	-	V
		V_{DD} = 3.0 V	2.3	-	-	V
		V_{DD} = 4.5 V	4.0	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 3.6 V; V_I = V_{DD}	–1	-	+1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; V_I = V_{SS}	–1	-	+1	µA
C_i	input capacitance		-	6	7	pF
C_o	output capacitance		-	6	7	pF
Interrupt INT						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	6	-	-	mA
I_{OH}	HIGH-level output current		–1	-	+1	µA
C_o	output capacitance		-	3.0	5	pF
Inputs RESET and OE						
V_{IL}	LOW-level input voltage		–0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2	-	5.5	V
I_{LI}	input leakage current		–1	-	+1	µA
C_i	input capacitance		-	3.0	5	pF
Inputs A0, A1, A2						
V_{IL}	LOW-level input voltage		–0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current		–1	-	+1	µA
C_i	input capacitance		-	3.5	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

12. Dynamic characteristics

Table 11: Dynamic characteristics

Symbol	Parameter	Conditions		Standard mode I²C-bus		Fast mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		[1]	0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time [2]			0.1	3.45	0.1	0.9	µs
$t_{VD;DAT}$	data valid time [3]			0.1	3.45	0.1	0.9	µs
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals		[4] [5]	-	300	$20 + 0.1C_b$ [6]	300	ns
t_r	rise time of both SDA and SCL signals		[4] [5]	-	1000	$20 + 0.1C_b$ [6]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[7]	-	50	-	50	ns
Port timing								
t_{en}	enable time	output		-	80	-	80	ns
t_{dis}	disable time	output		-	40	-	40	ns
$t_{v(Q)}$	data output valid time			-	250	-	250	ns
$t_{su(D)}$	data input setup time			100	-	100	-	ns
$t_{h(D)}$	data input hold time			0.5	-	0.5	-	µs
Interrupt timing								
$t_{v(INT\_N)}$	valid time on pin INT_N			-	4	-	4	µs
$t_{rst(INT\_N)}$	reset time on pin INT_N			-	4	-	4	µs
Reset								
$t_{w(rst)}$	reset pulse width			4	-	4	-	ns
$t_{rec(rst)}$	reset recovery time			0	-	0	-	ns
t_{rst}	reset time			100	-	100	-	ns

[1] Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either SDA or SCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.

[2] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[3] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[4] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] C_b = total capacitance of one bus line in pF.

[7] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

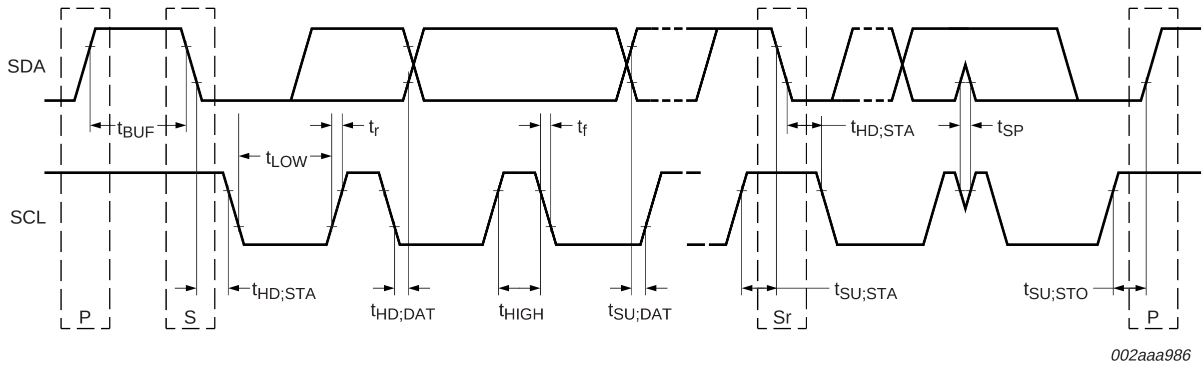
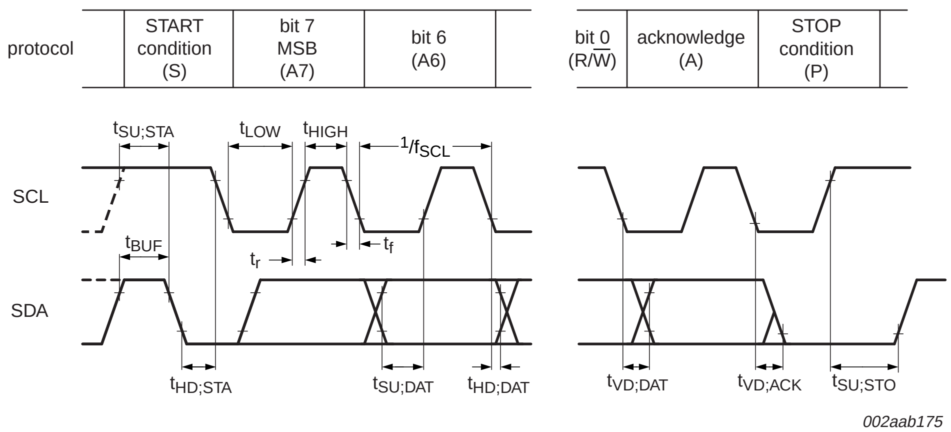


Fig 16. Definition of timing on the I^2C-bus



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 17. I^2C-bus timing diagram

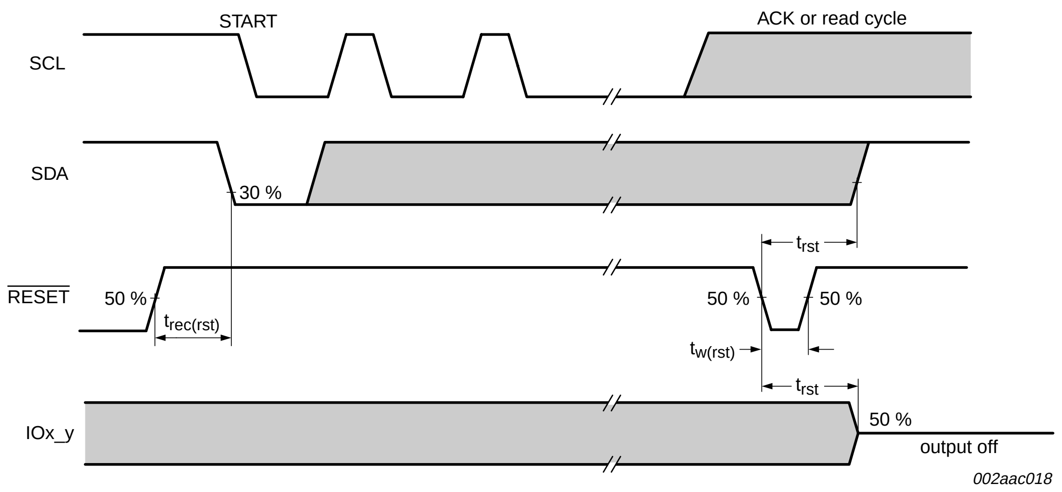
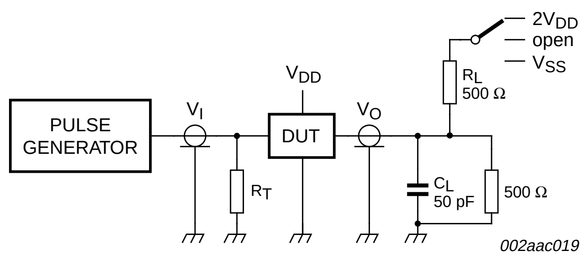


Fig 18. Reset timing

13. Test information



R_L = load resistance

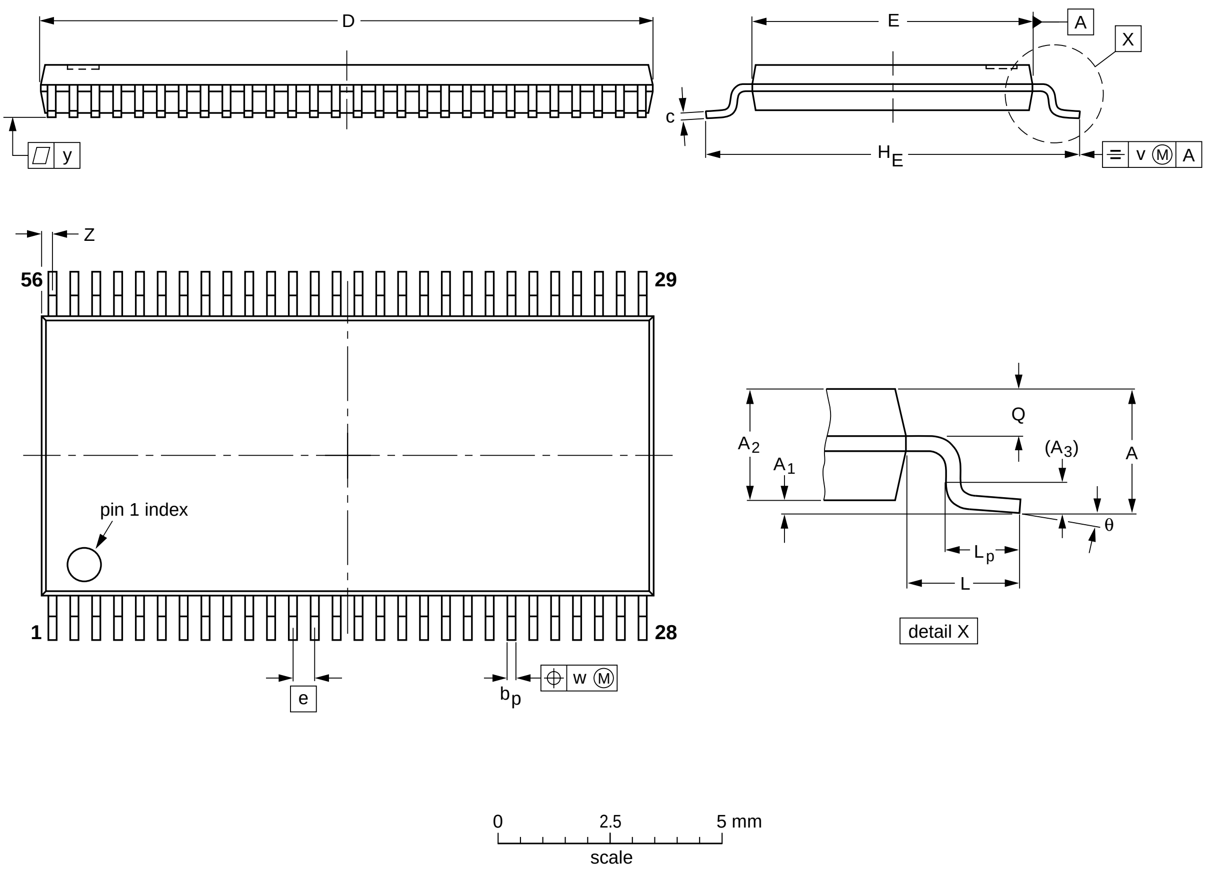
C_L = load capacitance includes jig and probe capacitance

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 19. Test circuitry for switching times

14. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

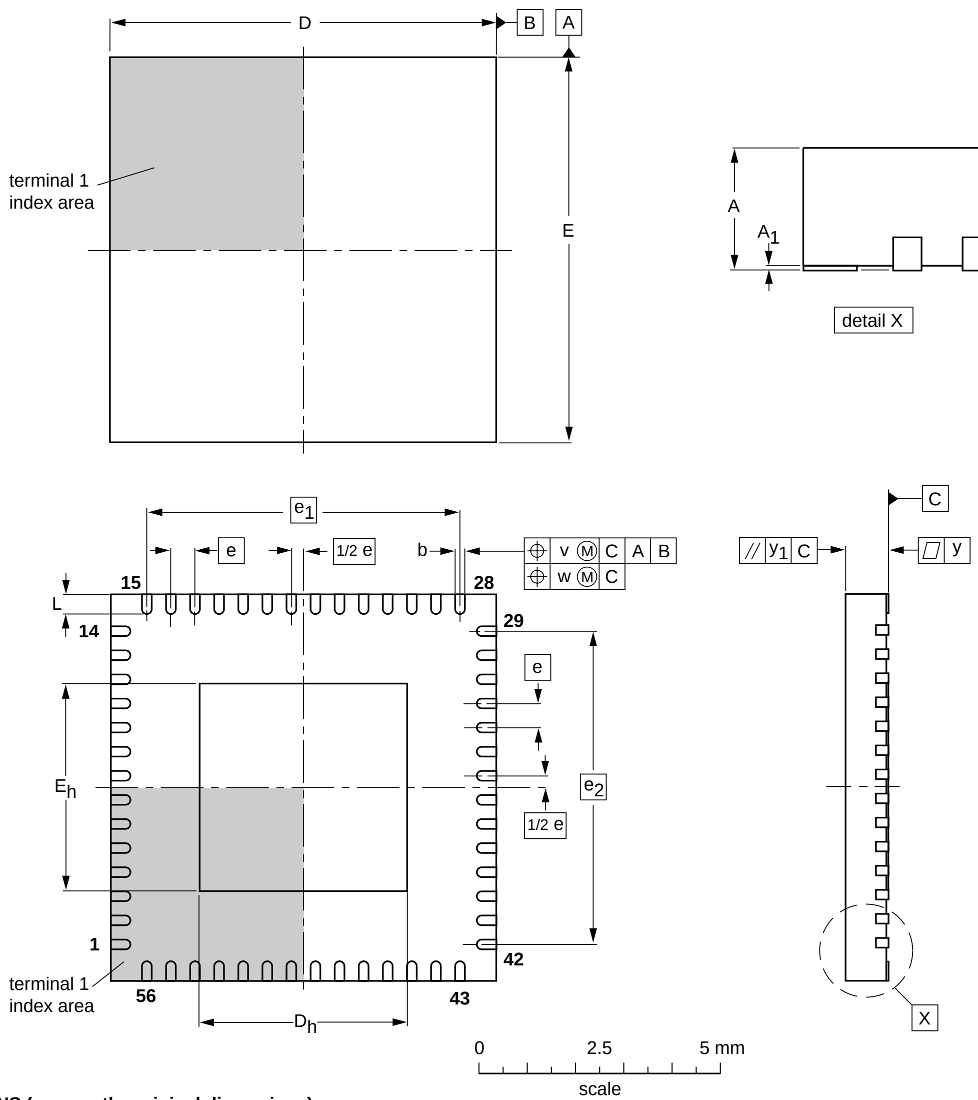
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 20. Package outline SOT364-1 (TSSOP56)

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm **SOT684-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	8.1 7.9	4.45 4.15	8.1 7.9	4.45 4.15	0.5	6.5	6.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT684-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 21. Package outline SOT684-1 (HVQFN56)

15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in *Data Handbook IC24 under "Handling MOS devices"*.

16. Soldering

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

16.5 Package related soldering information

Table 12: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	**Soldering method**	
	Wave	**Reflow** [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

17. Abbreviations

Table 13: Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
IC	Integrated Circuit
I^2C-bus	Inter IC bus
LED	Light Emitting Diode
MM	Machine Model
PLC	Programmable Logic Controller
POR	Power-On Reset
PWM	Pulse Width Modulation
RAID	Redundant Array of Independent Disks

18. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCA9506_1	20060214	Product data sheet	-	9397 750 14939	-

19. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

20. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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24. Contents

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