National Semiconductor

October 26, 2010

LM139JAN

Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM139 is a distinct advantage over standard comparators.

Features

- Wide supply voltage range 5V to 36 V_{DC} or ±2.5V to ±18 V_{DC}
- Very low supply current drain (0.8 mA) - independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Offset voltage: ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

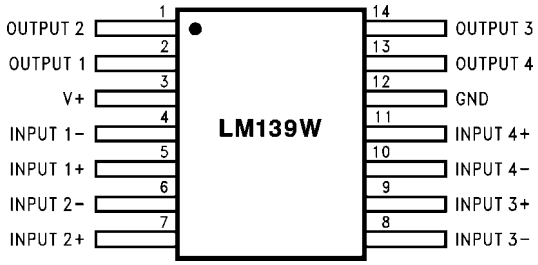
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Ordering Information

NS Part Number	JAN Part Number	NS Package Number	Package Description
JL139BDA	JM38510/11201BDA	W14B	14LD CERPACK

Connection Diagrams



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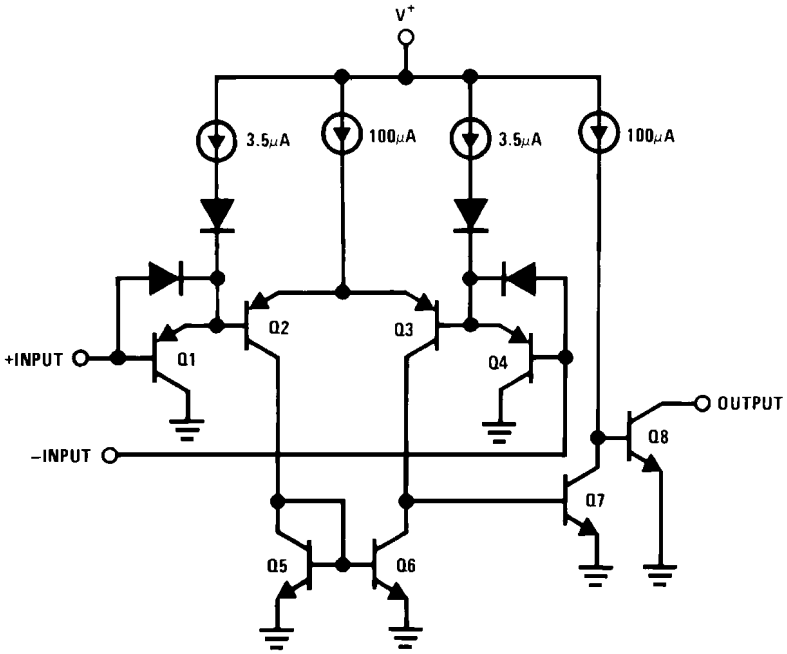
See NS Package Number W14B

Schematic Diagram



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Absolute Maximum Ratings (*Note 1*)

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage (*Note 7*)	36 V_{DC}
Output Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Input Current (V_{IN} < −0.3 V_{DC}) (*Note 3*)	50 mA
Power Dissipation (*Note 4*, *Note 12*)	
CERPACK	350 mW @ T_A = 125°C
Output Short-Circuit to GND, (*Note 2*)	Continuous
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Maximum Junction Temperature (T_J)	+175°C
Lead Temperature (Soldering, 10 seconds)	260°C
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C
Thermal Resistance	
θ_{JA}	
CERPACK (Still Air)	183°C/W
CERPACK (500LF / Min Air flow)	120°C/W
θ_{JC}	
CERPACK	23°C/W
Package Weight (typical)	
CERPACK	460mg
ESD rating (*Note 11*)	600V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LM139 JAN Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified. $-V_{CC} = 0V$

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 30V$, $V_O = 15V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $V_O = -13V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC} = 5V$, $V_O = 1.4V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC} = 2V$, $-V_{CC} = -3V$, $V_O = -1.6V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
I_{IO}	Input Offset Current	$+V_{CC} = 30V$, $R_S = 20K\Omega$, $V_O = 15V$	(*Note 8*)	-25	25	nA	1, 2
			(*Note 8*)	-75	75	nA	3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $R_S = 20K\Omega$, $V_O = -13V$	(*Note 8*)	-25	25	nA	1, 2
			(*Note 8*)	-75	75	nA	3
		$+V_{CC} = 5V$, $R_S = 20K\Omega$, $V_O = 1.4V$	(*Note 8*)	-25	25	nA	1, 2
			(*Note 8*)	-75	75	nA	3
		$+V_{CC} = 2V$, $-V_{CC} = -3V$, $R_S = 20K\Omega$, $V_O = -1.6V$	(*Note 8*)	-25	25	nA	1, 2
			(*Note 8*)	-75	75	nA	3
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 30V$, $R_S = 20K\Omega$, $V_O = 15V$	(*Note 8*)	-100	+0.1	nA	1, 2
			(*Note 8*)	-200	+0.1	nA	3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $R_S = 20K\Omega$, $V_O = -13V$	(*Note 8*)	-100	+0.1	nA	1, 2
			(*Note 8*)	-200	+0.1	nA	3
		$+V_{CC} = 5V$, $R_S = 20K\Omega$, $V_O = 1.4V$	(*Note 8*)	-100	+0.1	nA	1, 2
			(*Note 8*)	-200	+0.1	nA	3
		$+V_{CC} = 2V$, $-V_{CC} = -3V$, $R_S = 20K\Omega$, $V_O = -1.6V$	(*Note 8*)	-100	+0.1	nA	1, 2
			(*Note 8*)	-200	+0.1	nA	3
CMRR	Input Voltage Common Mode Rejection	$+V_{CC} = 30V$		76		dB	1, 2, 3
		$+V_{CC} = 5V$		70		dB	1, 2, 3
I_{CEX}	Output Leakage	$+V_{CC} = 30V$, $V_O = +30V$			1.0	µA	1, 2, 3
$+I_{IL}$	Input Leakage Current	$+V_{CC} = 36V$, $V + i = 34V$, $V - i = 0V$		-500	500	nA	1, 2, 3
$-I_{IL}$	Input Leakage Current	$+V_{CC} = 36V$, $V + i = 0V$, $V - i = 34V$		-500	500	nA	1, 2, 3
V_{OL}	Logical "0" Output Voltage	$+V_{CC} = 4.5V$, $I_O = 4mA$			0.4	V	1
					0.7	V	2, 3
		$+V_{CC} = 4.5V$, $I_O = 8mA$			1.5	V	1
					2.0	V	2, 3
I_{CC}	Power Supply Current	$+V_{CC} = 5V$, $V_{ID} = 15mV$			2.0	mA	1, 2
					3.0	mA	3
		$+V_{CC} = 30V$, $V_{ID} = 15mV$			3.0	mA	1, 2
					4.0	mA	3
$\Delta V_{IO}/\Delta T$	Temperature Coefficient of Input Offset Voltage	$25°C \le T_A \le 125°C$	(*Note 9*)	-25	25	µV/°C	2
		$-55°C \le T_A \le 25°C$	(*Note 9*)	-25	25	µV/°C	3
$\Delta I_{IO}/\Delta T$	Temperature Coefficient of Input Offset Current	$25°C \le T_A \le 125°C$	(*Note 9*)	-300	300	pA/°C	2
		$-55°C \le T_A \le 25°C$	(*Note 9*)	-400	400	pA/°C	3

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
A_{VS}	Open Loop Voltage Gain	$+V_{CC}$ = 15V, R_L=15KΩ,	(*Note 10*)	50		V/mV	4
		1V ≤ V_O ≤ 11V	(*Note 10*)	25		V/mV	5, 6
V_{IO}	Tempco Screen				4.0	mV	
CMRR	Tempco Screen				70	dB	
I_{IO}	Tempco Screen				13	nA	
I_{IB}	Tempco Screen				12	nA	

AC Parameters

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time: Low-to-High	$+V_{CC}$ = 5V, V_I = 100mV,			5.0	µS	7, 8B
		R_L = 5.1KΩ, V_{OD} = 5mV			7.0	µS	8A
		$+V_{CC}$ = 5V, V_I = 100mV,			0.8	µS	7, 8B
		R_L = 5.1KΩ, V_{OD} = 50mV			1.2	µS	8A
t_{RHL}	Response Time: High-to-Low	$+V_{CC}$ = 5V, V_I = 100mV,			2.5	µS	7, 8B
		R_L = 5.1KΩ, V_{OD} = 5mV			3.0	µS	8A
		$+V_{CC}$ = 5V, V_I = 100mV,			0.8	µS	7, 8B
		R_L = 5.1KΩ, V_{OD} = 50mV			1.0	µS	8A
C_S	Channel Separation	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, A to B		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, A to C		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, A to D		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, B to A		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, B to C		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, B to D		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, C to A		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, C to B		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, C to D		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, D to A		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, D to B		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, D to C		80		dB	7
V_{LAT}	Voltage Latch (Logical "1" Input)	$+V_{CC}$ = 5V, V_I = 10V, I_O = 4mA			0.4	V	9

DC Parameters Drift Values

The following conditions apply, unless otherwise specified. $-V_{CC}$ = 0V

Delta calculations performed on JAN S product at Group B, Subgroup 5.

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_{CC} = 30V,V_O = 15V		-1.0	1.0	mV	1
$\pm I_{Bias}$	Input Bias Current	V_{CC} = 30V,R_S = 20KΩ, V_O = 15V		-15	15	nA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guaranteed specific performance limits. For guaranteed specifications and test conditions, see, the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than –0.3 V_{DC} (at 25°)C.

Note 4: The low bias dissipation and the ON-OFF characteristics of the outputs keeps the chip dissipation very small ($P_D \leq$ 100mW), provided the output transistors are allowed to saturate.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20mA independent of the magnitude of V+

Note 7: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3 V_{DC} (or 0.3 V_{DC}below the magnitude of the negative power supply, if used) (at 25°C).

Note 8: S/S R_S = 20KΩ, tested at R_S = 10KΩ as equivalent test.

Note 9: Calculated parameter; for Delta V_{IO} / Delta T use V_{IO} test at $+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = 15V; and for Delta I_{IO} / Delta T use I_{IB} test at $+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = 15V

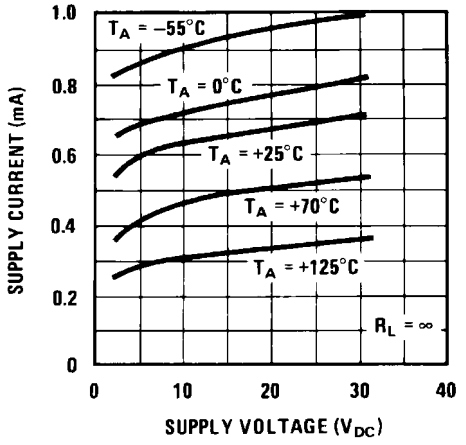
Note 10: Datalog of K = V/mV.

Note 11: Human Body model, 1.5 KΩ in series with 100 pF

Note 12: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (Package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} — T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Typical Performance Characteristics

Supply Current



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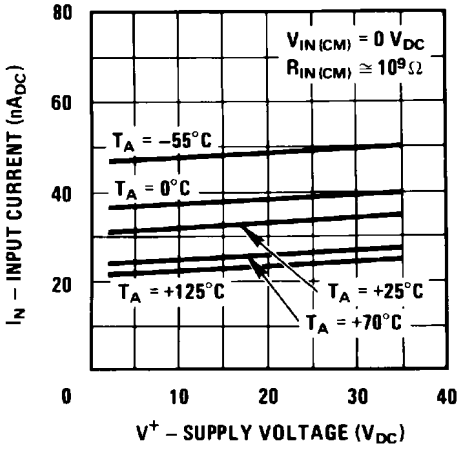
Input Current



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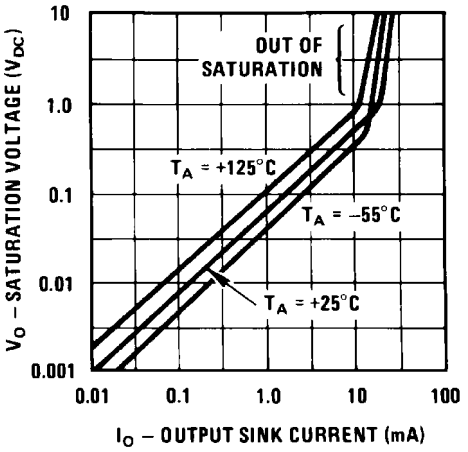
Output Saturation Voltage



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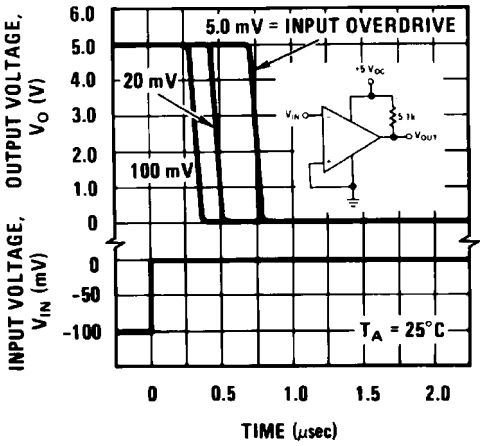
Response Time for Various Input Overdrives —Negative Transition



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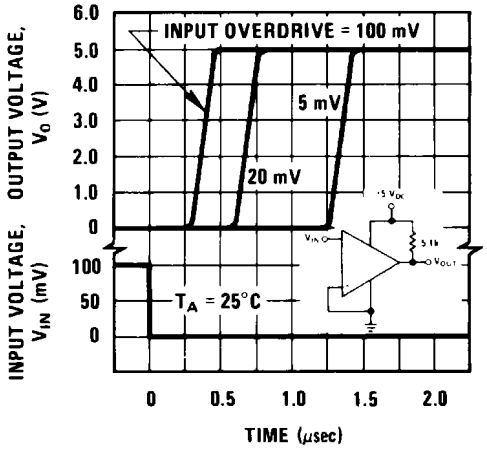
Response Time for Various Input Overdrives —Positive Transition



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Application Hints

The LM139 is a high gain, wide bandwidth device which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be tied to the negative supply.

The bias network of the LM139 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 5 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

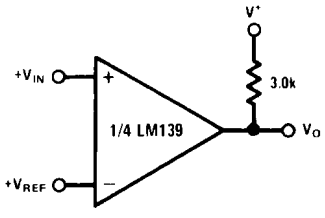
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than –0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications

(V^+ = 5.0 V_{DC})

Basic Comparator



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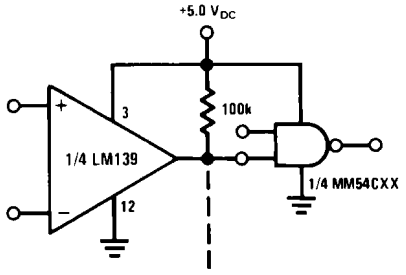
Driving CMOS



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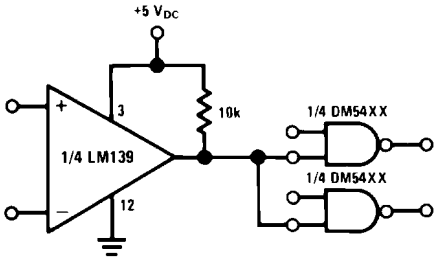
Driving TTL



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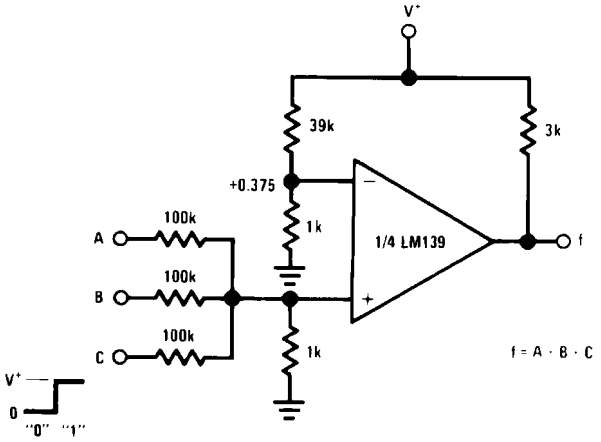
AND Gate



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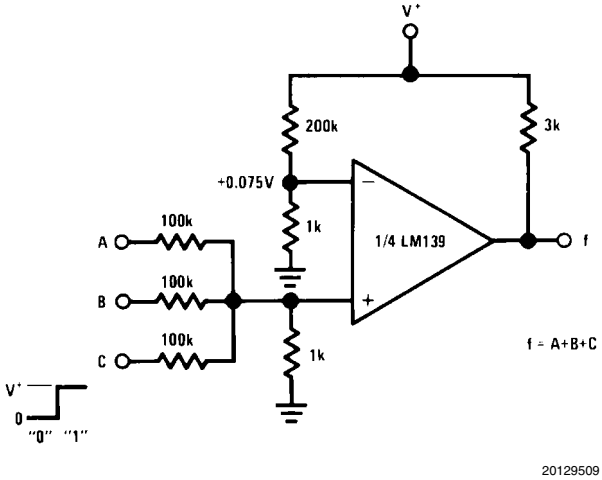
OR Gate



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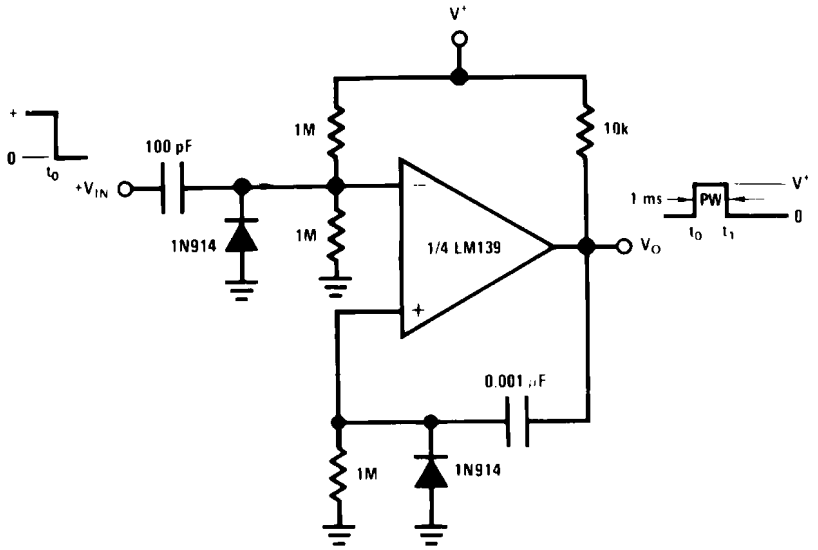
Typical Applications

(V^+= 15 V_{DC})

One-Shot Multivibrator



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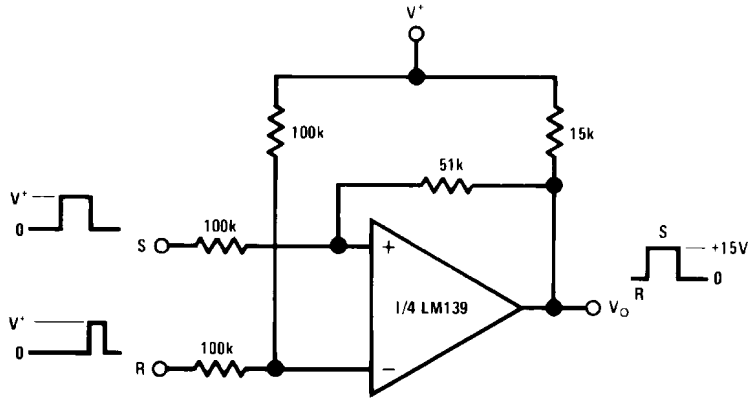
Bi-Stable Multivibrator



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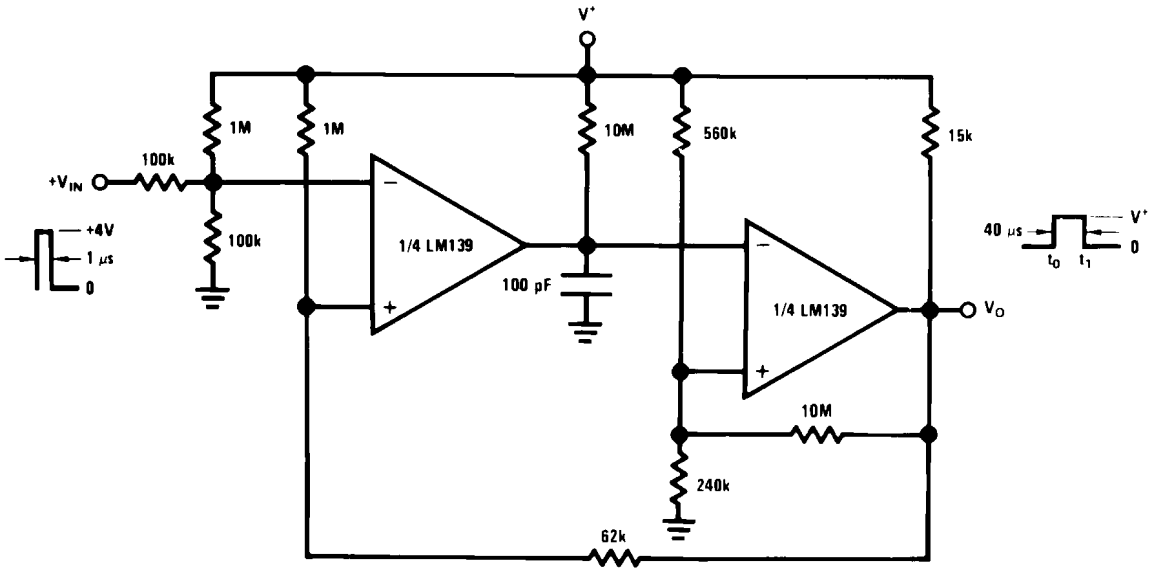
One-Shot Multivibrator with Input Lock Out



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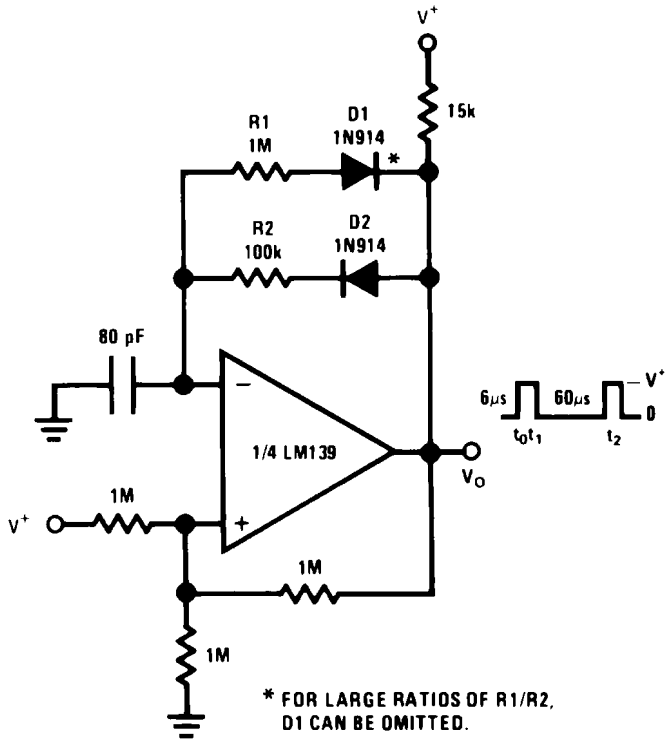
Pulse Generator



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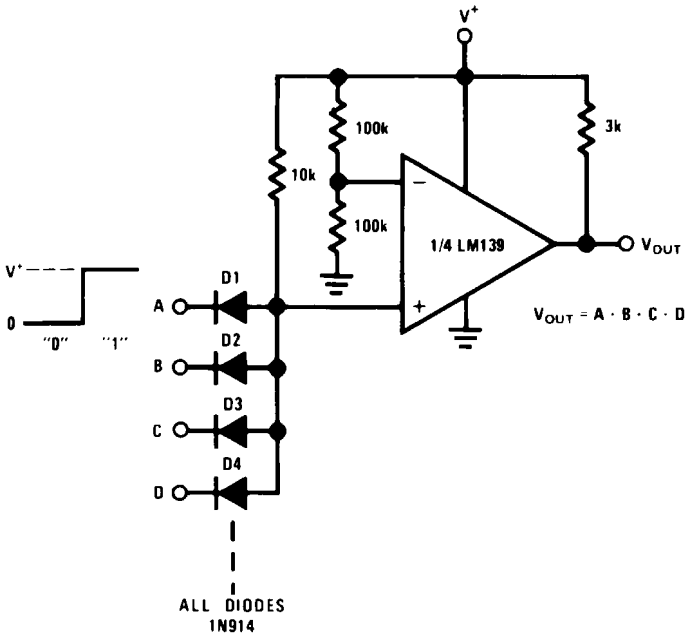
Large Fan-In AND Gate



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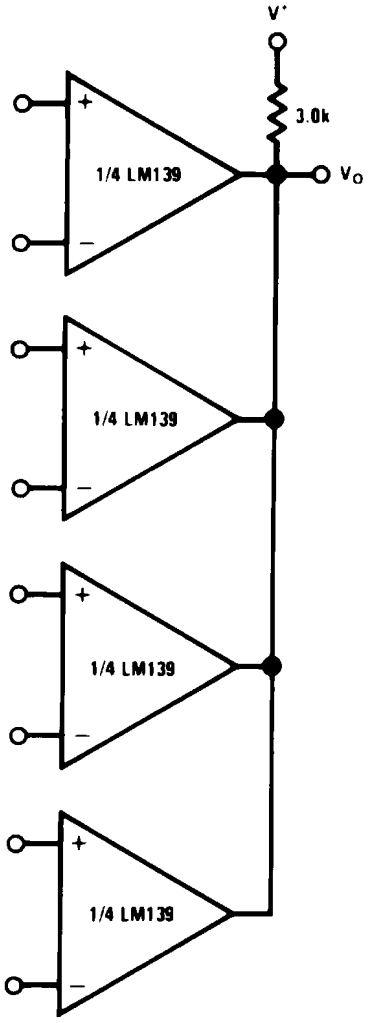
ORing the Outputs



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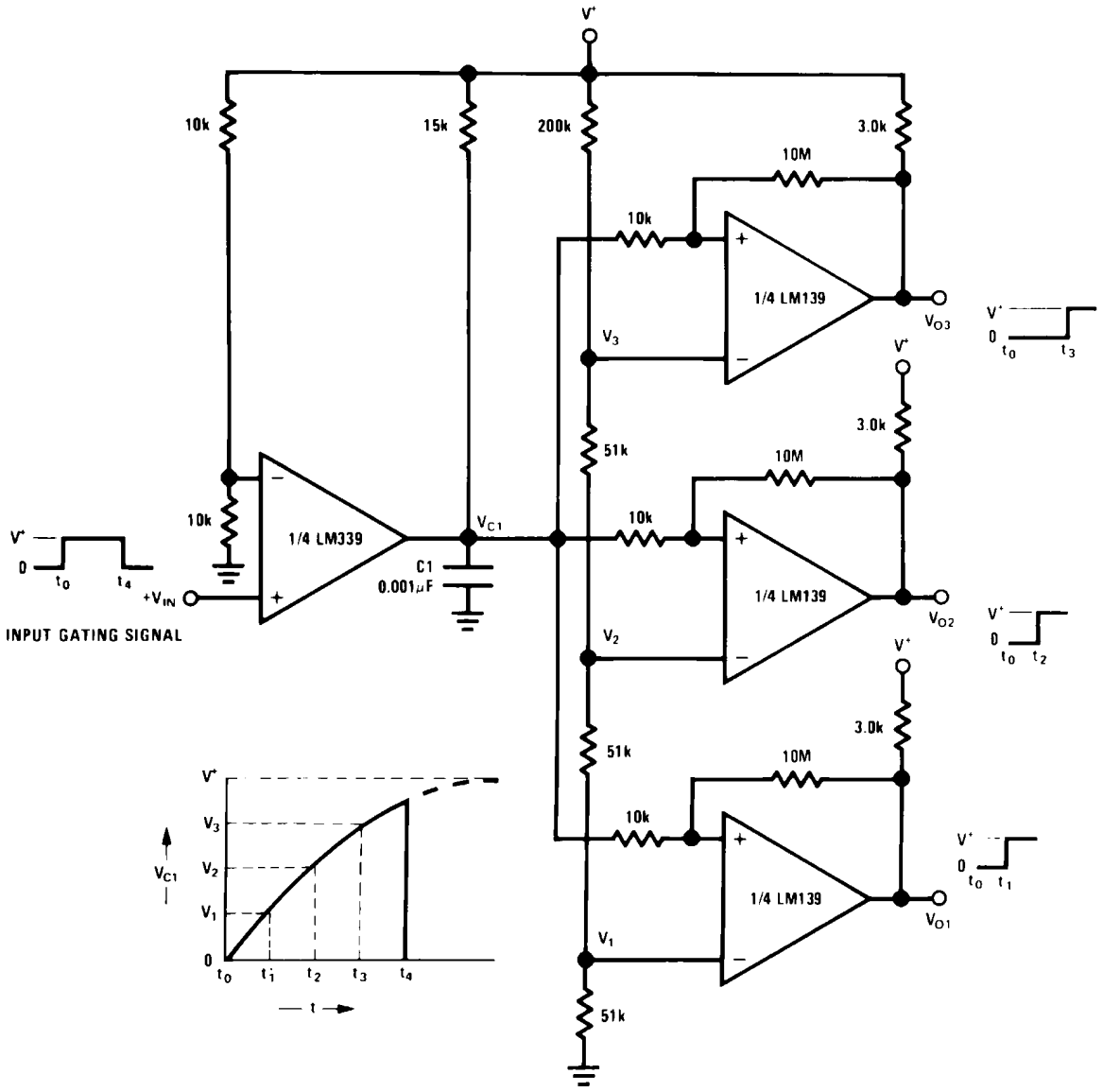
Time Delay Generator



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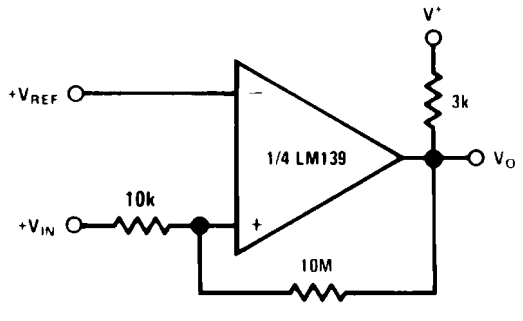
Non-Inverting Comparator with Hysteresis



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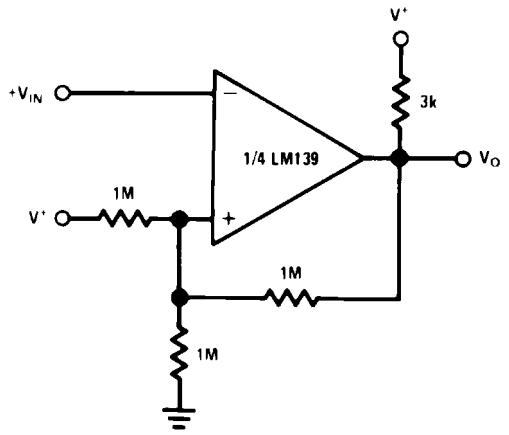
Inverting Comparator with Hysteresis



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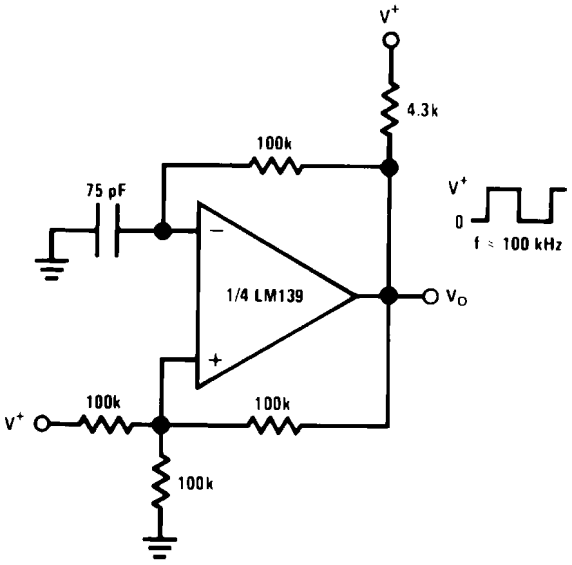
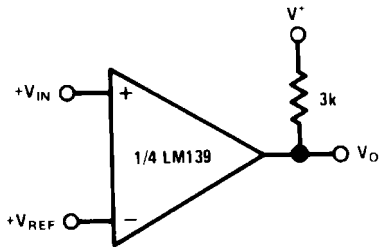
Squarewave Oscillator



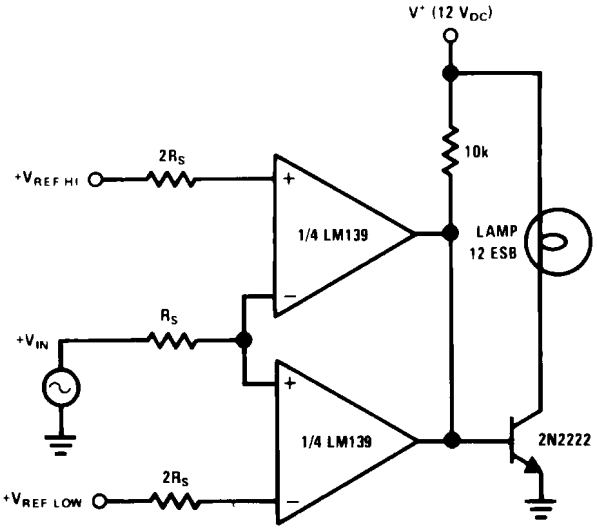
20129516

Basic Comparator



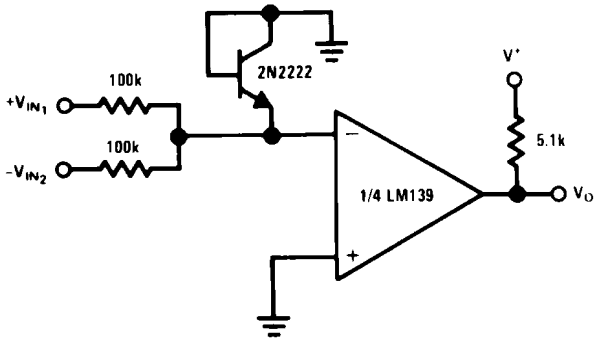
20129521

Limit Comparator



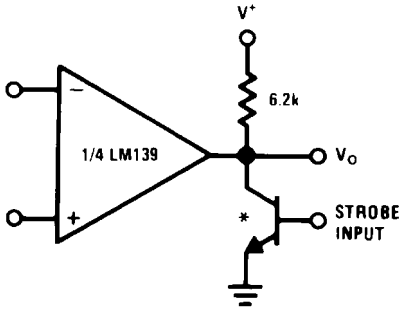
20129524

Comparing Input Voltages of Opposite Polarity



20129520

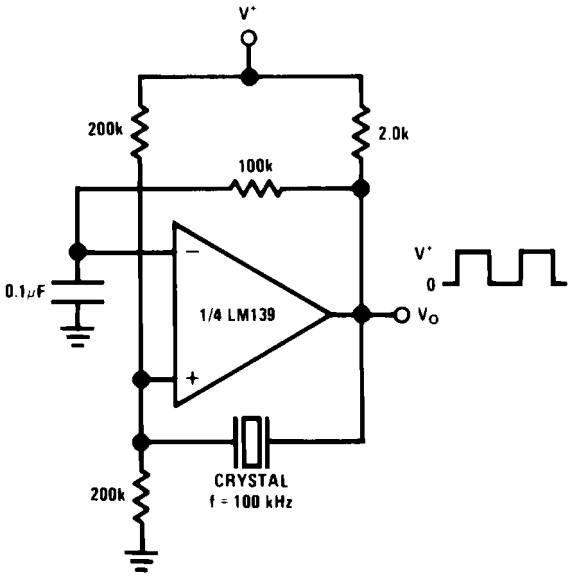
Output Strobing



20129522

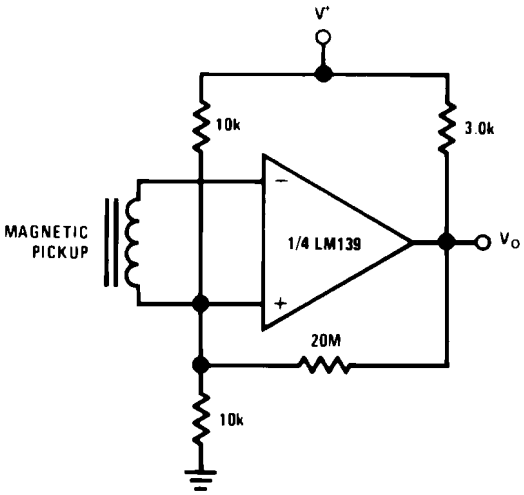
* Or open-collector logic gate without pull-up resistor

Crystal Controlled Oscillator



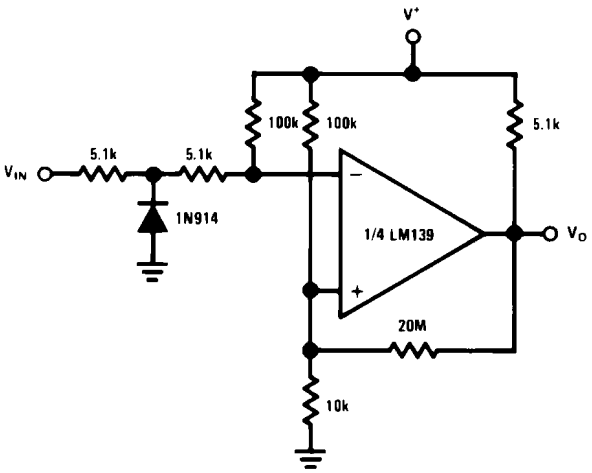
20129525

Transducer Amplifier



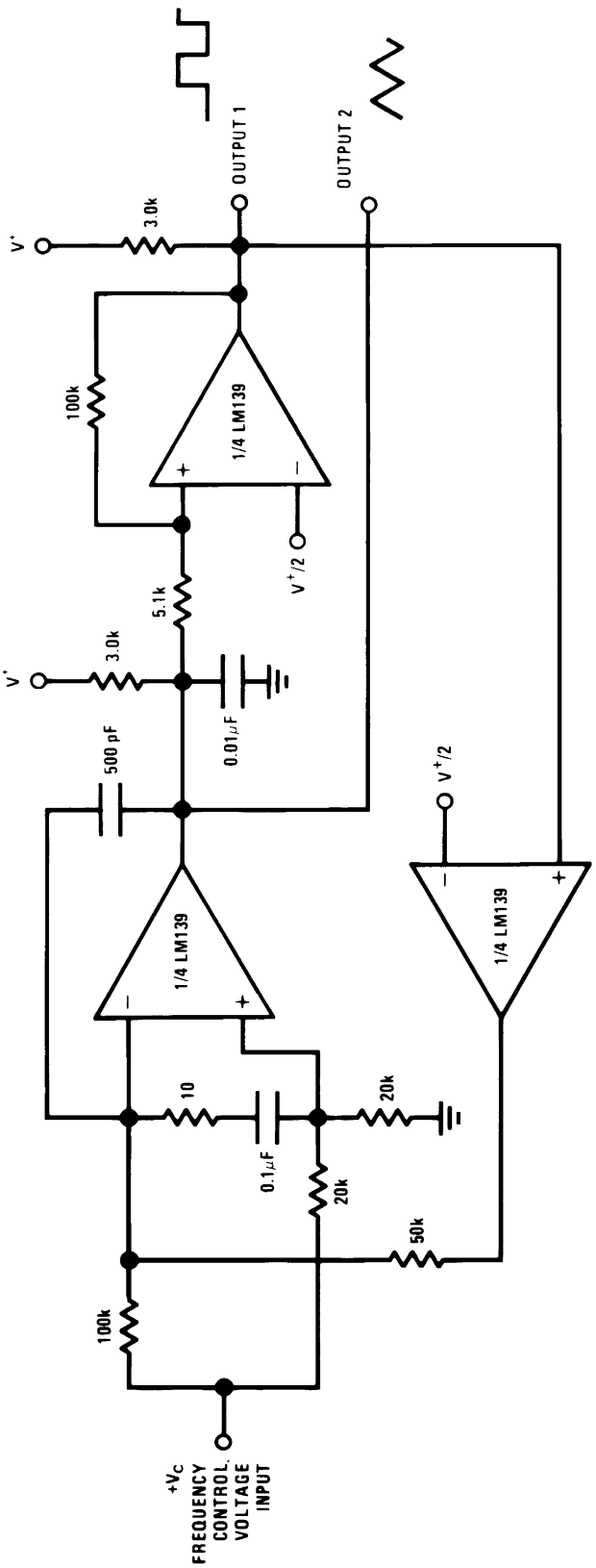
20129528

Zero Crossing Detector (Single Power Supply)



20129530

Two-Decade High-Frequency VCO



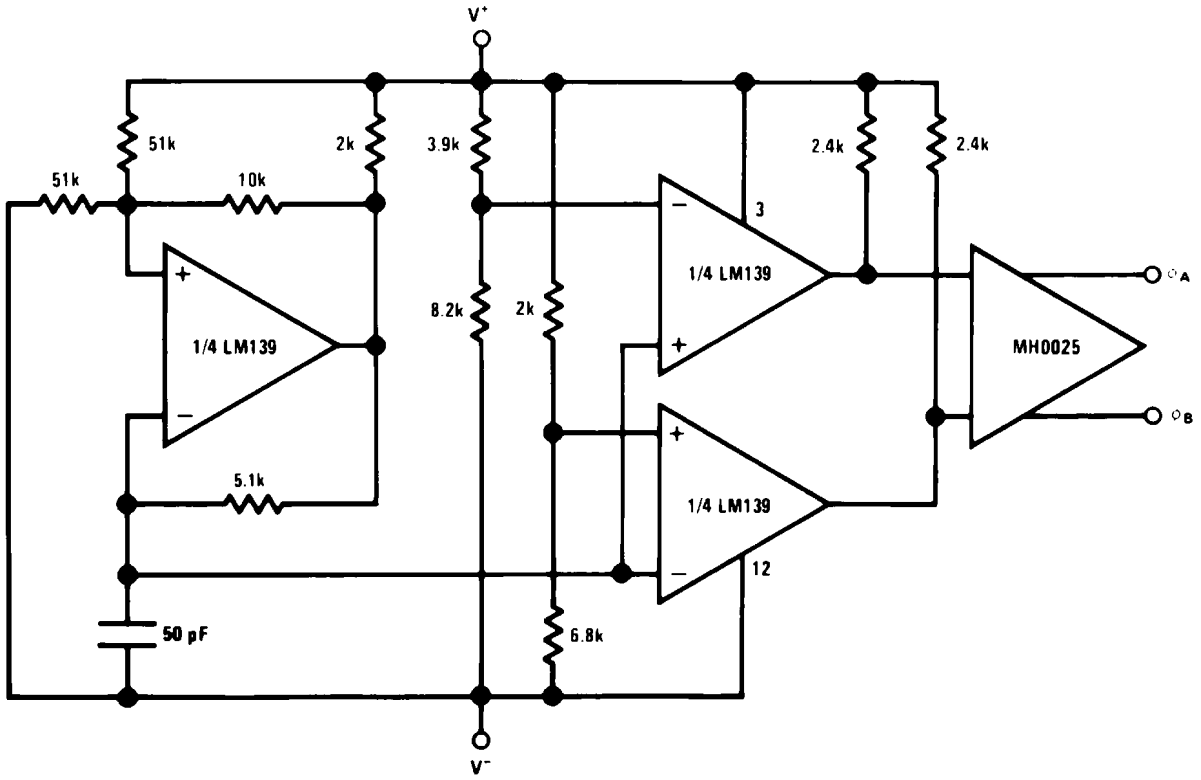
20129523

V+ = +30 V_{DC}
250 $mV_{DC} \leq V_C \leq +50\ V_{DC}$
700 Hz $\leq f_O \leq$ 100 kHz

Split-Supply Applications

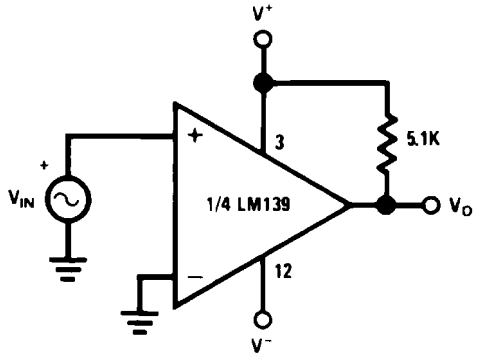
(V^+ = +15 V_{DC} and V^- = −15 V_{DC})

MOS Clock Driver



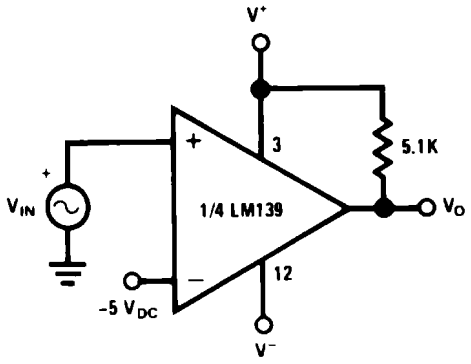
20129531

Zero Crossing Detector



20129532

Comparator With a Negative Reference

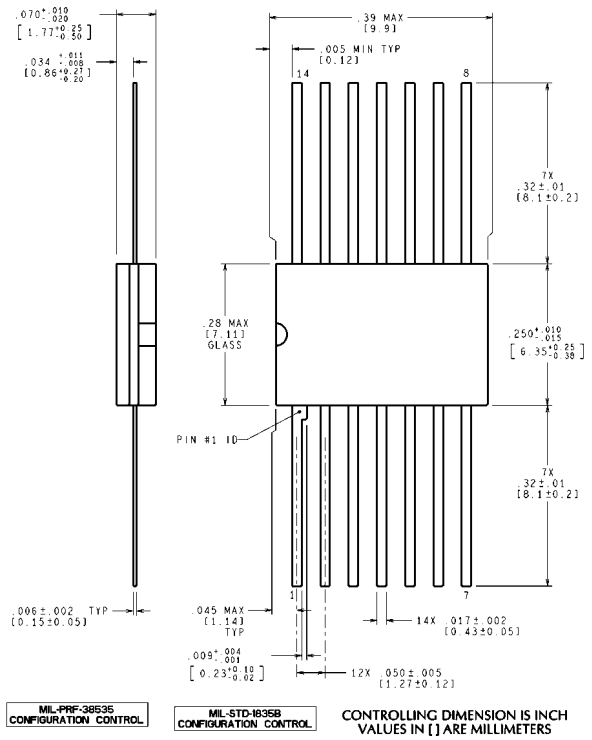


20129533

Revision History

Date Released	Revision	Section	Changes
02/15/05	A	New Release to corporate format	1 MDS datasheet converted into Corp. datasheet format. MJLM139-X rev 0D0. MDS datasheet will be archived.
10/26/2010	B	Order Information, Connection Diagrams, Absolute Ratings, Physical Dimensions drawings,	Update with current device information and format. Deleted J and WG pkg references. Revision A will be Archived

Physical Dimensions inches (millimeters) unless otherwise noted



W14B (Rev P)

Ceramic Flat Package (W)
NS Package Number W14B

Notes

Notes

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