National Semiconductor

October 21, 2010

LM7171QML

Very High Speed, High Output Current, Voltage Feedback Amplifier

General Description

The LM7171 is a high speed voltage feedback amplifier that has the slewing characteristic of a current feedback amplifier; yet it can be used in all traditional voltage feedback amplifier configurations. The LM7171 is stable for gains as low as +2 or −1. It provides a very high slew rate at 4100V/µs and a wide unity-gain bandwidth of 200 MHz while consuming only 6.5 mA of supply current. It is ideal for video and high speed signal processing applications such as HDSL and pulse amplifiers. With 100 mA output current, the LM7171 can be used for video distribution, as a transformer driver or as a laser diode driver.

Operation on ±15V power supplies allows for large signal swings and provides greater dynamic range and signal-to-noise ratio. The LM7171 offers low SFDR and THD, ideal for ADC/DAC systems. In addition, the LM7171 is specified for ±5V operation for portable applications.

The LM7171 is built on National's advanced VIP® III (Vertically integrated PNP) complementary bipolar process.

Features

(Typical Unless Otherwise Noted)

- Easy-To-Use Voltage Feedback Topology
- Very High Slew Rate: 2400V/µs
- Wide Unity-Gain Bandwidth: 200 MHz
- −3 dB Frequency @ A_V = +2: 220 MHz
- Low Supply Current: 6.5 mA
- High Open Loop Gain: 85 dB
- High Output Current: 100 mA
- Specified for ±15V and ±5V Operation
- Available with radiation guarantee
  - — Total Ionizing Dose 300 krad(Si)
  - — ELDRS Free 300 krad(Si)

Applications

- HDSL and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- Video Amplifiers
- Copiers/Scanners/Fax
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- CATV/Fiber Optics Signal Processing

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM7171AMJ-QML	5962-9553601QPA	J08A	8LD Ceramic Dip
LM7171AMJFQMLV **HIGH DOSE RATE** (*Note 5*)	5962F9553601VPA 300 krad(Si)	J08A	8LD Ceramic Dip
LM7171AMWFQMLV **HIGH DOSE RATE** (*Note 5*)	5962F9553601VHA 300 krad(Si)	W10A	10LD Ceramic Flatpack
LM7171AMWFLQMLV **ELDRS FREE** (*Note 14*)	5962F9553602VHA 300 krad(Si)	W10A	10LD Ceramic Flatpack
LM7171AMWG-QML	5962-9553601QXA	WG10A	10LD Ceramic SOIC
LM7171AMWGFQMLV **HIGH DOSE RATE** (*Note 5*)	5962F9553601VXA 300 krad(Si)	WG10A	10LD Ceramic SOIC
LM7171AMWGFLQV **ELDRS FREE** (*Note 14*)	5962F9553602VXA 300 krad(Si)	WG10A	10LD Ceramic SOIC

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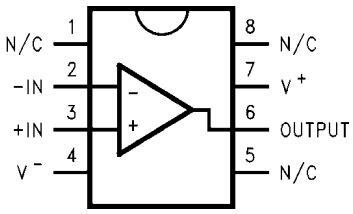
Connection Diagrams

8-Pin Ceramic DIP



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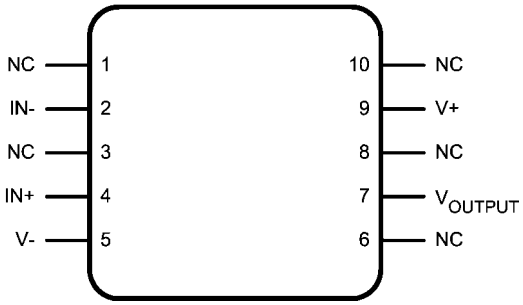
Top View

10-Pin Ceramic SOIC & Ceramic Flatpack



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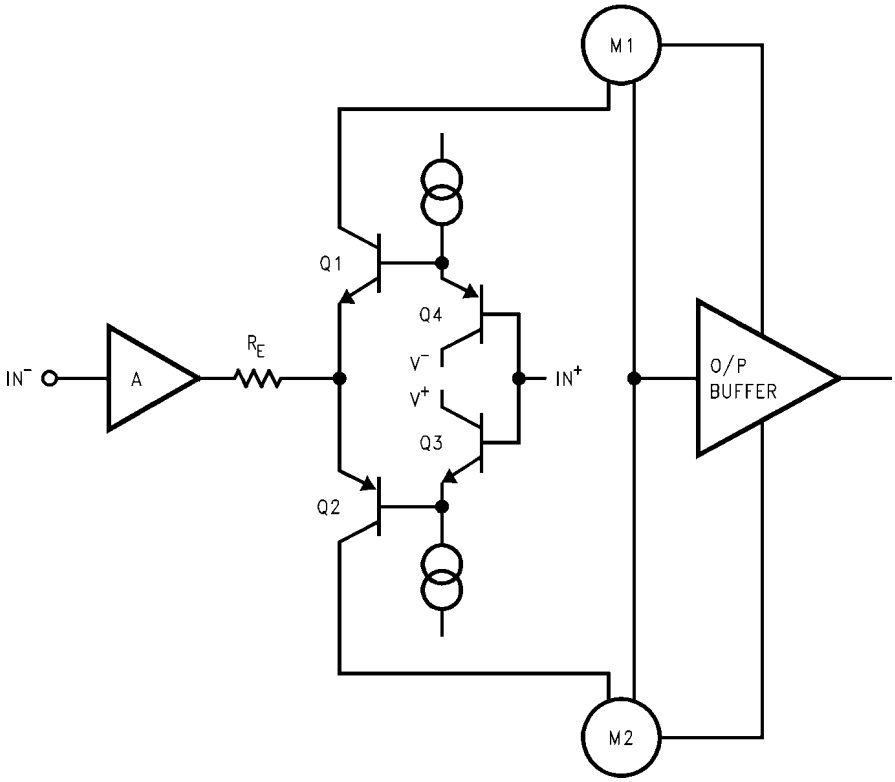
Top View

Simplified Schematic Diagram



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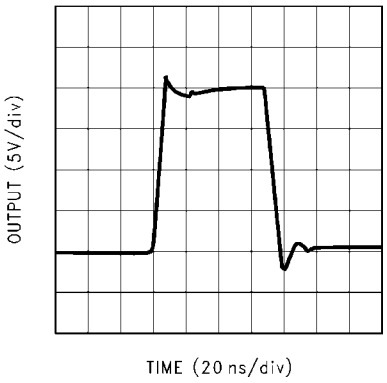
Note: M1 and M2 are current mirrors.

Typical Performance

Large Signal Pulse Response
A_V = +2, V_S = ±15V



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Absolute Maximum Ratings (*Note 1*)

Supply Voltage (V^+–V^-)	36V
Differential Input Voltage (*Note 10*)	±10V
Maximum Power Dissipation (*Note 2*)	730mW
Output Short Circuit to Ground (*Note 6*)	Continuous
Storage Temperature Range	$-65°C \le T_A \le +150°C$
Thermal Resistance (*Note 13*)	
θ_{JA}	
8LD Ceramic Dip (Still Air)	106°C/W
8LD Ceramic Dip (500LF/Min Air flow)	53°C/W
10LD Ceramic Flatpack (Still Air)	182°C/W
10LD Ceramic Flatpack (500LF/Min Air flow)	105°C/W
10LD Ceramic SOIC (Still Air)	182°C/W
10LD Ceramic SOIC (500LF/Min Air flow)	105°C/W
θ_{JC}	
8LD Ceramic Dip	3°C/W
10LD Ceramic Flatpack	5°C/W
10LD Ceramic SOIC (*Note 3*)	5°C/W
Package Weight (Typical)	
8LD Ceramic Dip	965mg
10LD Ceramic Flatpack	235mg
10LD Ceramic SOIC	230mg
Maximum Junction Temperature (*Note 2*)	150°C
ESD Tolerance (*Note 4*)	3000V

Recommended Operating Conditions (*Note 1*)

Supply Voltage	$5.5V \le V_S \le 36V$
Operating Temperature Range	$-55°C \le T_A \le +125°C$

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM7171 (±15) Electrical Characteristics

DC Parameters (*Note 5*)

The following conditions apply, unless otherwise specified.

DC: T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L > 1MΩ

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			−1.0	1.0	mV	1
				−7.0	7.0	mV	2, 3
$+I_{IB}$	Input Bias Current				10	µA	1
					12	µA	2, 3
$-I_{IB}$	Input Bias Current				10	µA	1
					12	µA	2, 3
I_{IO}	Input Offset Current			−4.0	4.0	µA	1
				−6.0	6.0	µA	2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V		85		dB	1
				70		dB	2, 3
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V		85		dB	1
				80		dB	2, 3
A_V	Large Signal Voltage Gain	R_L = 1KΩ, V_O = ±5V	(*Note 7*)	80		dB	1
			(*Note 7*)	75		dB	2, 3
		R_L = 100Ω, V_O = ±5V	(*Note 7*)	75		dB	1
			(*Note 7*)	70		dB	2, 3
V_O	Output Swing	R_L = 1KΩ		13	-13	V	1
				12.7	-12.7	V	2, 3
		R_L = 100Ω		10.5	-9.5	V	1
				9.5	-9.0	V	2, 3
	Output Current (Open Loop)	Sourcing	(*Note 8*)	105		mA	1
		R_L = 100Ω	(*Note 8*)	95		mA	2, 3
		Sinking	(*Note 8*)		-95	mA	1
		R_L = 100Ω	(*Note 8*)		-90	mA	2, 3
I_S	Supply Current				8.5	mA	1
					9.5	mA	2, 3

AC Parameters (*Note 5*)

The following conditions apply, unless otherwise specified.

AC: T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L > 1MΩ

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
SR	Slew Rate	A_V = 2, V_I = ±2.5V 3nS Rise & Fall time	(*Note 11*), (*Note 9*)	2000		V/µS	4
GBW	Unity-Gain Bandwidth		(*Note 12*)	170		MHz	4

DC Drift Parameters (*Note 5*)

The following conditions apply, unless otherwise specified.

DC: T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L > 1MΩ

Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			-250	250	µV	1
$+I_{Bias}$	Input Bias Current			-500	500	nA	1
$-I_{Bias}$	Input Bias Current			-500	500	nA	1

LM7171 (±5) Electrical Characteristics

DC Parameters (*Note 5*)

The following conditions apply, unless otherwise specified.

DC: T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L > 1MΩ

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			−1.5	1.5	mV	1
				−7.0	7.0	mV	2, 3
$+I_{IB}$	Input Bias Current				10	µA	1
					12	µA	2, 3
$-I_{IB}$	Input Bias Current				10	µA	1
					12	µA	2, 3
I_{IO}	Input Offset Current			−4.0	4.0	µA	1
				−6.0	6.0	µA	2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V		80		dB	1
				70		dB	2, 3
A_V	Large Signal Voltage Gain	R_L = 1KΩ, V_O = ±1V	(*Note 7*)	75		dB	1
			(*Note 7*)	70		dB	2, 3
		R_L = 100Ω, V_O = ±1V	(*Note 7*)	72		dB	1
			(*Note 7*)	67		dB	2, 3
V_O	Output Swing	R_L = 1KΩ		3.2	-3.2	V	1
				3.0	-3.0	V	2, 3
		R_L = 100Ω		2.9	-2.9	V	1
				2.8	-2.75	V	2, 3
	Output Current (Open Loop)	Sourcing	(*Note 8*)	29		mA	1
		R_L = 100Ω	(*Note 8*)	28		mA	2, 3
		Sinking	(*Note 8*)		-29	mA	1
		R_L = 100Ω	(*Note 8*)		-27.5	mA	2, 3
I_S	Supply Current				8.0	mA	1
					9.0	mA	2, 3

DC Drift Parameters (*Note 5*)

The following conditions apply, unless otherwise specified.

DC: T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L > 1MΩ

Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			-250	250	µV	1
$+I_{Bias}$	Input Bias Current			-500	500	nA	1
$-I_{Bias}$	Input Bias Current			-500	500	nA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using θ_{JA}, rather than θ_{JC}, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated θ_{JC} thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.

Note 6: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 7: Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For $V_S = \pm15V$, $V_{OUT} = \pm5V$. For $V_S = \pm5V$, $V_{OUT} = \pm1V$.

Note 8: The open loop output current is guaranteed, by the measurement of the open loop output voltage swing, using 100Ω output load.

Note 9: Slew Rate measured between ±4V.

Note 10: Differential input voltage is applied at $V_S = \pm15V$.

Note 11: See AN00001 for SR test circuit.

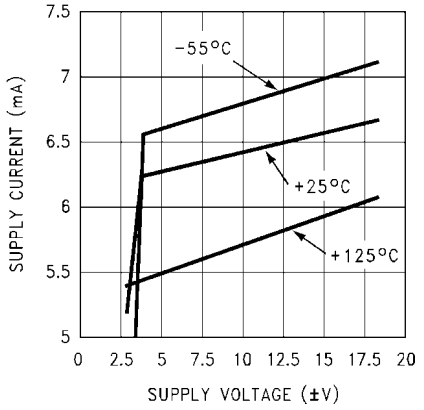
Note 12: See AN00002 for GBW test circuit.

Note 13: All numbers apply for packages soldered directly into a PC board.

Note 14: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. Low dose rate testing has been peformed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

Typical Performance Characteristics unless otherwise noted, T_A= 25°C

Supply Current vs Supply Voltage



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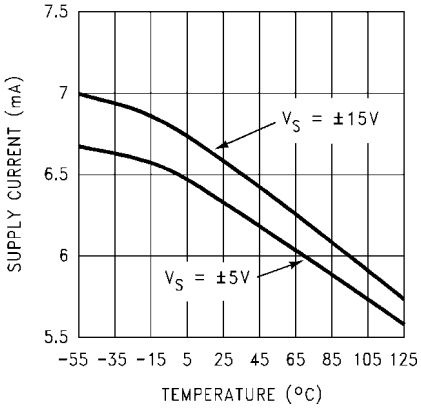
Supply Current vs Temperature



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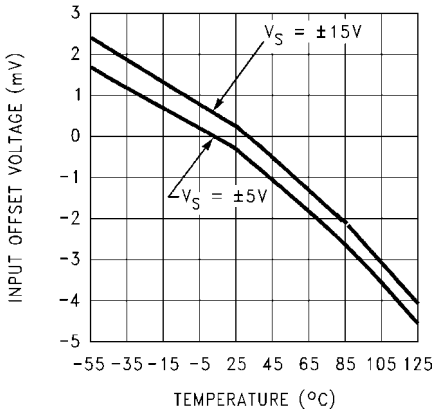
Input Offset Voltage vs Temperature



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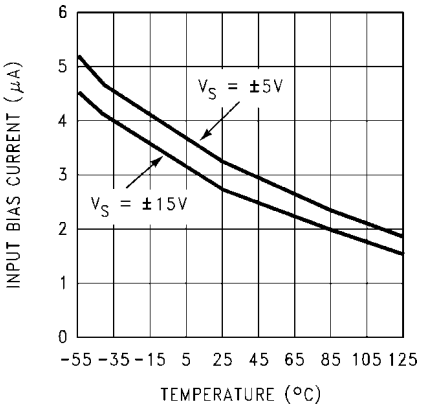
Input Bias Current vs Temperature



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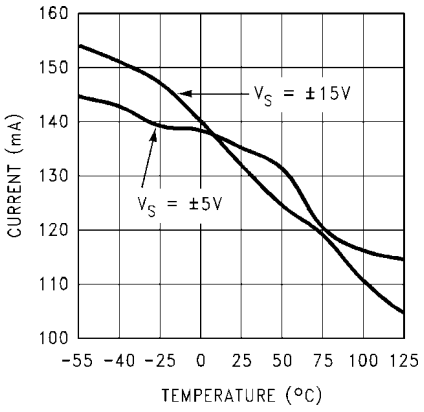
Short Circuit Current vs Temperature (Sourcing)



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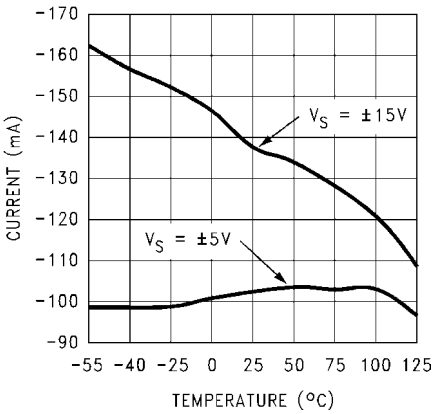
Short Circuit Current vs Temperature (Sinking)



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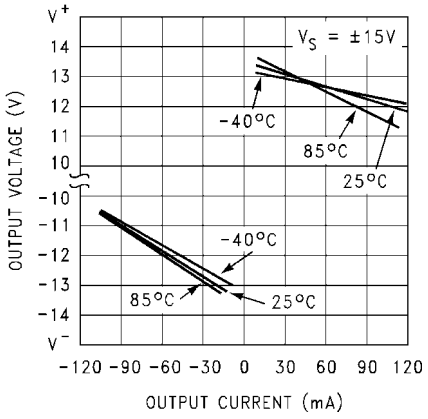
Output Voltage vs Output Current



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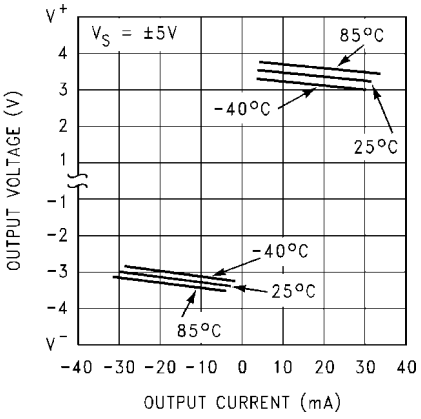
Output Voltage vs Output Current



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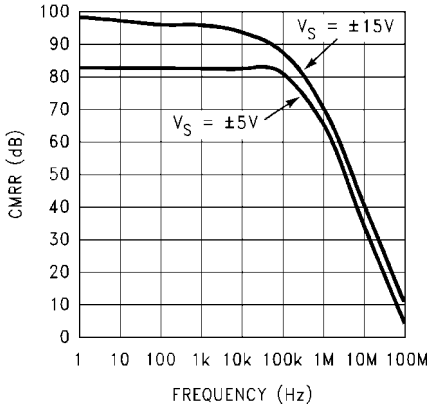
CMRR vs Frequency



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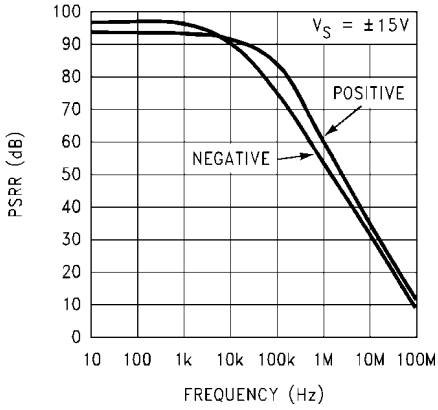
PSRR vs Frequency



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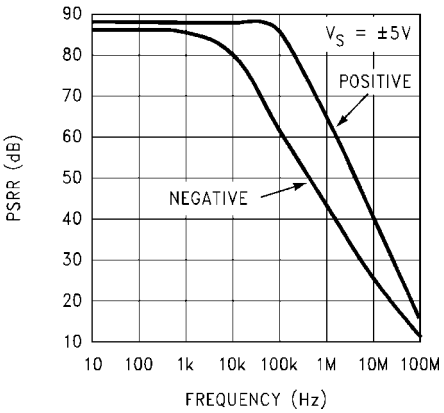
PSRR vs Frequency



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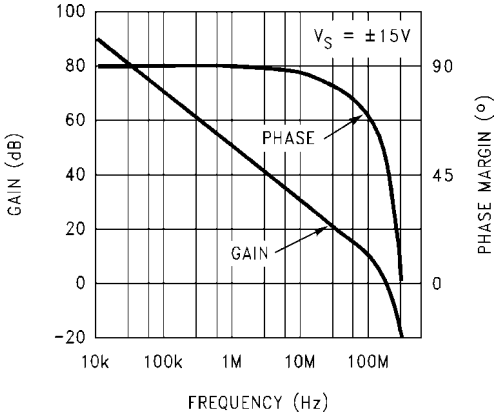
Open Loop Frequency Response



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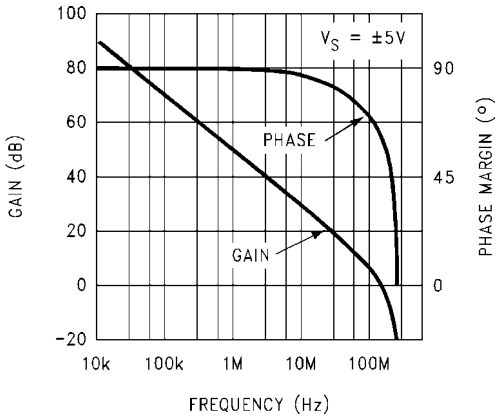
Open Loop Frequency Response



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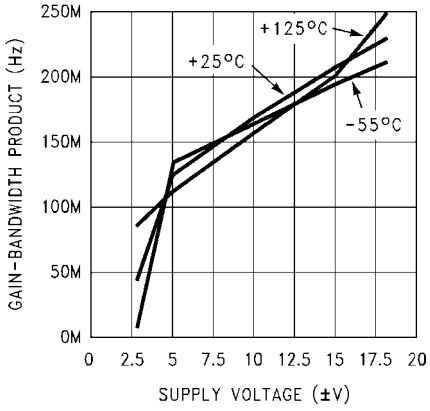
Gain-Bandwidth Product vs Supply Voltage



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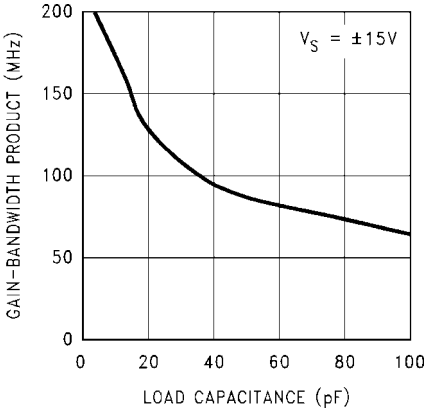
Gain-Bandwidth Product vs Load Capacitance



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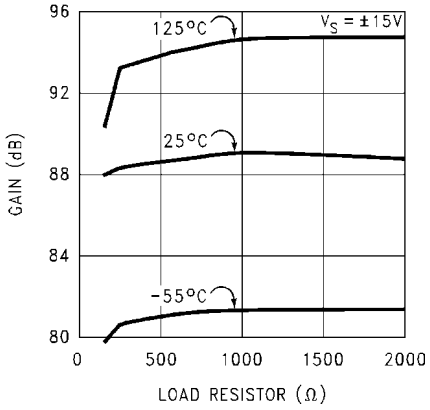
Large Signal Voltage Gain vs Load



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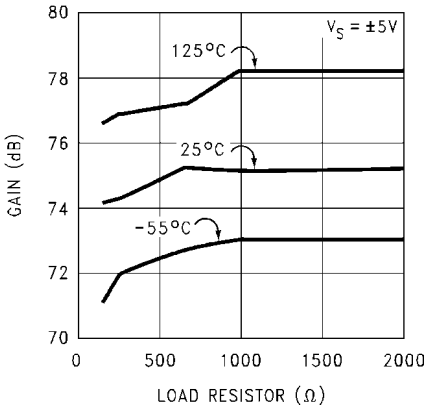
Large Signal Voltage Gain vs Load



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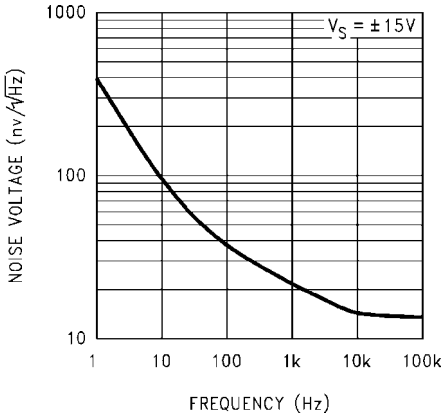
Input Voltage Noise vs Frequency



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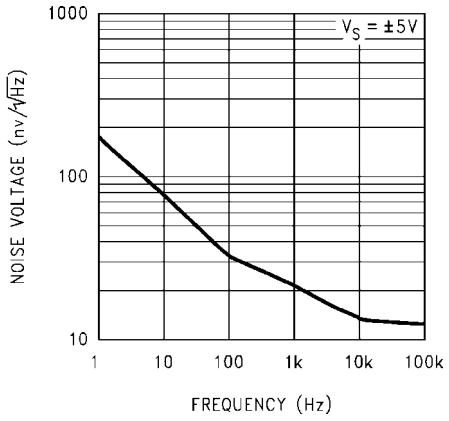
Input Voltage Noise vs Frequency



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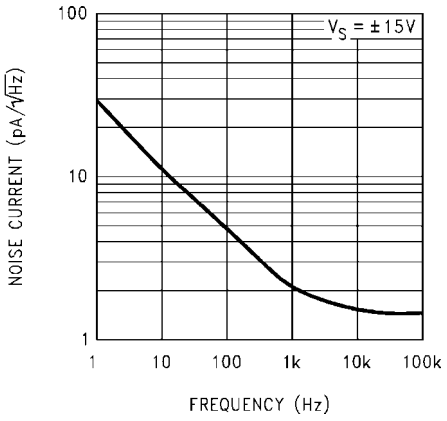
Input Current Noise vs Frequency



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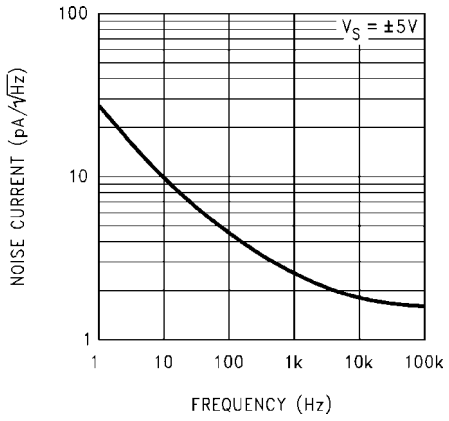
Input Current Noise vs Frequency



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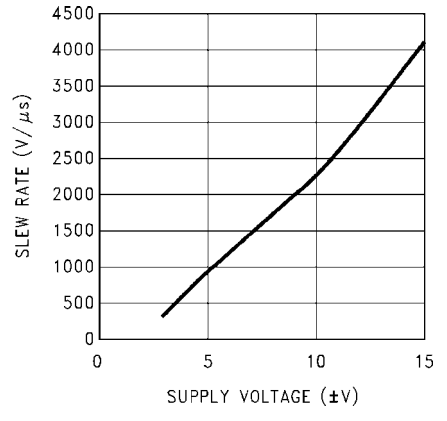
Slew Rate vs Supply Voltage



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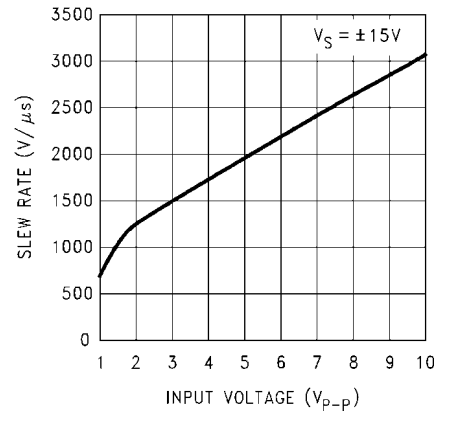
Slew Rate vs Input Voltage



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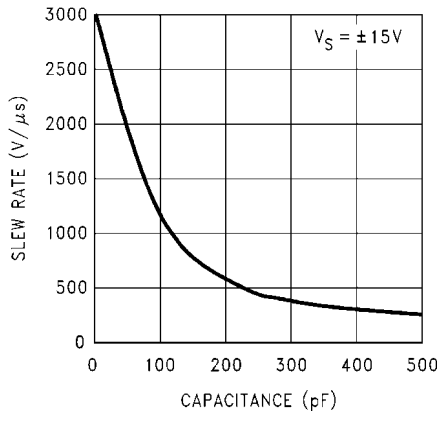
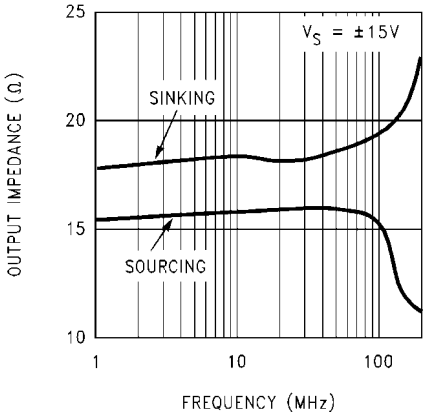
Slew Rate vs Load Capacitance



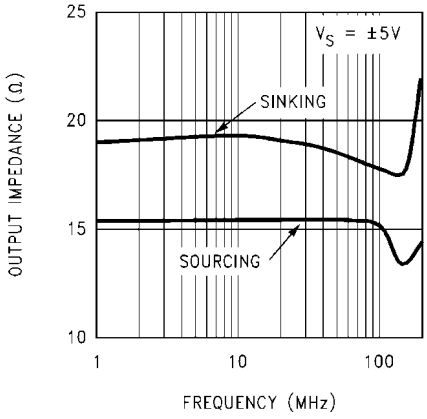
20159523

Open Loop Output Impedance vs Frequency



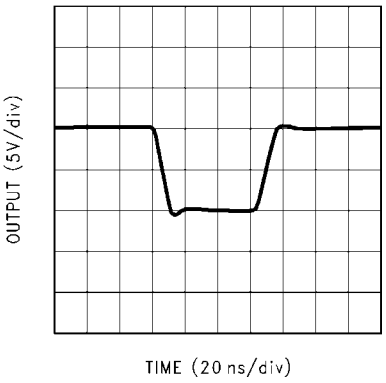
20159525

Open Loop Output Impedance vs Frequency



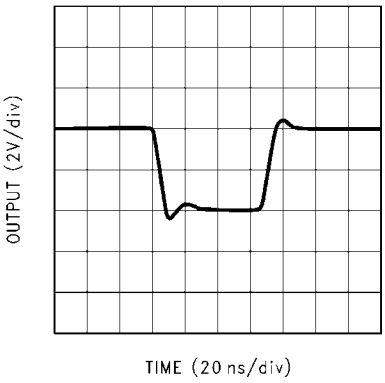
20159526

Large Signal Pulse Response A_V = –1, V_S = ±15V



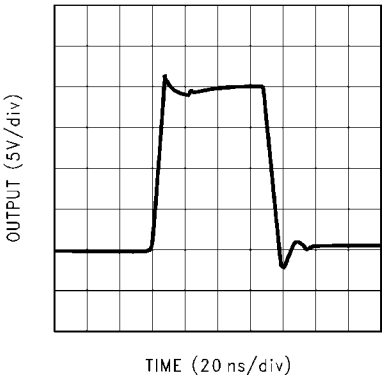
20159527

Large Signal Pulse Response A_V = –1, V_S = ±5V



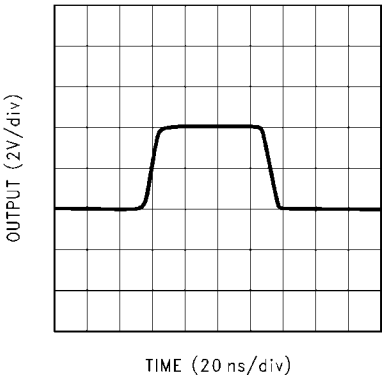
20159528

Large Signal Pulse Response A_V = +2, V_S = ±15V



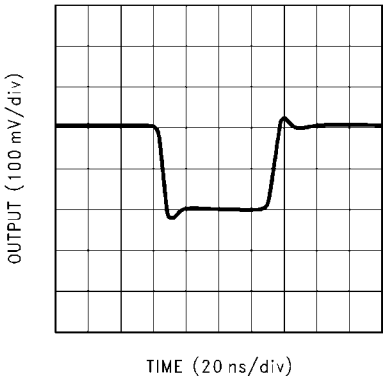
20159529

Large Signal Pulse Response A_V = +2, V_S = ±5V



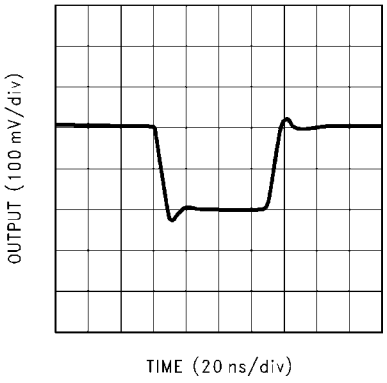
20159530

Small Signal Pulse Response $A_V = -1$, $V_S = \pm 15V$



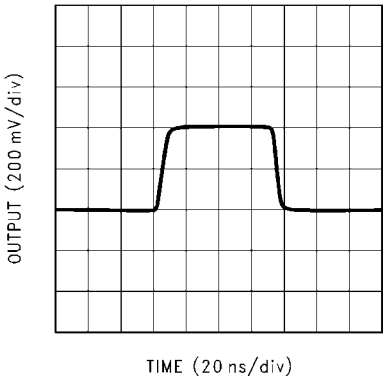
20159531

Small Signal Pulse Response $A_V = -1$, $V_S = \pm 5V$



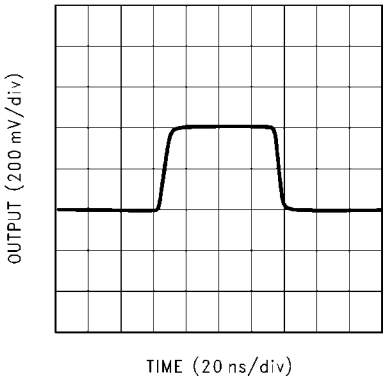
20159532

Small Signal Pulse Response $A_V = +2$, $V_S = \pm 15V$



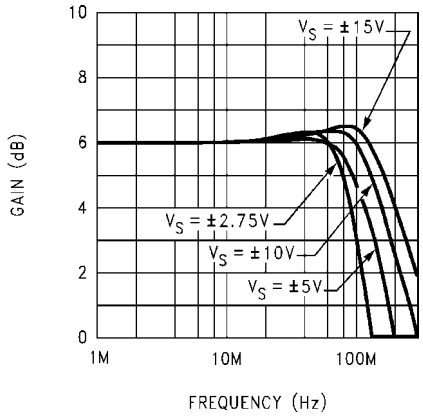
20159533

Small Signal Pulse Response $A_V = +2$, $V_S = \pm 5V$



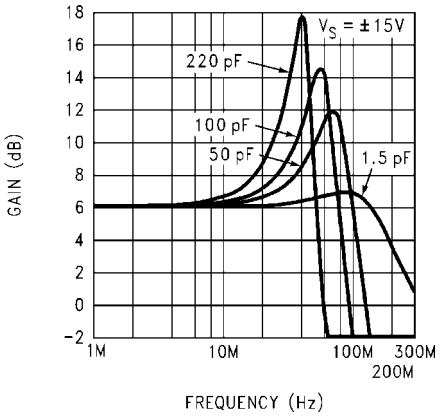
20159534

Closed Loop Frequency Response vs Supply Voltage ($A_V = +2$)



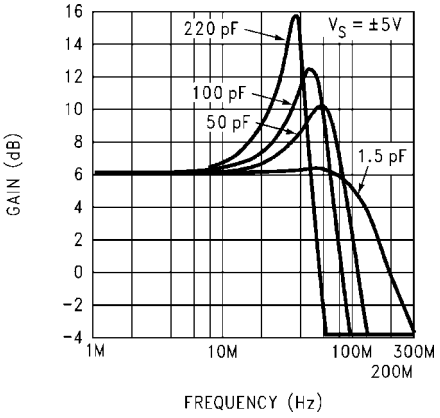
20159535

Closed Loop Frequency Response vs Capacitive Load ($A_V = +2$)



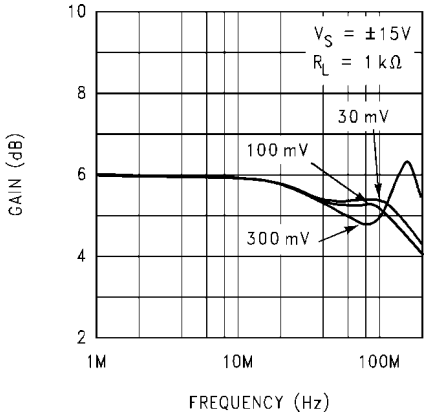
20159536

Closed Loop Frequency Response vs Capacitive Load (A_V = +2)



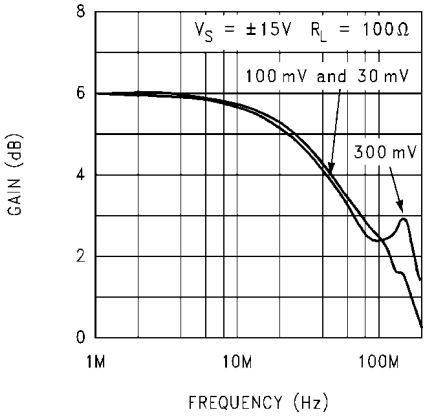
20159537

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)



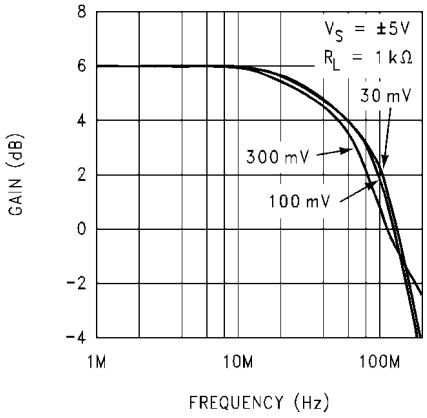
20159538

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)



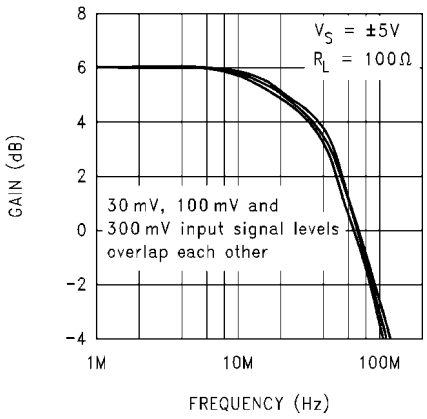
20159543

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)



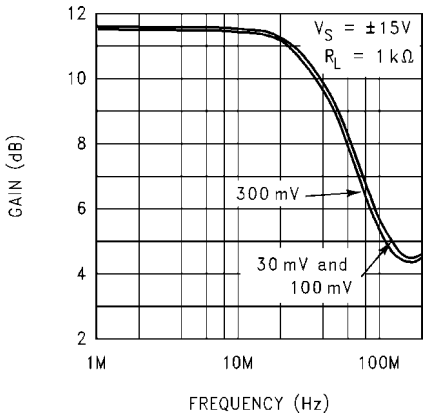
20159539

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)



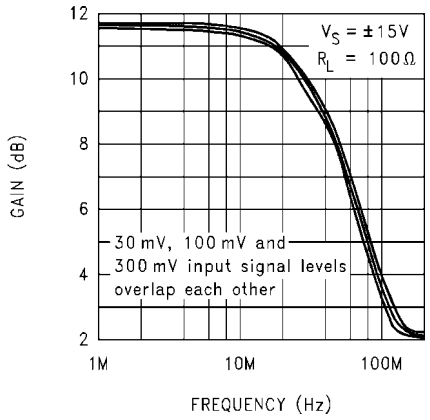
20159540

Closed Loop Frequency Response vs Input Signal Level (A_V = +4)



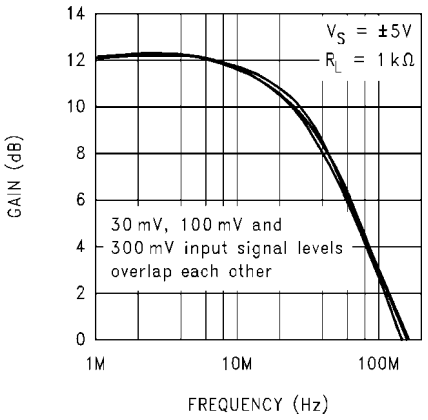
20159544

Closed Loop Frequency Response vs Input Signal Level (A_V = +4)



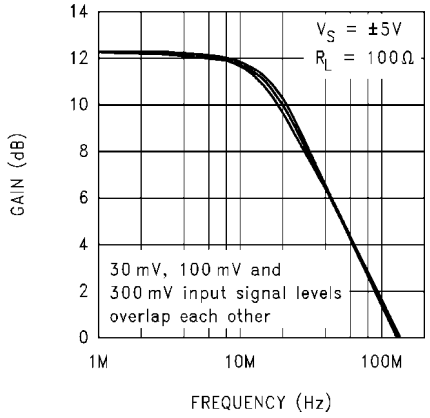
20159545

Closed Loop Frequency Response vs Input Signal Level (A_V = +4)



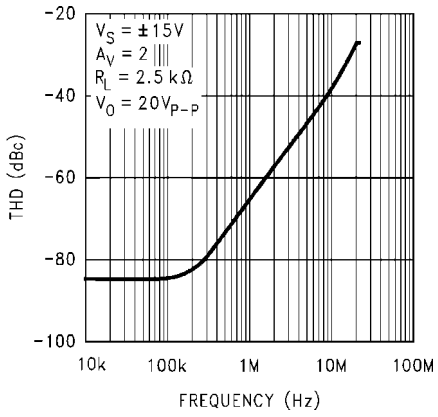
20159541

Closed Loop Frequency Response vs Input Signal Level (A_V = +4)



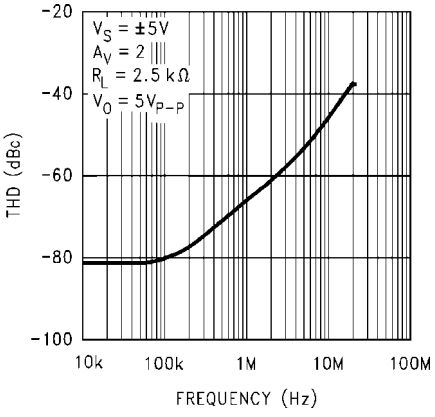
20159542

Total Harmonic Distortion vs Frequency (*Note 15*)



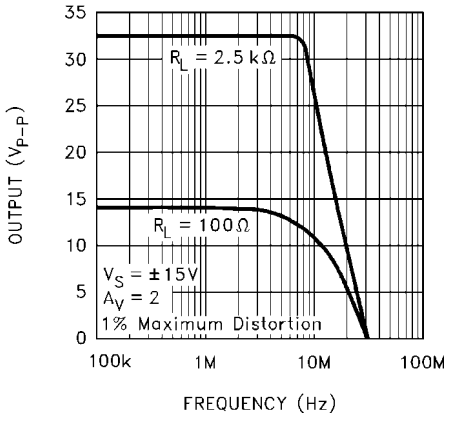
20159546

Total Harmonic Distortion vs Frequency (*Note 15*)



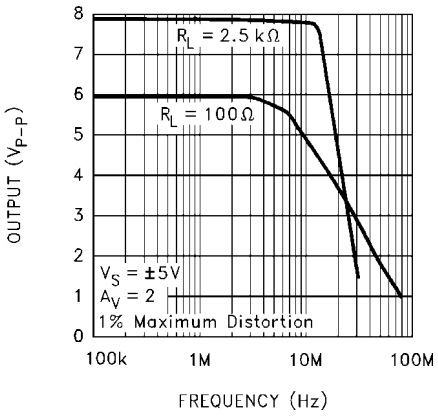
20159547

Undistorted Output Swing vs Frequency



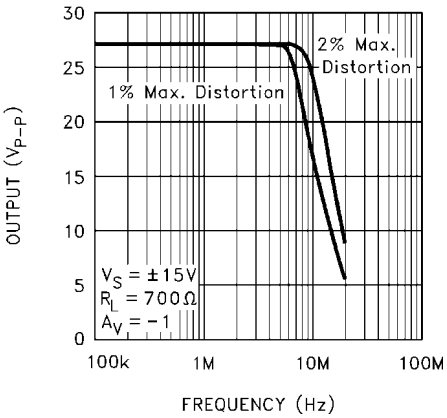
20159549

Undistorted Output Swing vs Frequency



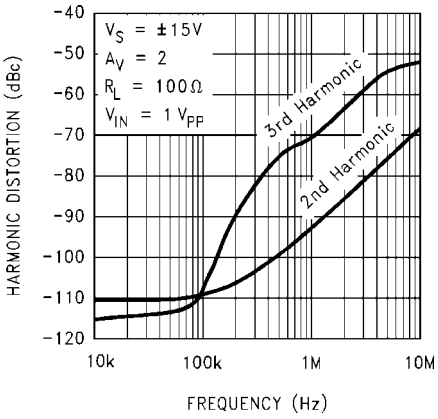
20159548

Undistorted Output Swing vs Frequency



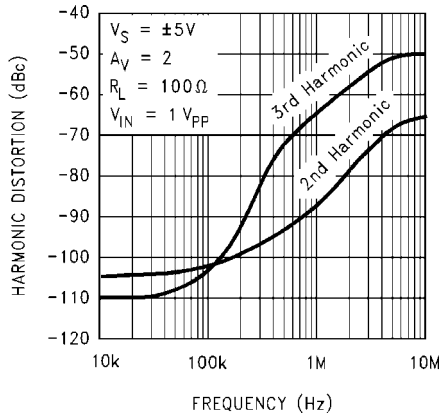
20159550

Harmonic Distortion vs Frequency



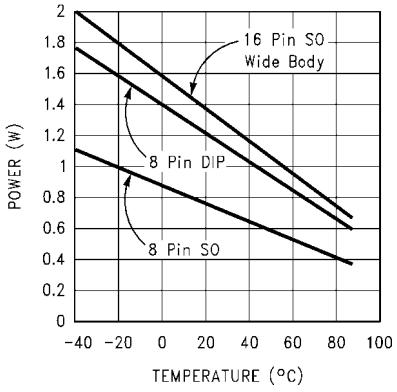
20159574

Harmonic Distortion vs Frequency



20159575

Maximum Power Dissipation vs Ambient Temperature



20159520

Note 15: The THD measurement at low frequency is limited by the test instrument.

Application Notes

LM7171 Performance Discussion

The LM7171 is a very high speed, voltage feedback amplifier. It consumes only 6.5 mA supply current while providing a unity-gain bandwidth of 200 MHz and a slew rate of 4100V/µs. It also has other great features such as low differential gain and phase and high output current.

The LM7171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFAs) have high impedance nodes. The low impedance inverting input in CFAs and a feedback capacitor create an additional pole that will lead to instability. As a result, CFAs cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators where a feedback capacitor is required.

LM7171 Circuit Operation

The class AB input stage in the LM7171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM7171 Simplified Schematic, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM7171 Slew Rate Characteristic

The slew rate of the LM7171 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations. A curve of slew rate versus input voltage level is provided in the “Typical Performance Characteristics”.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external resistor such as 1 kΩ in series with the input of the LM7171, the bandwidth is reduced to help lower the overshoot.

Slew Rate Limitation

If the amplifier's input signal has too large of an amplitude at too high of a frequency, the amplifier is said to be slew rate limited; this can cause ringing in time domain and peaking in frequency domain at the output of the amplifier.

In the “Typical Performance Characteristics” section, there are several curves of A_V = +2 and A_V = +4 versus input signal levels. For the A_V = +4 curves, no peaking is present and the LM7171 responds identically to the different input signal levels of 30 mV, 100 mV and 300 mV.

For the A_V = +2 curves, slight peaking occurs. This peaking at high frequency (>100 MHz) is caused by a large input signal at high enough frequency that exceeds the amplifier's slew rate. The peaking in frequency response does not limit the pulse response in time domain, and the LM7171 is stable with noise gain of ≥+2.

Layout Consideration

PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect high frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENT SELECTION AND FEEDBACK RESISTOR

It is important in high speed applications to keep all component leads short. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For the LM7171, a feedback resistor of 510Ω gives optimal performance.

Compensation for Input Capacitance

The combination of an amplifier's input capacitance with the gain setting resistors, adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F$$

can be used to cancel that pole. For the LM7171, a feedback capacitor of 2 pF is recommended. *Figure 1* illustrates the compensation circuit.

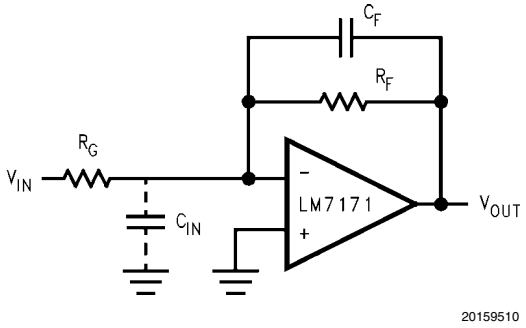


FIGURE 1. Compensating for Input Capacitance

Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 µF ceramic capacitors directly to power supply pins and 2.2 µF tantalum capacitors close to the power supply pins.

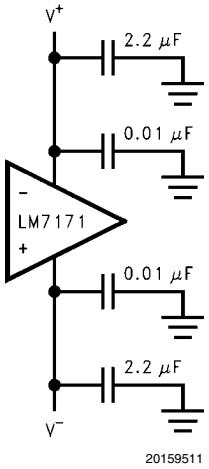


FIGURE 2. Power Supply Bypassing

Termination

In high frequency applications, reflections occur if signals are not properly terminated. *Figure 3* shows a properly terminated signal while *Figure 4* shows an improperly terminated signal.

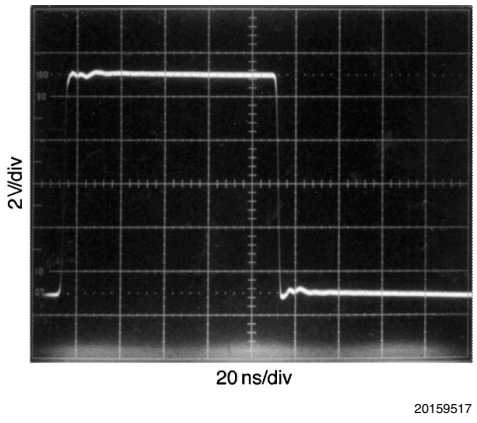


FIGURE 3. Properly Terminated Signal

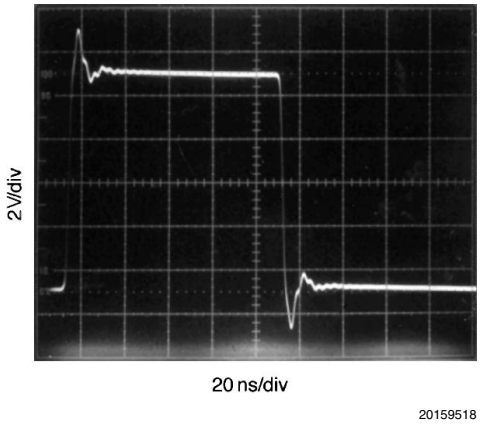


FIGURE 4. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown below in *Figure 5*. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM7171, a 50Ω isolation resistor is recommended for initial evaluation. *Figure 6* shows the LM7171 driving a 150 pF load with the 50Ω isolation resistor.

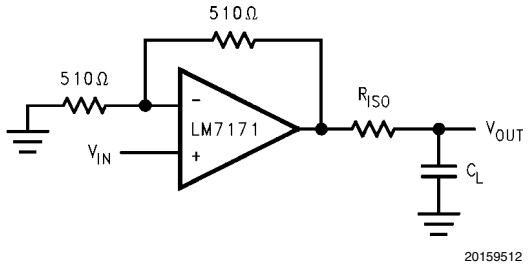


FIGURE 5. Isolation Resistor Used to Drive Capacitive Load

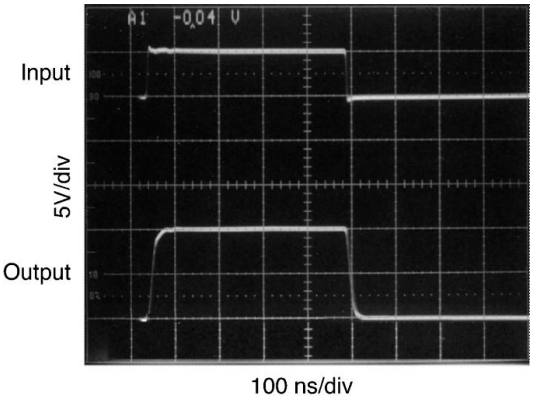


FIGURE 6. The LM7171 Driving a 150 pF Load with a 50Ω Isolation Resistor

Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A)/\theta_{JA}$$

Where

PD is the power dissipation in a device

$T_{J(max)}$ is the maximum junction temperature

T_A is the ambient temperature

θ_{JA} is the thermal resistance of a particular package

For example, for the LM7171 in a Ceramic SOIC package, the maximum power dissipation at 25°C ambient temperature is 680 mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin DIP package has a lower thermal resistance (106°C/W) than that of the Ceramic SOIC (182°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

P_Q: = supply current × total supply voltage with no load

P_L: = output current × (voltage difference between supply voltage and output voltage of the same side of supply voltage)

For example, the total power dissipated by the LM7171 with V_S = ±15V and output voltage of 10V into 1 kΩ is

$P_D = P_Q + P_L$

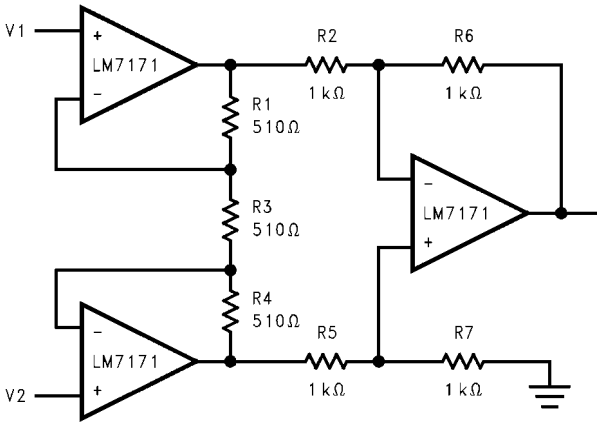
= (6.5 mA) × (30V) + (10 mA) × (15V − 10V)

= 195 mW + 50 mW

= 245 mW

Application Circuit

Fast Instrumentation Amplifier



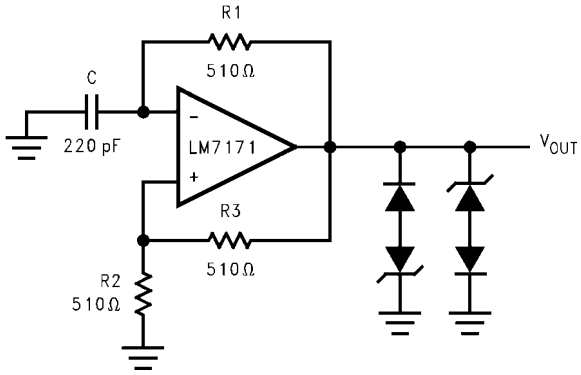
$$V_{IN} = V_2 - V_1$$

if R6 = R2, R7 = R5, and R1 = R4

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

20159580

Multivibrator

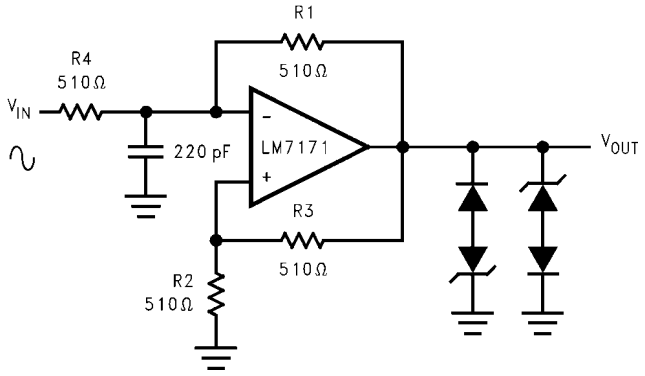


$$f = \frac{1}{2\left(R1\,C\ln\left(1 + 2\frac{R2}{R3}\right)\right)}$$

f = 4 MHz

20159581

Pulse Width Modulator



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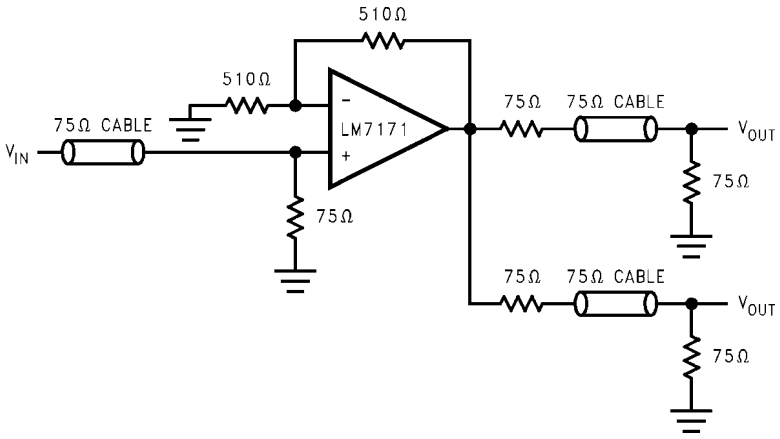
Video Line Driver

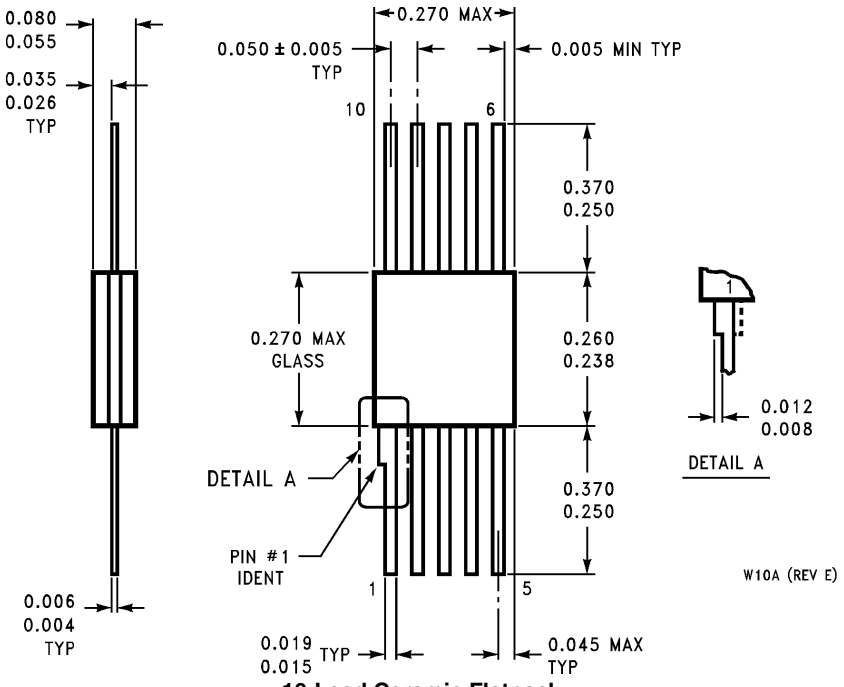


20159521

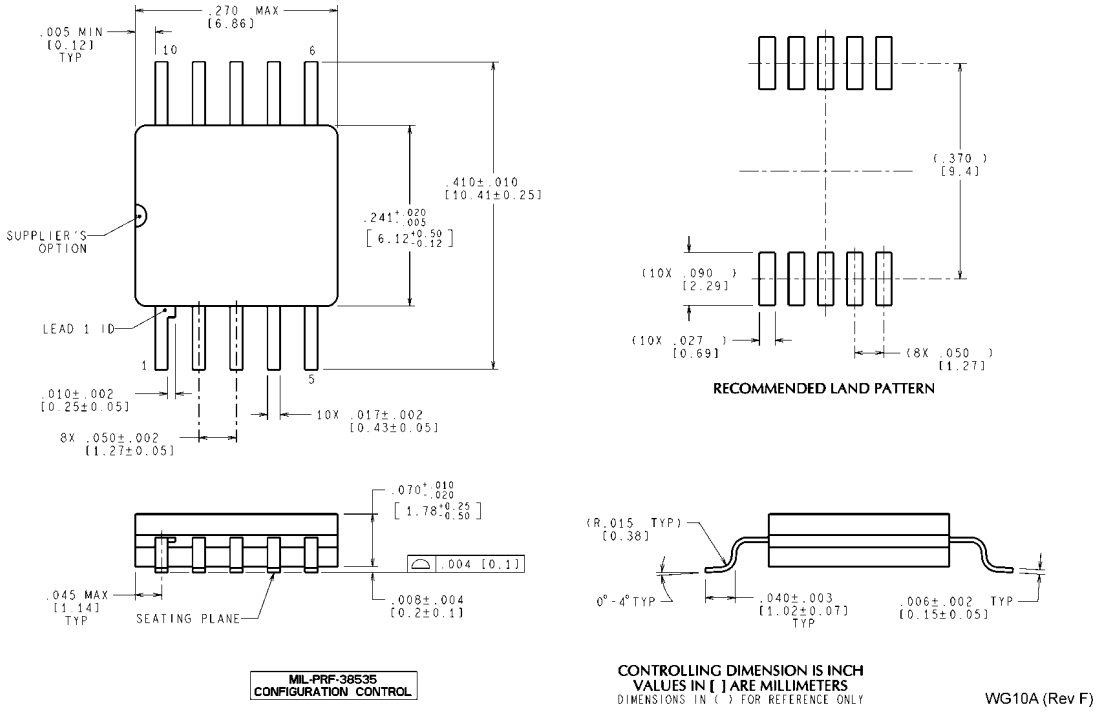
Revision History

Released	Revision	Section	Changes
02/04/09	A	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. Added ELDRS NSID's to Ordering Information Table. MNLM7171AM-X-RH Rev 0C0 will be archived.

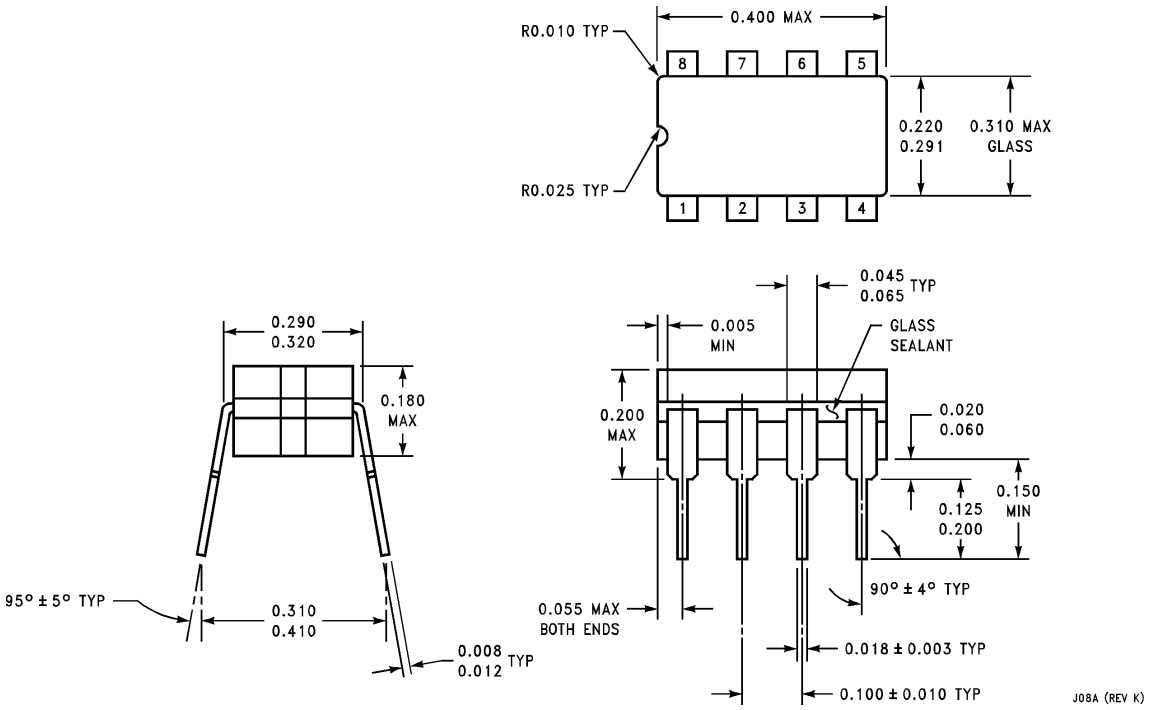
Physical Dimensions inches (millimeters) unless otherwise noted



10-Lead Ceramic Flatpack
NS Package Number W10A



10-Lead Ceramic SOIC
NS Package Number WG10A



8-Lead Dual-In-Line Package
NS Package Number J08A

Notes

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