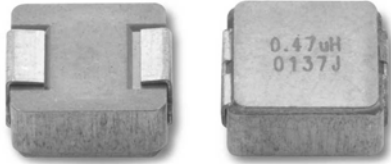


Low Profile, High Current IHLP® Inductor



Manufactured under one or more of the following:
US Patents; 6,198,375/6,204,744/6,449,829/6,460,244.
 Several foreign patents, and other patents pending.

FEATURES

- Shielded construction
- Frequency range up to 5.0 MHz
- Lowest DCR/µH, in this package size
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- Compliant to RoHS Directive 2002/95/EC



RoHS
 COMPLIANT
GREEN
 (5-2008)**

APPLICATIONS

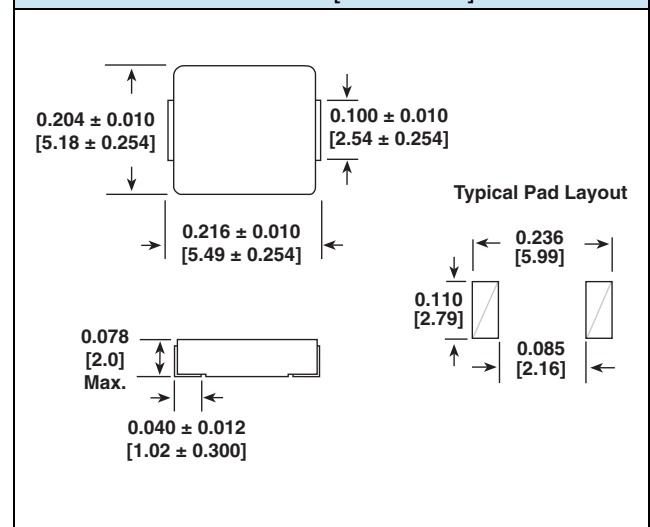
- PDA/notebook/desktop/server applications
- High current POL converters
- Low profile, high current power supplies
- Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)

STANDARD ELECTRICAL SPECIFICATIONS				
L ₀ INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (µH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) ⁽³⁾	SATURATION CURRENT DC TYP. (A) ⁽⁴⁾
0.10	3.6	3.9	17.0	45.0
0.22	4.9	5.2	15.0	22.0
0.33	7.6	8.2	12.0	25.0
0.47	8.9	9.4	11.5	21.0
0.68	11.2	12.4	10.0	15.0
1.0	18.9	20.0	7.0	16.0
2.2	45.6	50.1	4.2	9.5
3.3	79.2	85.5	3.3	8.5
4.7	108.0	116.6	2.8	5.0
5.6	113.0	122.0	2.5	4.5
6.8	139.0	150.0	2.4	4.3
10	184.0	199.0	2.3	4.0

Notes

- (1) All test data is referenced to 25 °C ambient
 - (2) Operating temperature range - 55 °C to + 125 °C
 - (3) DC current (A) that will cause an approximate ΔT of 40 °C
 - (4) DC current (A) that will cause L₀ to drop approximately 20 %
- (5) The part temperature (ambient + temp. rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.

DIMENSIONS in inches [millimeters]



DESCRIPTION

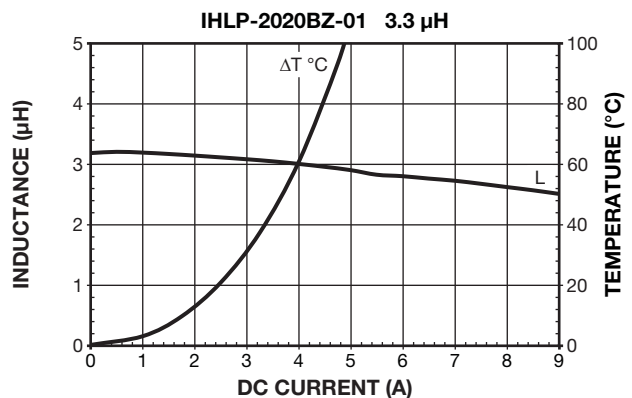
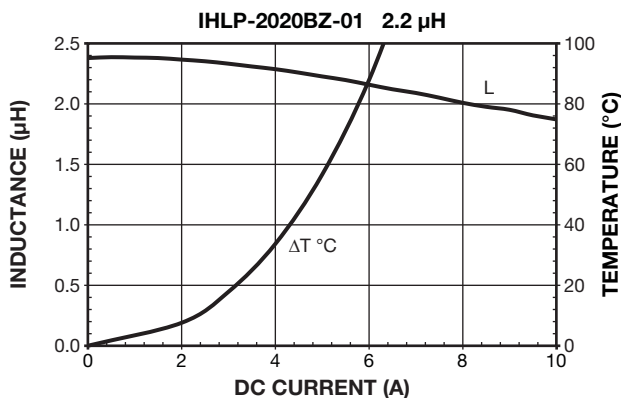
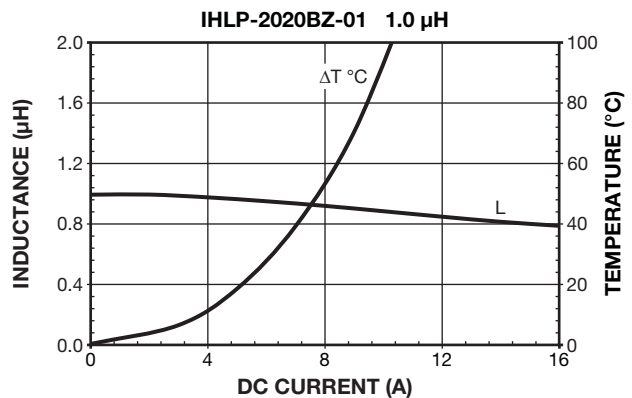
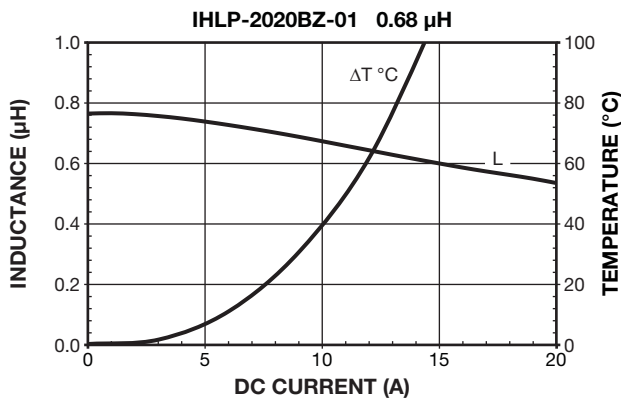
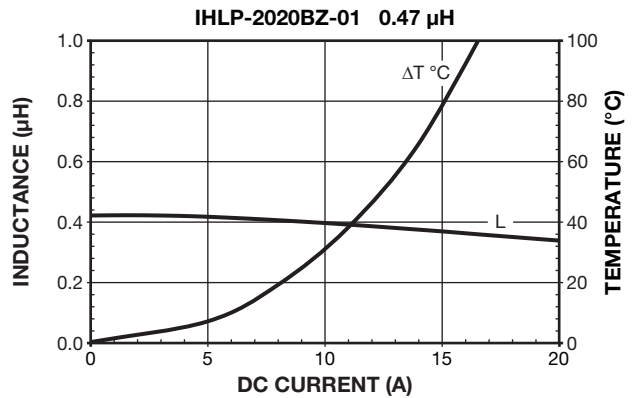
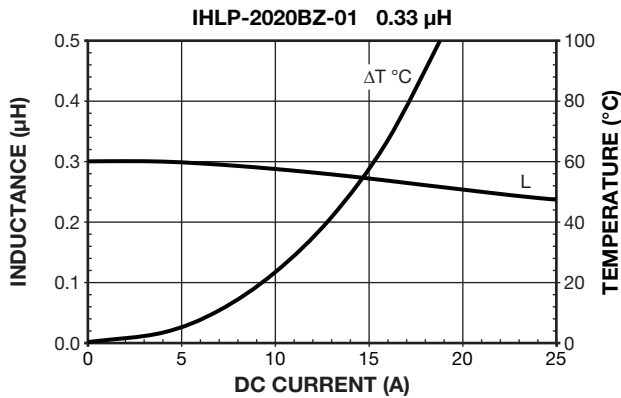
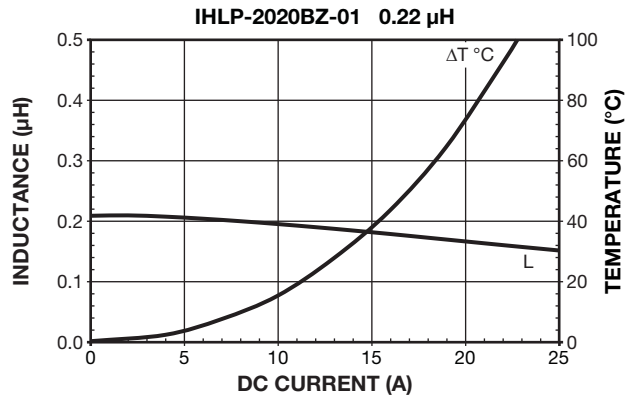
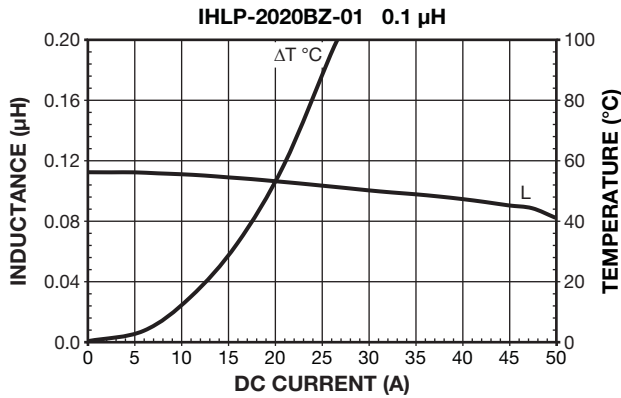
IHLP-2020BZ-01	4.7 µH	± 20 %	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC LEAD (Pb)-FREE STANDARD

GLOBAL PART NUMBER

I	H	L	P	2	0	2	0	B	Z	E	R	4	R	7	M	0	1
PRODUCT FAMILY				SIZE				PACKAGE CODE		INDUCTANCE VALUE			TOL.	SERIES			

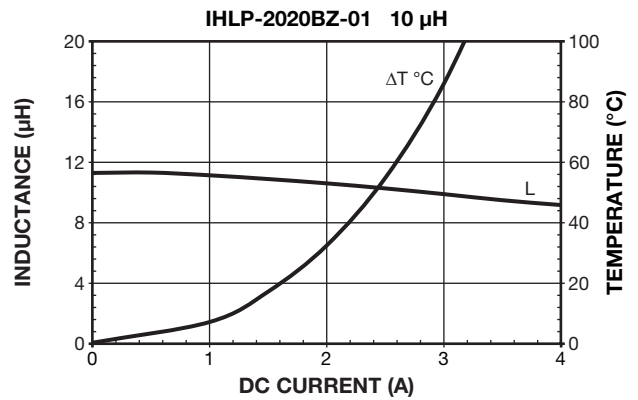
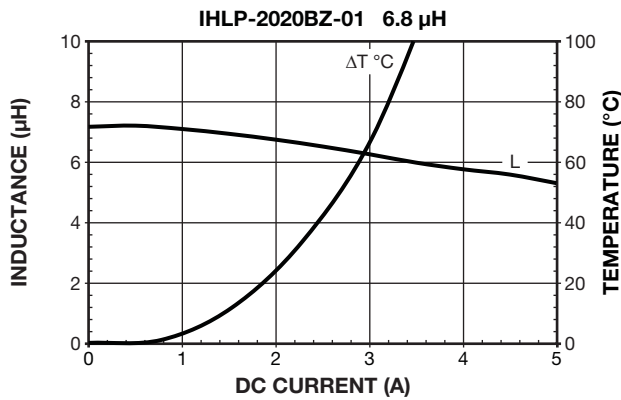
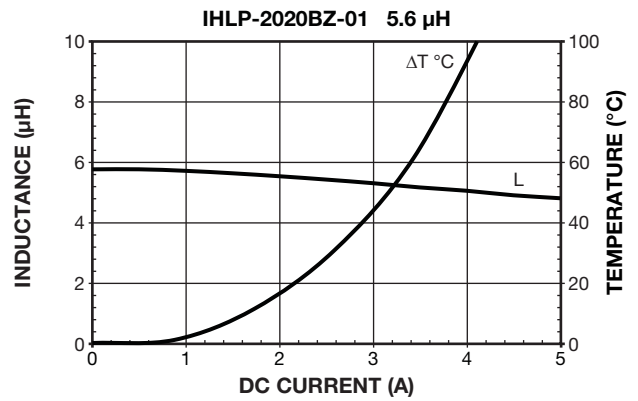
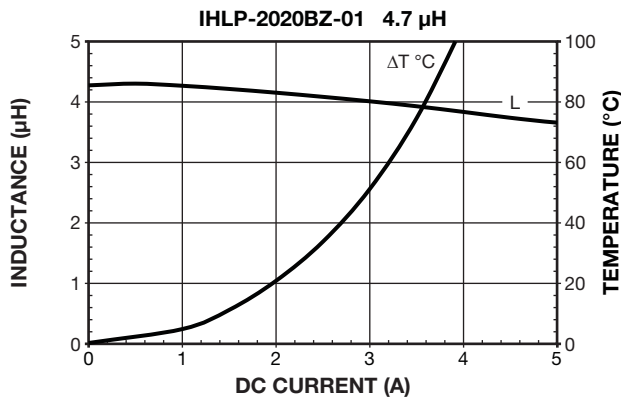
** Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

PERFORMANCE GRAPHS

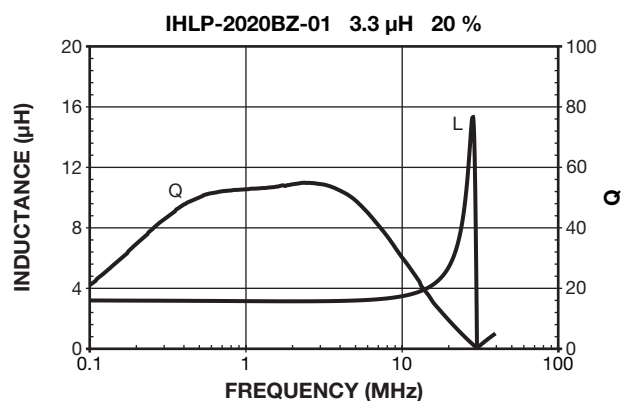
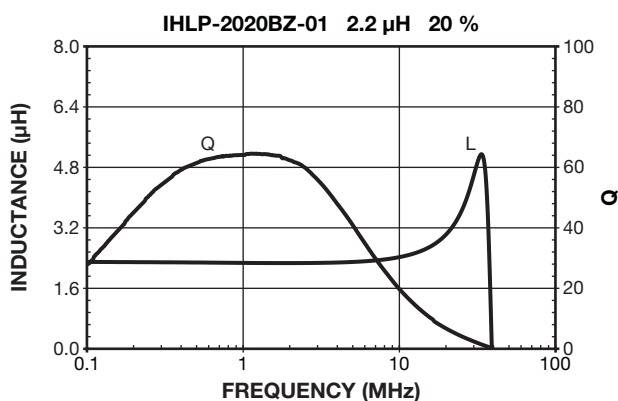
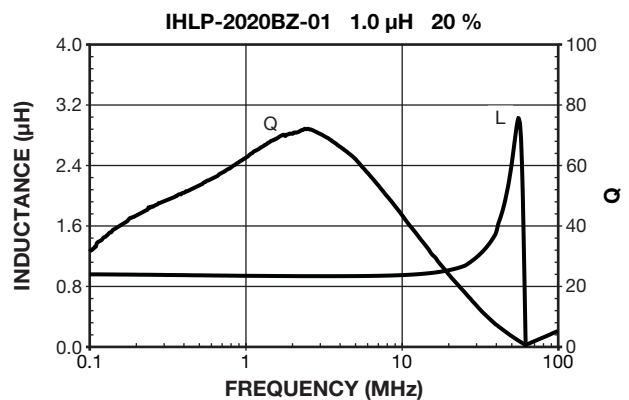
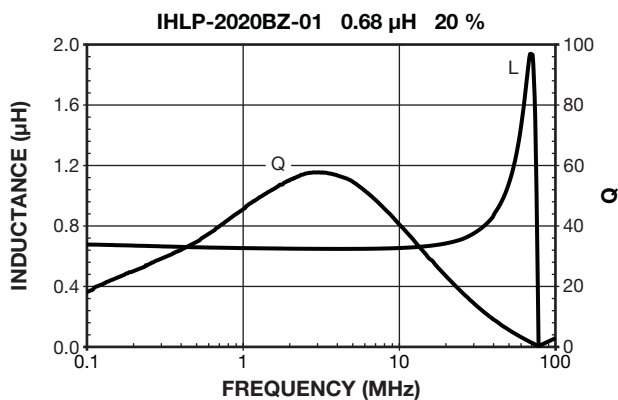
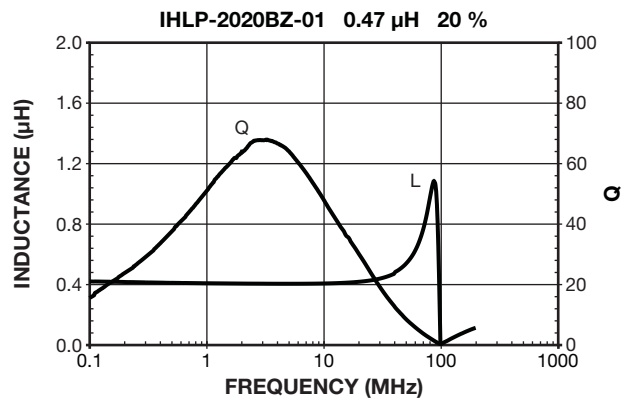
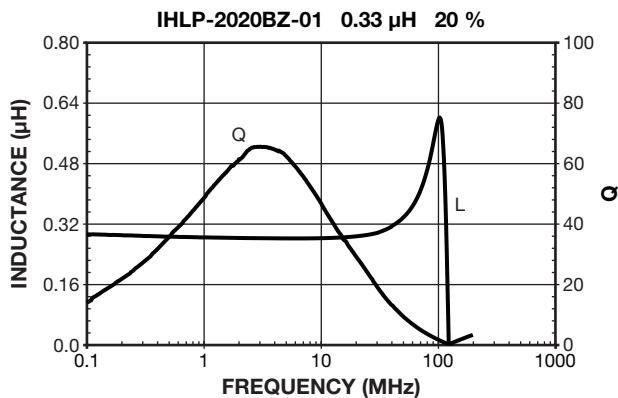
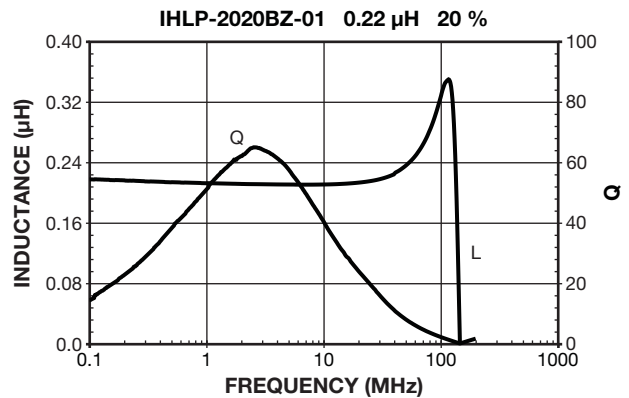
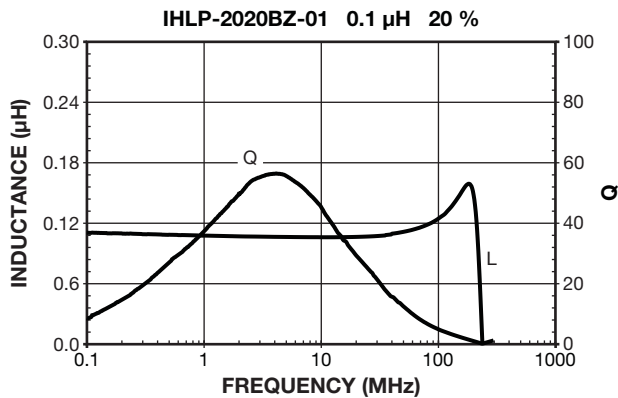




PERFORMANCE GRAPHS

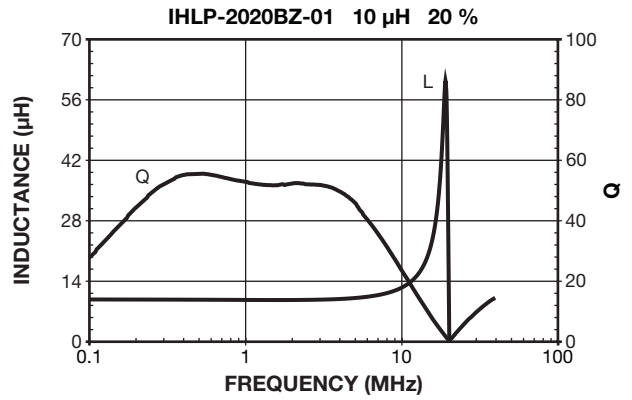
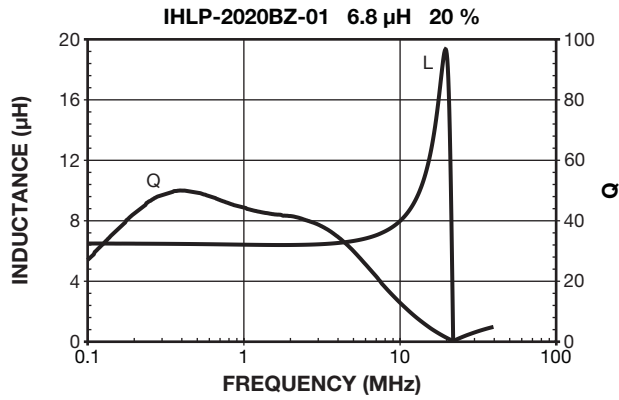
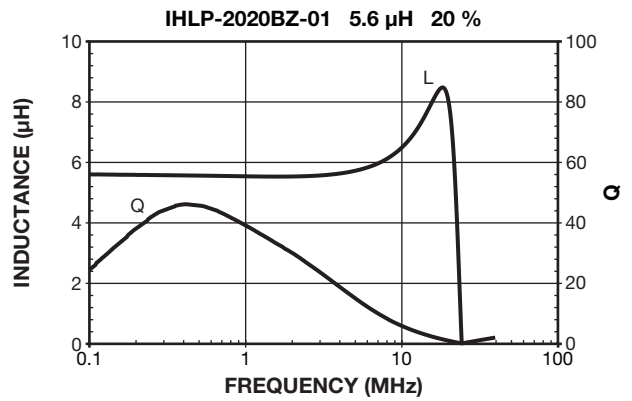
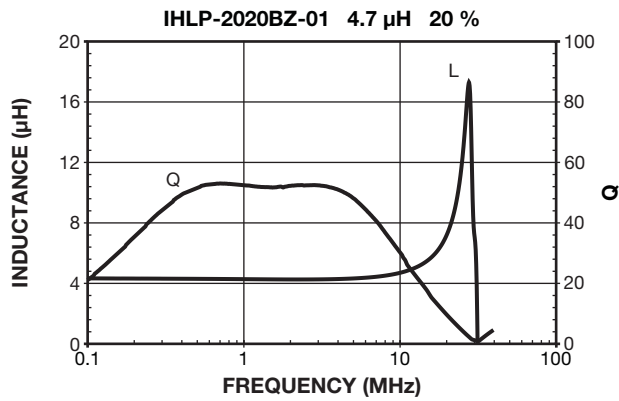


PERFORMANCE GRAPHS: INDUCTANCE AND Q VS. FREQUENCY





PERFORMANCE GRAPHS: INDUCTANCE AND Q VS. FREQUENCY





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