74LV74

Dual D-type flip-flop with set and reset; positive edge-trigger

Rev. 03 — 28 September 2007 Product data sheet

1. General description

The 74LV74 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC74 and 74HCT74.

The device is a dual positive edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}$D) and ($\overline{R}$D) inputs, and complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt trigger action in the clock input makes the circuit highly tolerant of slower clock rise and fall times.

2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical output V_{OH} undershoot > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

founded by Philips

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV74N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV74D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV74DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV74PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV74PW	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

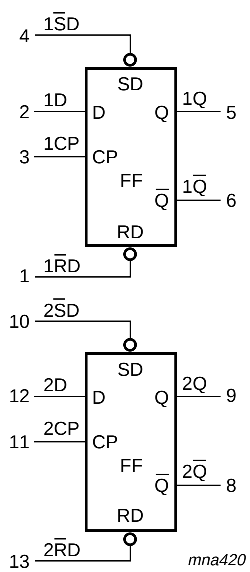


Fig 1. Logic symbol

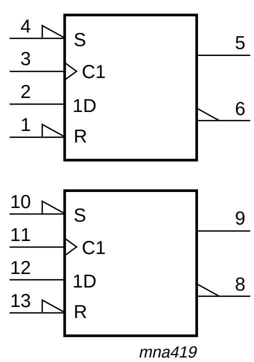


Fig 2. IEC logic symbol

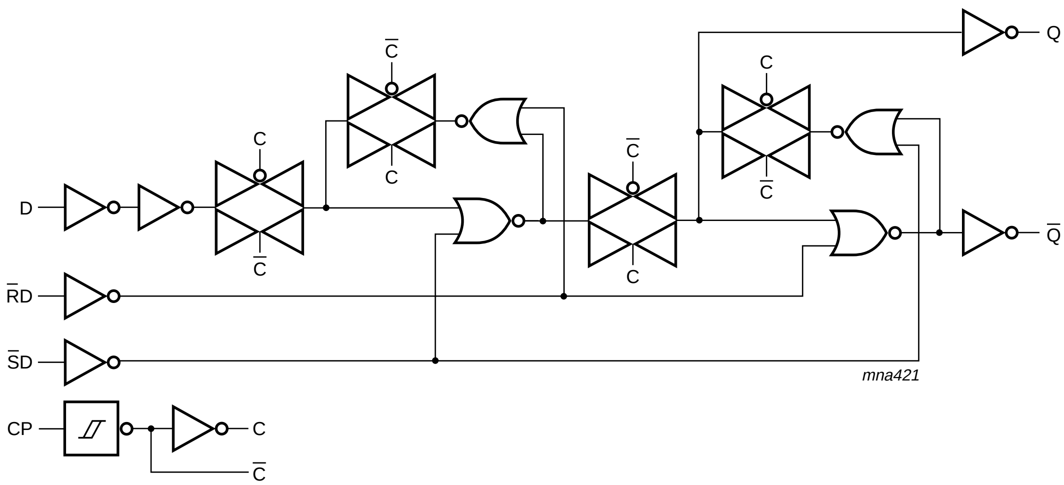


Fig 3. Logic diagram (one flip-flop)

5. Pinning information

5.1 Pinning

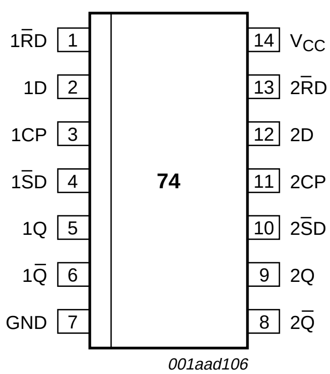
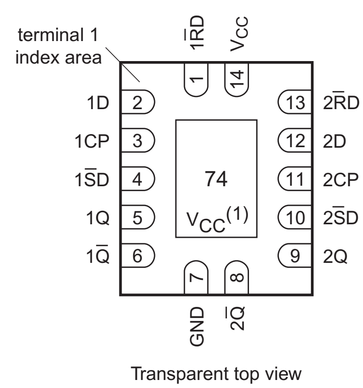


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol (n = 1, 2)	Pin	Description
n$\overline{RD}$	1, 13	asynchronous reset-direct input (active LOW)
nD	2, 12	data input
nCP	3, 11	clock input (LOW-to-HIGH, edge-triggered)
n$\overline{SD}$	4, 10	asynchronous set-direct input (active LOW)
nQ	5, 9	true flip-flop output
n$\overline{Q}$	6, 8	complement flip-flop output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Inputs				Outputs	
n$\overline{SD}$	**n$\overline{RD}$**	**nCP**	**nD**	**nQ**	**n$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don’t care

Table 4. Function table[1]

Inputs				Outputs	
n$\overline{SD}$	**n$\overline{RD}$**	**nCP**	**nD**	**nQ_{n+1}**	**$n\overline{Q}_{n+1}$**
H	H	$\uparrow$	L	L	H
H	H	$\uparrow$	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level
$\uparrow$ = LOW-to-HIGH transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±50	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
		DIP14 package	[2]	-	750	mW
		SO14 package	[3]	-	500	mW
		(T)SSOP14 package	[4]	-	500	mW
		DHVQFN14 package	[5]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage[1]		1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate[2]	$V_{CC} = 1.0$ V to 2.0 V	-	-	500	ns/V
		$V_{CC} = 2.0$ V to 2.7 V	-	-	200	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	100	ns/V
		$V_{CC} = 3.6$ V to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from $V_{CC} = 1.2$ V to $V_{CC} = 5.5$ V, but LV devices are guaranteed to function down to $V_{CC} = 1.0$ V (with input levels GND or V_{CC}).

[2] Except for clock inputs, which have Schmitt trigger action..

9. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7V_{CC}	-	-	0.7V_{CC}	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3V_{CC}	-	0.3V_{CC}	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = −100 μA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		I_O = −100 μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I_O = −100 μA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I_O = −100 μA; V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I_O = −100 μA; V_{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I_O = −6 mA; V_{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
		I_O = −12 mA; V_{CC} = 4.5 V	3.6	4.2	-	3.5	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.2 V	-	0	-	-	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	-	0.65	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20	-	80	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC}$ − 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 8. Dynamic characteristics
GND = 0 V; For test circuit see Figure 8.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, n$\overline{Q}$; see Figure 6	[2]						
		V_{CC} = 1.2 V		-	70	-	-	-	ns
		V_{CC} = 2.0 V		-	24	44	-	56	ns
		V_{CC} = 2.7 V		-	18	28	-	41	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	11	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	13	26	-	33	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	-	9.5	17	-	23	ns
		n$\overline{SD}$ to nQ, n$\overline{Q}$; n$\overline{RD}$ to nQ, n$\overline{Q}$; see Figure 7							
		V_{CC} = 1.2 V		-	90	-	-	-	ns
		V_{CC} = 2.0 V		-	31	46	-	58	ns
		V_{CC} = 2.7 V		-	23	34	-	43	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	14	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	17	27	-	34	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	-	12	19	-	24	ns
t_W	pulse width	clock HIGH or LOW; see Figure 6; set or reset LOW; see Figure 7							
		V_{CC} = 2.0 V		34	10	-	41	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	7	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	15	6	-	18	-	ns
t_{rec}	recovery time	set or reset; see Figure 7							
		V_{CC} = 1.2 V		-	5	-	-	-	ns
		V_{CC} = 2.0 V		14	2	-	15	-	ns
		V_{CC} = 2.7 V		10	1	-	11	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	8	1	-	9	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	6	1	-	7	-	ns
t_{su}	set-up time	nD to nCP; see Figure 6							
		V_{CC} = 1.2 V		-	10	-	-	-	ns
		V_{CC} = 2.0 V		22	4	-	26	-	ns
		V_{CC} = 2.7 V		12	3	-	15	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	8	2	-	10	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	6	1	-	8	-	ns

Table 8. Dynamic characteristics *…continued*

GND = 0 V; For test circuit see Figure 8.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_h	hold time	nD to nCP; see Figure 6							
		V_{CC} = 1.2 V		-	–10	-	-	-	ns
		V_{CC} = 2.0 V		3	–2	-	3	-	ns
		V_{CC} = 2.7 V		3	–2	-	3	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	3	–2	-	3	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	3	–2	-	3	-	ns
f_{max}	maximum frequency	see Figure 6							
		V_{CC} = 2.0 V		14	40	-	12	-	MHz
		V_{CC} = 2.7 V		50	90	-	40	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF		-	76	-	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[3]	60	100	-	48	-	MHz
		V_{CC} = 4.5 V to 5.5 V	[3]	70	110	-	56	-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC}	[4]	-	24	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

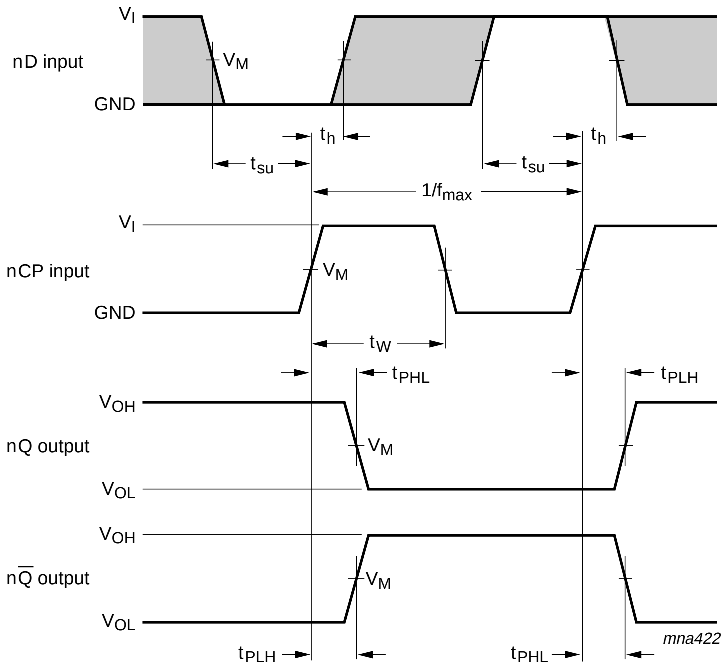
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. Waveforms

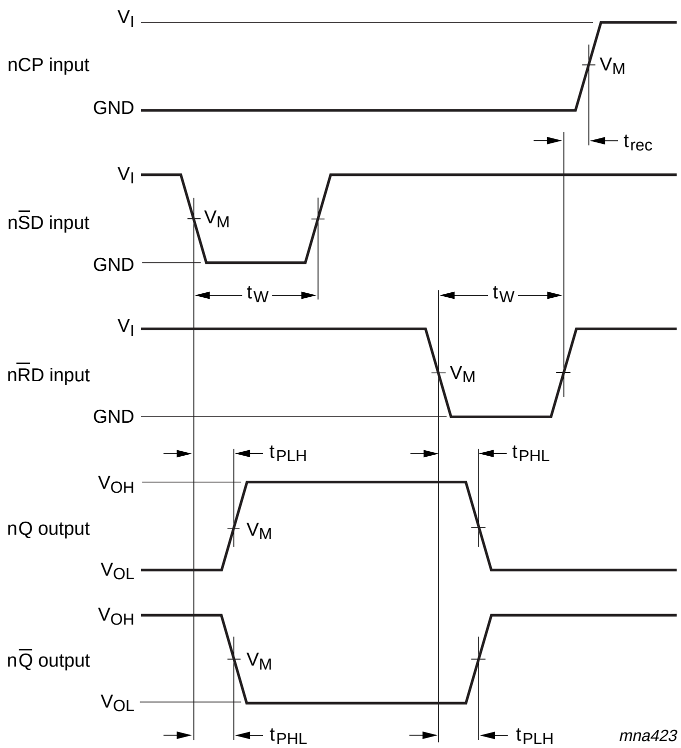


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 6. The clock input (nCP) to output (nQ, n$\overline{Q}$) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, and the maximum frequency



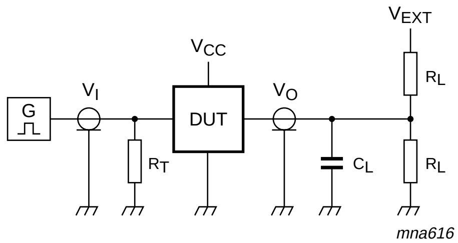
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 7. The set ($n\overline{SD}$) and reset ($n\overline{RD}$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse widths, and the $n\overline{RD}$ to nCP recovery time

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 10.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

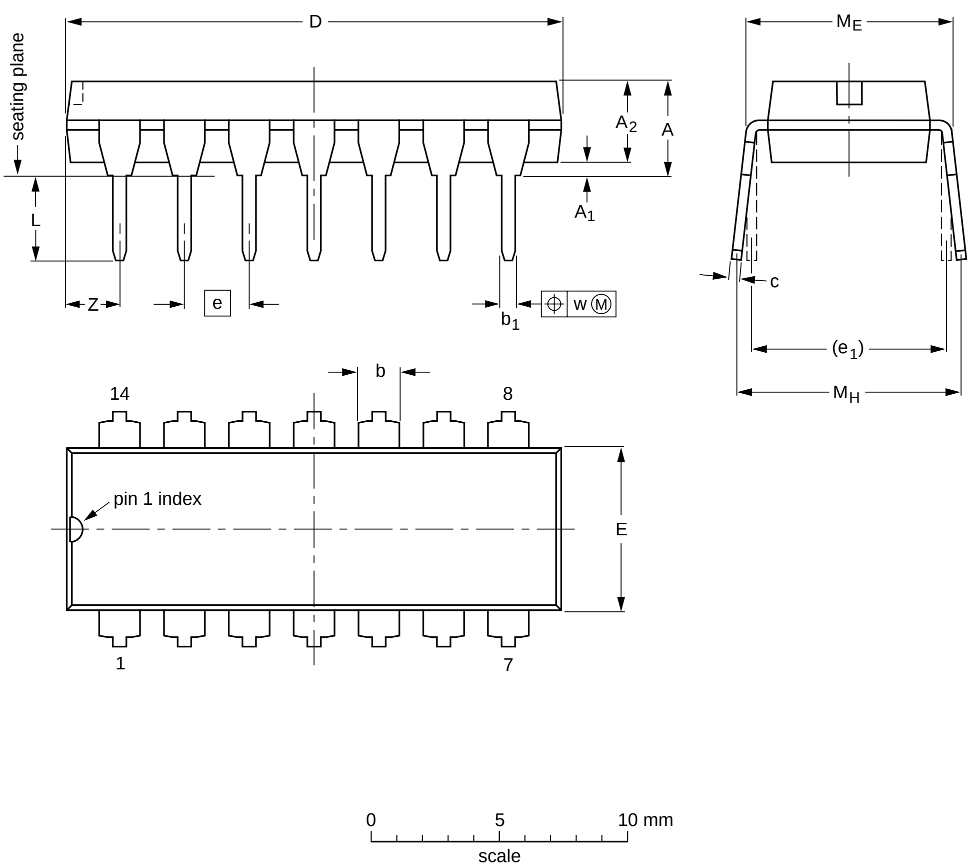
Fig 8. Load circuit for switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

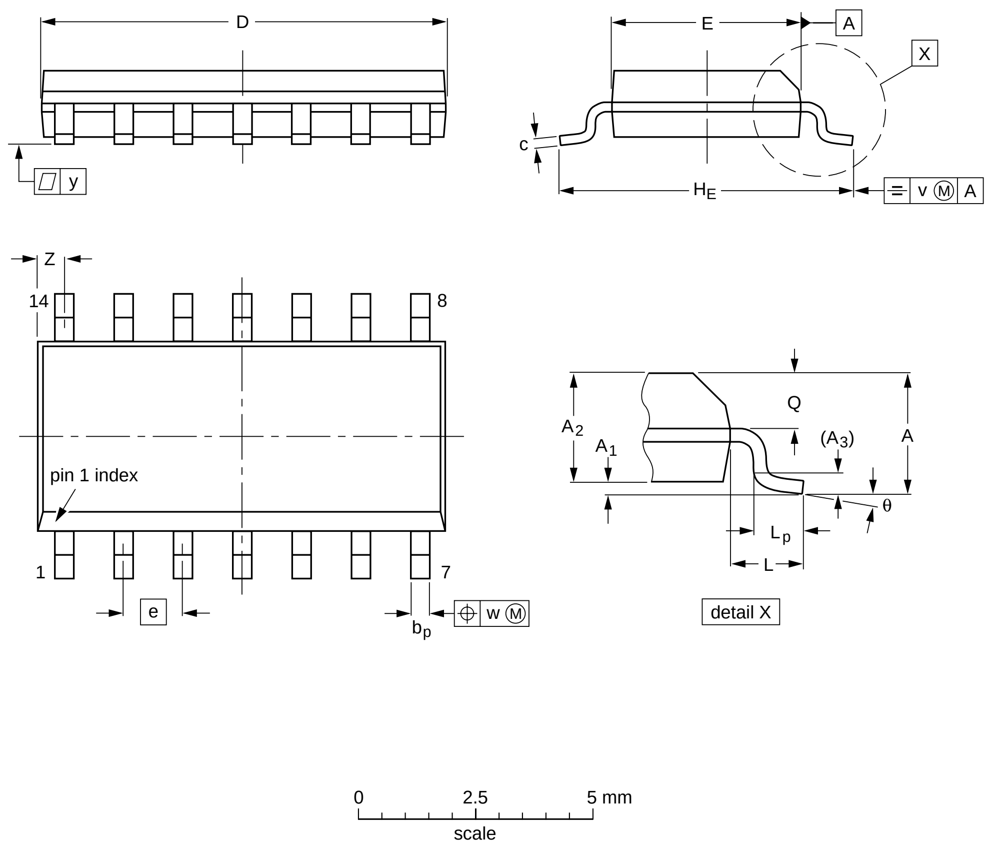
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

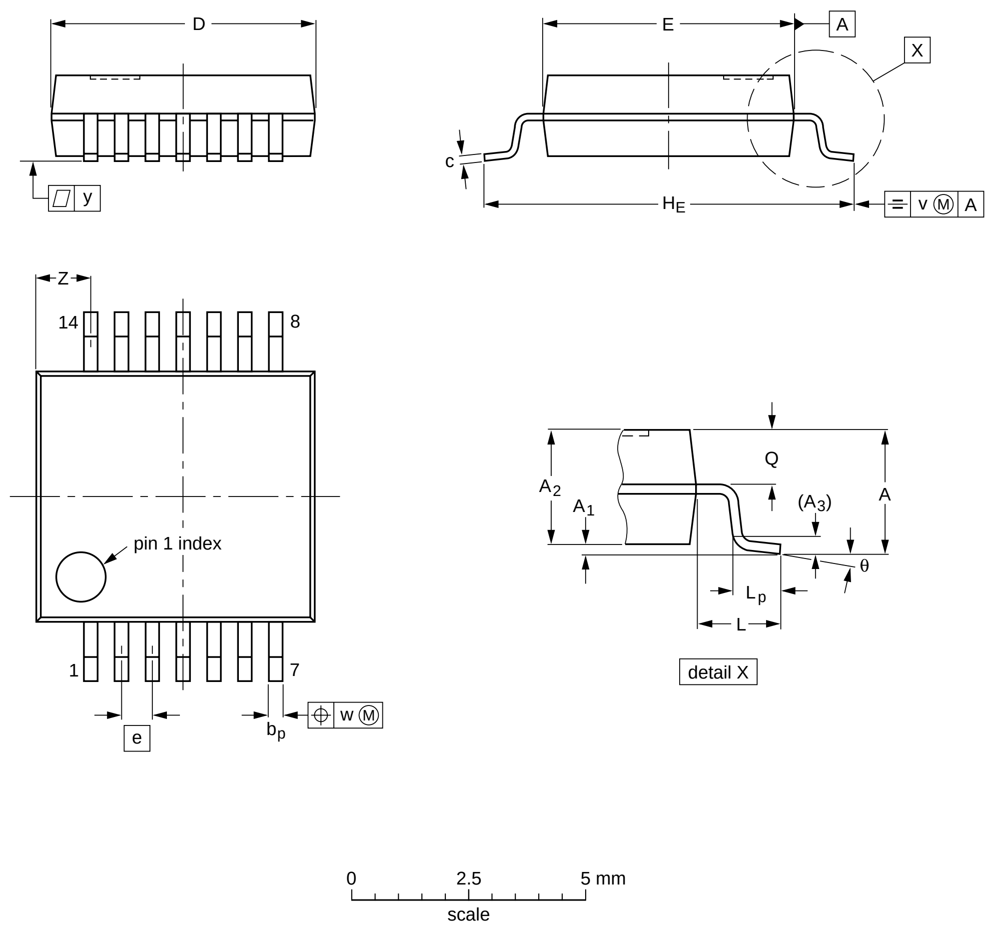
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

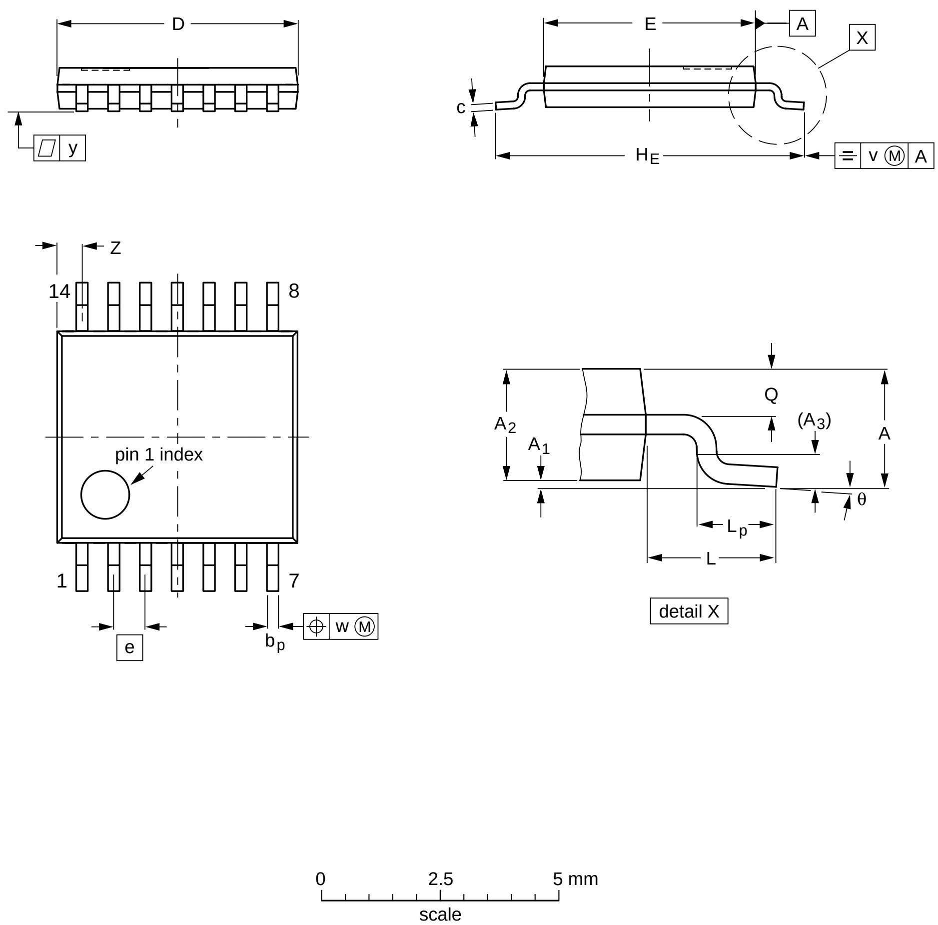
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

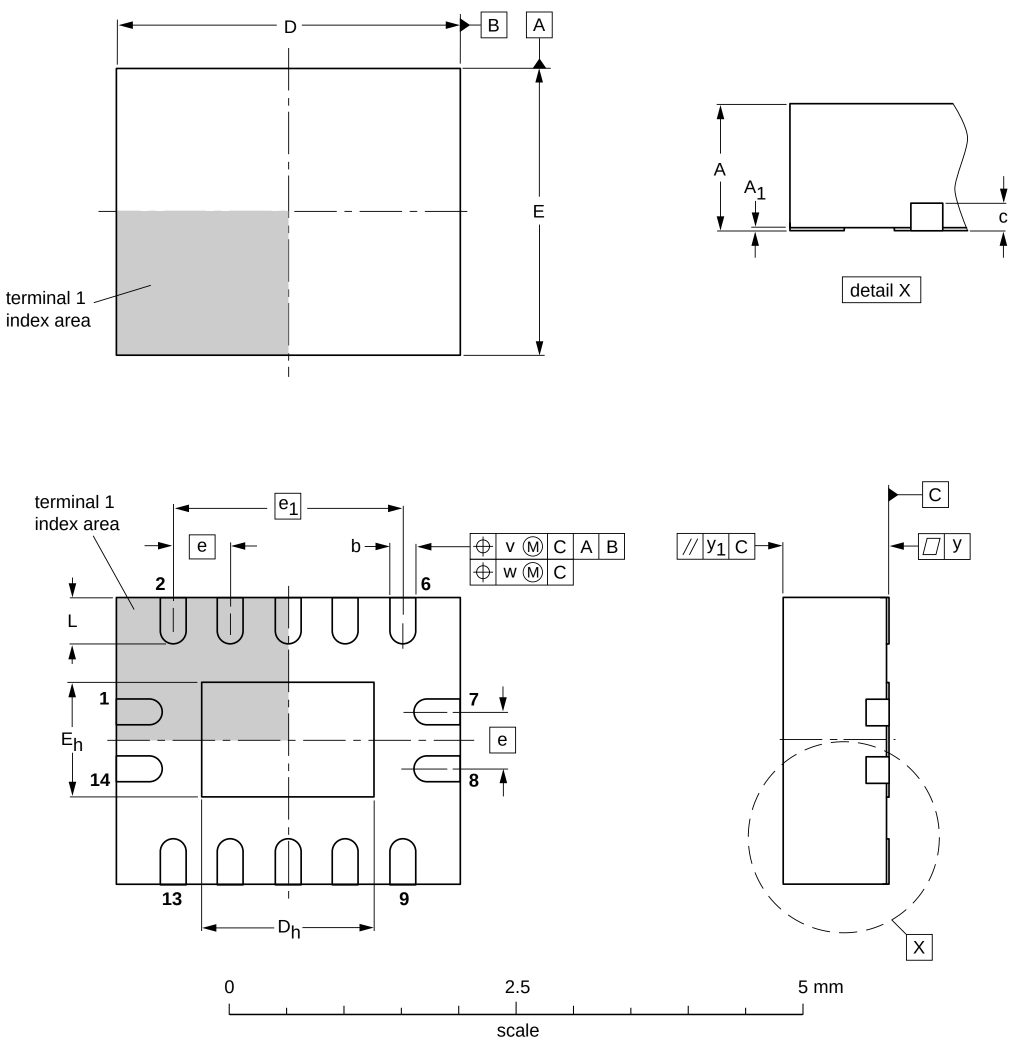
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV74_3	20070928	Product data sheet	-	74LV74_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name when appropiate. • Section 3: DHVQFN14package added. • Section 7: derating values added for DHVQFN14 package. • Section 12: outline drawing added for DHVQFN14 package.			
74LV74_2	19980420	Product specification	-	74LV74_1
74LV74_1	19961107	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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