

Features

- Pin and function compatible with CY7C1049CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 90 \text{ mA @ } 10 \text{ ns (Industrial)}$
- Low CMOS standby power
 - $I_{SB2} = 10 \text{ mA}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in Pb-free 36-pin (400 Mil) Molded SOJ and 44-pin TSOP II packages

Functional Description

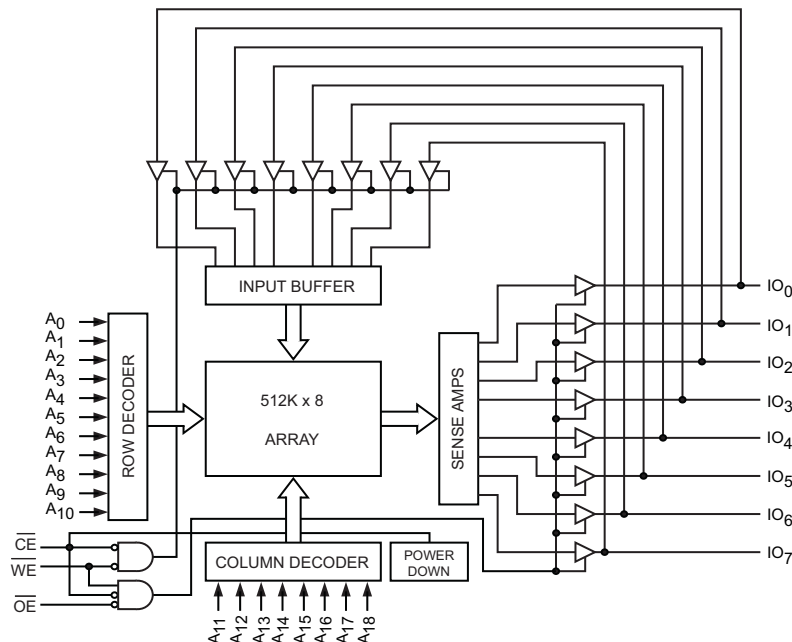
The CY7C1049DV33 is a high performance CMOS Static RAM organized as 512K words by 8-bits. Easy memory expansion is provided by an Active LOW Chip Enable (\overline{CE}), an Active LOW Output Enable (\overline{OE}), and tri-state drivers. You can write to the device by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight IO pins (IO_0 through IO_7) is then written into the location specified on the address pins (A_0 through A_{18}).

You can read from the device by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.

The eight input or output pins (IO_0 through IO_7) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1049DV33 is available in standard 400 Mil wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

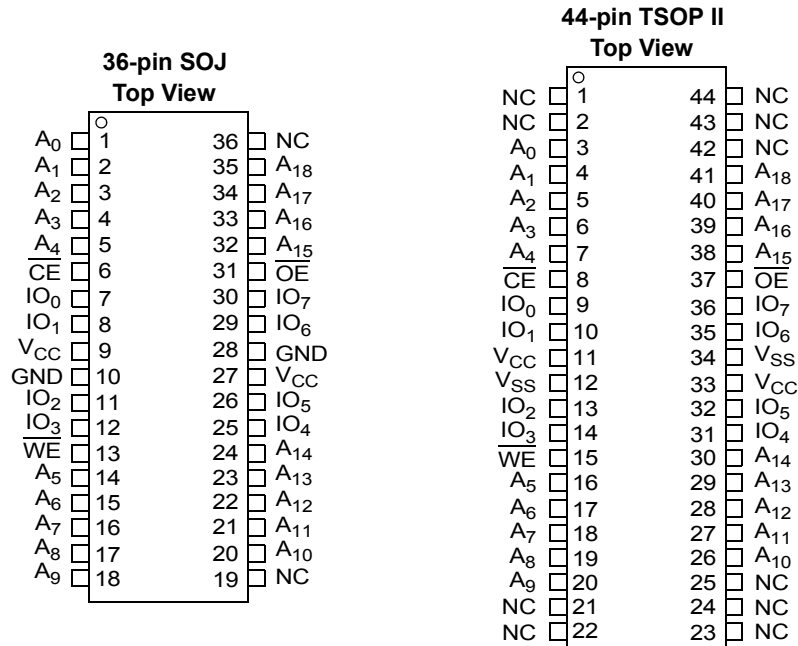
Logic Block Diagram



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Pin Configuration



Selection Guide

| | -10 (Industrial) | -12 (Automotive) ^[1] | Unit |
|------------------------------|------------------|---------------------------------|------|
| Maximum Access Time | 10 | 12 | ns |
| Maximum Operating Current | 90 | 95 | mA |
| Maximum CMOS Standby Current | 10 | 15 | mA |

Note

1. Automotive product information is preliminary.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

| | |
|--|----------------------------|
| Storage Temperature | -65 °C to +150 °C |
| Ambient Temperature with Power Applied | -55 °C to +125 °C |
| Supply Voltage on V_{CC} to Relative GND ^[2] | -0.3 V to +4.6 V |
| DC Voltage Applied to Outputs in High Z State ^[2] | -0.3 V to $V_{CC} + 0.3$ V |
| DC Input Voltage ^[2] | -0.3 V to $V_{CC} + 0.3$ V |

| | |
|----------------------------------|-------------------------------------|
| Current into Outputs (LOW) | 20 mA |
| Static Discharge Voltage | > 2001 V (MIL-STD-883, Method 3015) |

Latch up Current

Operating Range

| Range | Ambient Temperature | V_{CC} | Speed |
|------------|---------------------|---------------|-------|
| Industrial | -40 °C to +85 °C | 3.3 V ± 0.3 V | 10 ns |
| Automotive | -40 °C to +125 °C | 3.3 V ± 0.3 V | 12 ns |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | -10 (Industrial) | | -12 (Automotive) | | Unit | |
|----------------|--|--|------------------|----------------|------------------|----------------|------|----|
| | | | Min | Max | Min | Max | | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | - | 2.4 | - | V | |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$ | - | 0.4 | - | 0.4 | V | |
| $V_{IH}^{[2]}$ | Input HIGH Voltage | | 2.0 | $V_{CC} + 0.3$ | 2.0 | $V_{CC} + 0.3$ | V | |
| $V_{IL}^{[2]}$ | Input LOW Voltage ^[2] | | -0.3 | 0.8 | -0.3 | 0.8 | V | |
| I_{IX} | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | -1 | +1 | µA | |
| I_{OZ} | Output Leakage Current | $GND \leq V_{OUT} \leq V_{CC}$, Output Disabled | -1 | +1 | -1 | +1 | µA | |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max}$, $f = f_{MAX} = 1/t_{RC}$ | 100 MHz | - | 90 | - | - | mA |
| | | | 83 MHz | - | 80 | - | 95 | mA |
| | | | 66 MHz | - | 70 | - | 85 | mA |
| | | | 40 MHz | - | 60 | - | 75 | mA |
| I_{SB1} | Automatic CE Power down Current —TTL Inputs | Max V_{CC} , $\overline{CE} \geq V_{IH}$; $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | - | 20 | - | 25 | mA | |
| I_{SB2} | Automatic CE Power down Current —CMOS Inputs | Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$ | - | 10 | - | 15 | mA | |

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | Max | Unit |
|-----------|-------------------|--|-----|------|
| C_{IN} | Input Capacitance | $T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{ V}$ | 8 | pF |
| C_{OUT} | IO Capacitance | | 8 | pF |

Note

2. $V_{IL}(\text{min.}) = -2.0 \text{ V}$ and $V_{IH}(\text{max.}) = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

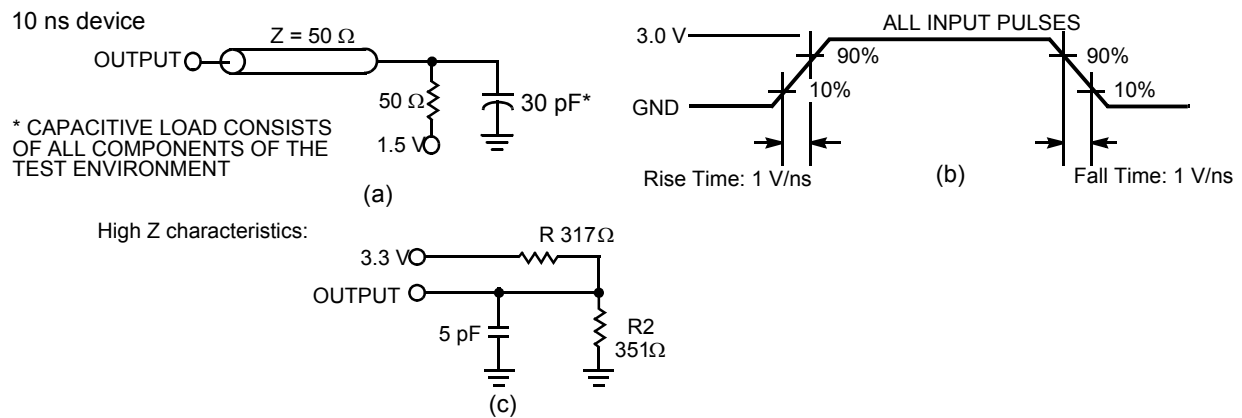
Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | 36-pin SOJ Package | 44-pin TSOP II Package | Unit |
|---------------|--|--|--------------------|------------------------|------|
| Θ_{JA} | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 inch, two layer printed circuit board | 57.91 | 50.66 | °C/W |
| Θ_{JC} | Thermal Resistance (Junction to Case) | | 36.73 | 17.17 | °C/W |

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms [4]

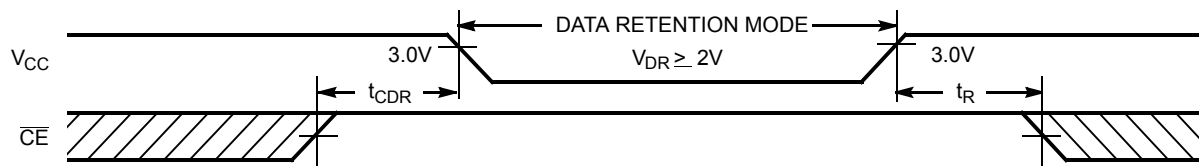


Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions [5] | Min | Max | Unit | |
|-----------------|--------------------------------------|---|------------|-----|------|----|
| V_{DR} | V_{CC} for Data Retention | | 2.0 | – | V | |
| I_{CCDR} | Data Retention Current | $V_{CC} = V_{DR} = 2.0 \text{ V}$, $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$ | Industrial | – | 10 | mA |
| | | $V_{IN} \geq V_{CC} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$ | Auto | – | 15 | mA |
| $t_{CDR}^{[3]}$ | Chip Deselect to Data Retention Time | | 0 | – | ns | |
| $t_R^{[6]}$ | Operation Recovery Time | | t_{RC} | – | ns | |

Figure 2. Data Retention Waveform



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in Figure 1 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 1 (c).
- No input may exceed $V_{CC} + 0.3 \text{ V}$.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50 \mu\text{s}$ or stable at $V_{CC(min.)} \geq 50 \mu\text{s}$.

AC Switching Characteristics

Over the Operating Range ^[7]

| Parameter | Description | -10 (Industrial) | | -12 (Automotive) | | Unit |
|---------------------------------------|--|------------------|-----|------------------|-----|---------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| $t_{power}^{[8]}$ | V_{CC} (typical) to the first access | 100 | – | 100 | – | μ s |
| t_{RC} | Read Cycle Time | 10 | – | 12 | – | ns |
| t_{AA} | Address to Data Valid | – | 10 | – | 12 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | – | 3 | – | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | – | 10 | – | 12 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | – | 5 | – | 6 | ns |
| t_{LZOE} | \overline{OE} LOW to Low $Z^{[9]}$ | 0 | – | 0 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High $Z^{[9, 10]}$ | – | 5 | – | 6 | ns |
| t_{LZCE} | \overline{CE} LOW to Low $Z^{[9]}$ | 3 | – | 3 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to High $Z^{[9, 10]}$ | – | 5 | – | 6 | ns |
| t_{PU} | \overline{CE} LOW to Power up | 0 | – | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to Power down | – | 10 | – | 12 | ns |
| Write Cycle^[11, 12] | | | | | | |
| t_{WC} | Write Cycle Time | 10 | – | 12 | – | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 7 | – | 8 | – | ns |
| t_{AW} | Address Set up to Write End | 7 | – | 8 | – | ns |
| t_{HA} | Address Hold from Write End | 0 | – | 0 | – | ns |
| t_{SA} | Address Set up to Write Start | 0 | – | 0 | – | ns |
| t_{PWE} | \overline{WE} Pulse Width | 7 | – | 8 | – | ns |
| t_{SD} | Data Set up to Write End | 5 | – | 6 | – | ns |
| t_{HD} | Data Hold from Write End | 0 | – | 0 | – | ns |
| t_{LZWE} | \overline{WE} HIGH to Low $Z^{[9]}$ | 3 | – | 3 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High $Z^{[9, 10]}$ | – | 5 | – | 6 | ns |

Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
8. t_{POWER} gives the minimum amount of time that the power supply must be at stable, typical V_{CC} values until the first memory access is performed.
9. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of [Figure 1 on page 5](#). Transition is measured when the outputs enter a high impedance state.
11. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set up and hold timing must be referred to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 2 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 3. Read Cycle No. 1^[13, 14]

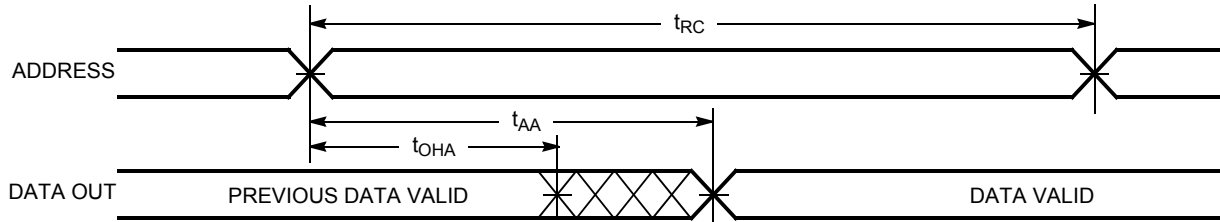


Figure 4. Read Cycle No. 2 (\overline{OE} Controlled)^[14, 15]

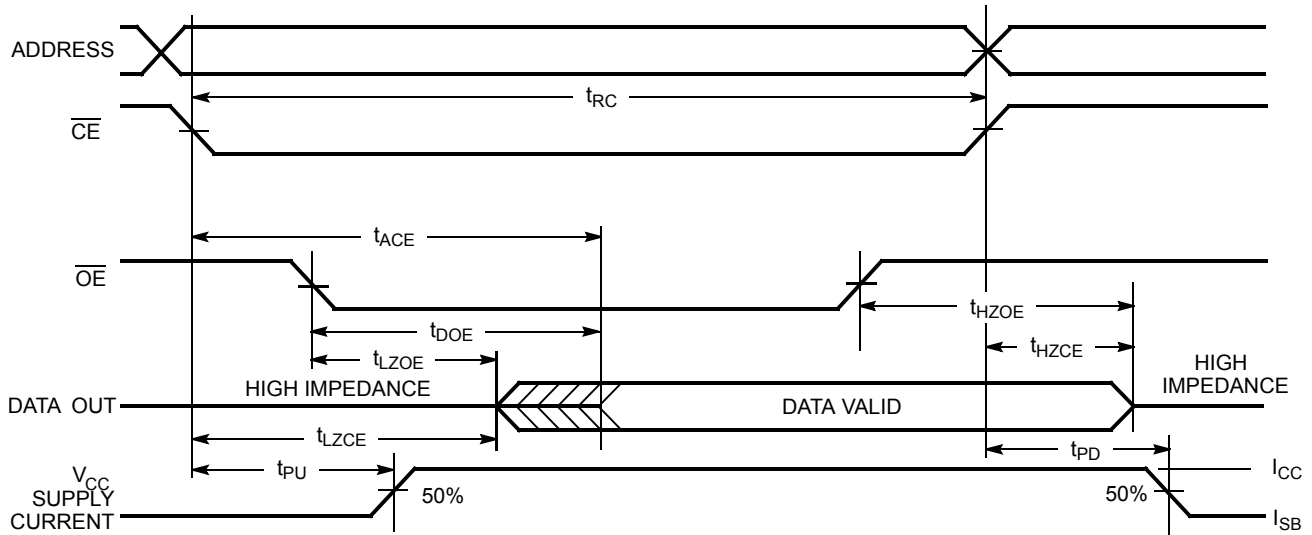
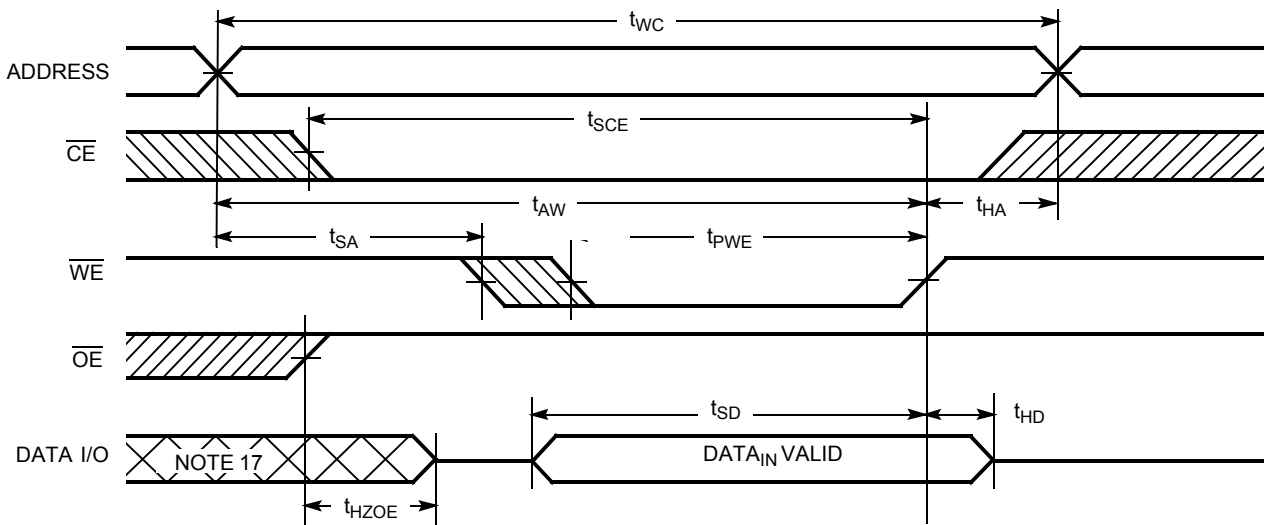


Figure 5. Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[16, 17]



Notes

- 13. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
- 14. WE is HIGH for read cycle.
- 15. Address valid prior to or coincident with \overline{CE} transition LOW.
- 16. Data IO is high impedance if $\overline{OE} = V_{IH}$.
- 17. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW)^[18]

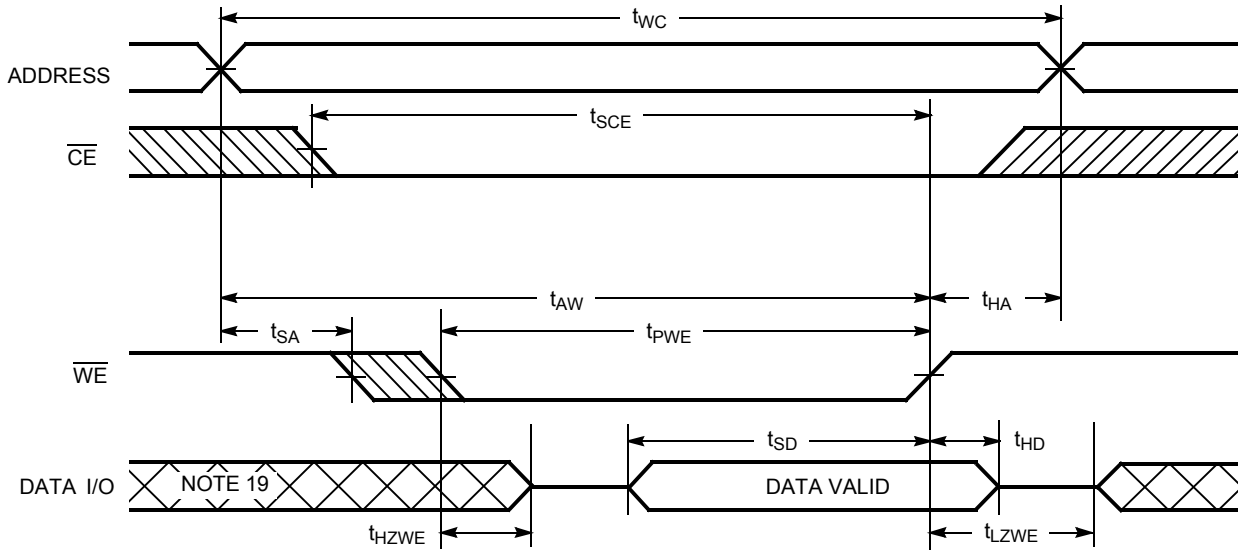
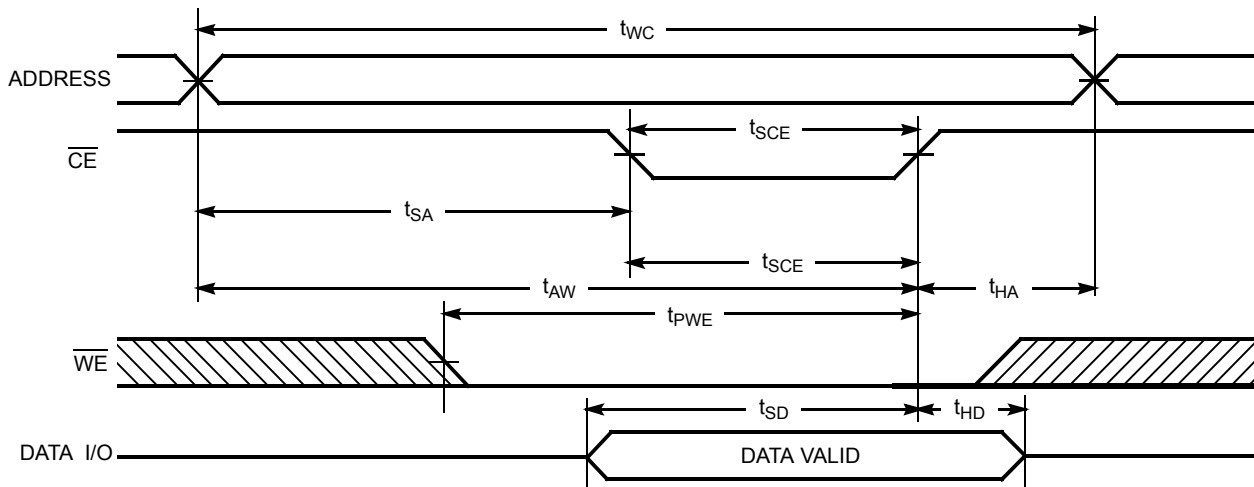


Figure 7. Write Cycle No. 3 (\overline{CE} Controlled)^[18, 20]



Notes

- 18. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.
- 19. During this period the IOs are in the output state and input signals must not be applied.
- 20. Data IO is high impedance if $\overline{OE} = V_{IH}$.

Truth Table

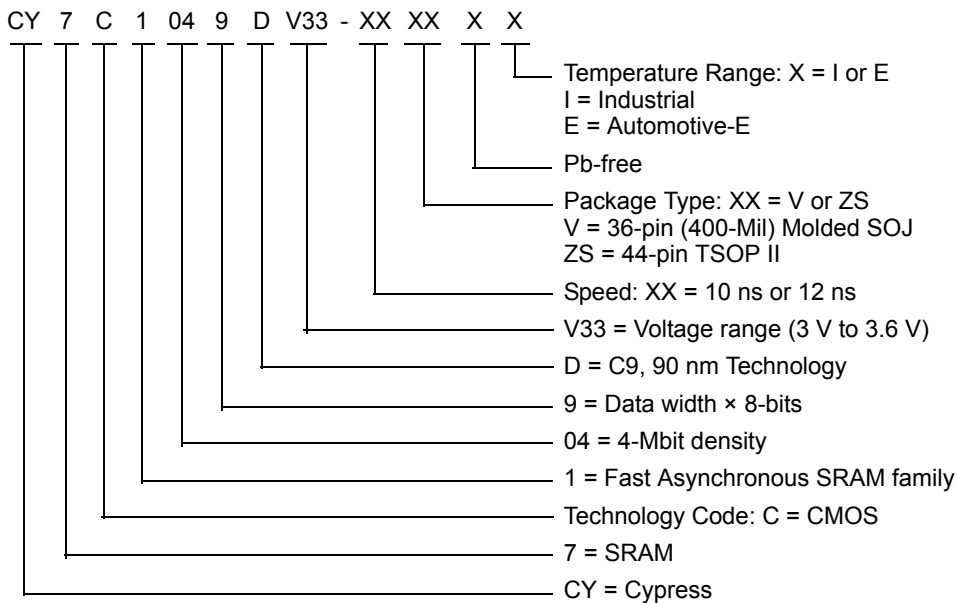
| \overline{CE} | \overline{OE} | \overline{WE} | IO_0 - IO_7 | Mode | Power |
|-----------------|-----------------|-----------------|-----------------|----------------------------|----------------------|
| H | X | X | High Z | Power down | Standby (I_{SB}) |
| L | L | H | Data Out | Read | Active (I_{CC}) |
| L | X | L | Data In | Write | Active (I_{CC}) |
| L | H | H | High Z | Selected, Outputs Disabled | Active (I_{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------------|--------------|---------------------------------------|-----------------|
| 10 | CY7C1049DV33-10VXI | 51-85090 | 36-pin (400-Mil) Molded SOJ (Pb-free) | Industrial |
| | CY7C1049DV33-10ZSXI | 51-85087 | 44-pin TSOP II (Pb-free) | |
| 12 | CY7C1049DV33-12VXE | 51-85090 | 36-pin (400-Mil) Molded SOJ (Pb-free) | Automotive |
| | CY7C1049DV33-12ZSXE | 51-85087 | 44-pin TSOP II (Pb-free) | |

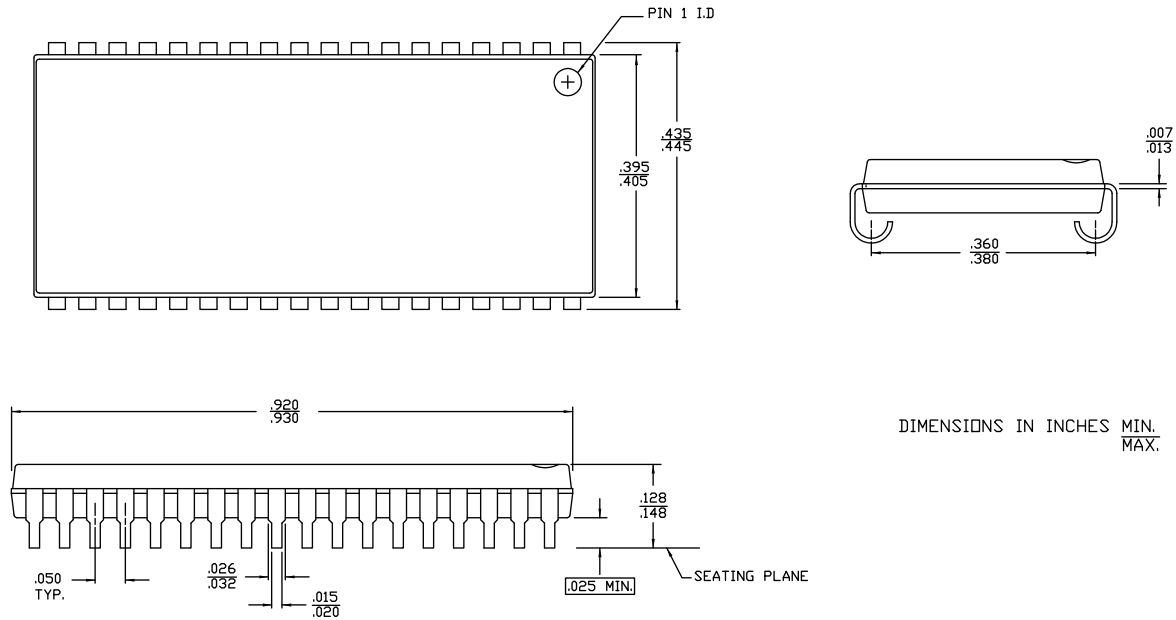
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 8. 36-pin (400-Mil) Molded SOJ V36.4, (51-85090)

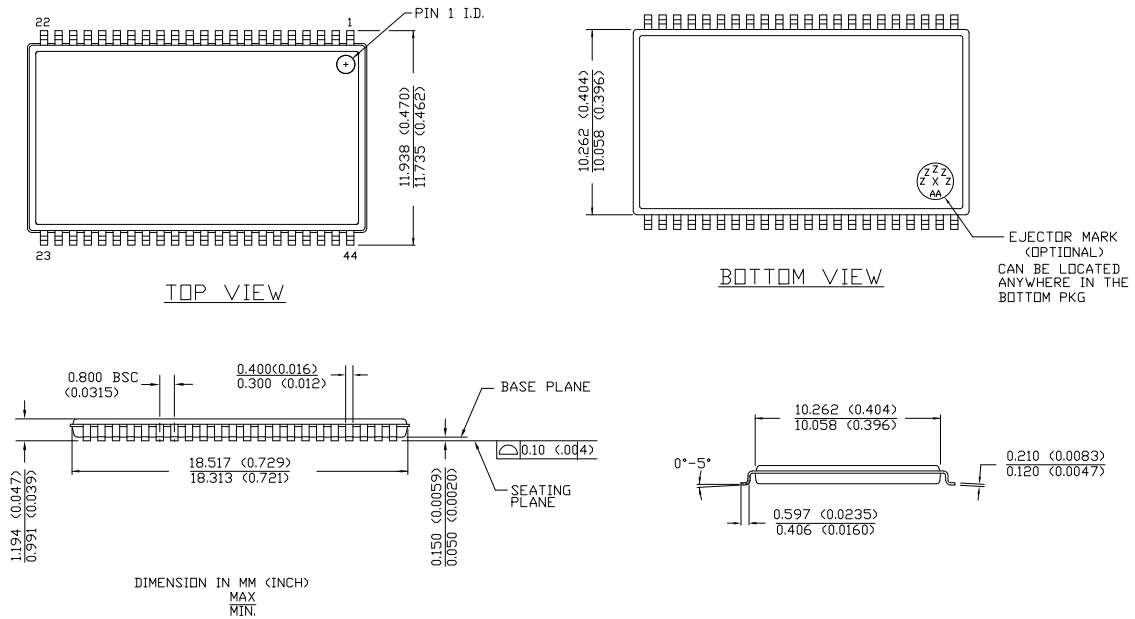


DIMENSIONS IN INCHES MIN. MAX.

51-85090 *E

Package Diagrams (continued)

Figure 9. 44-pin TSOP Z44-II, (51-85087)



51-85087 *C

Acronyms

| Acronym | Description |
|-----------------|---|
| \overline{CE} | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| \overline{OE} | output enable |
| SOJ | small outline J-lead |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| TTL | transistor-transistor logic |
| \overline{WE} | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celcius |
| MHz | Mega Hertz |
| μA | micro Amperes |
| μs | micro seconds |
| mA | milli Amperes |
| mm | milli meter |
| ms | milli seconds |
| ns | nano seconds |
| Ω | ohms |
| % | percent |
| pF | pico Farad |
| V | Volts |
| W | Watts |

Document History Page

| Document Title: CY7C1049DV33, 4-Mbit (512 K × 8) Static RAM | | | | |
|---|---------|------------|-----------------|---|
| Document Number: 38-05475 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 201560 | See ECN | SWI | Advance Datasheet for C9 IPP |
| *A | 233729 | See ECN | SYT | 1.AC, DC parameters are modified as per EROS (Specification # 01-2165) 2.Pb-free offering in the Ordering Information Table |
| *B | 351096 | See ECN | PCI | Changed from Advance to Preliminary Removed 20 ns Speed bin Corrected DC voltage (min) value in maximum ratings section from - 0.5 to - 0.3V Redefined I _{CC} values for Com'l and Ind'l temperature ranges I _{CC} (Com'l): Changed from 100, 80, and 67 mA to 90, 80 and, 75 mA for 8, 10, and 12ns speed bins respectively I _{CC} (Ind'l): Changed from 80 and 67 mA to 90 and 85 mA for 10 and 12ns speed bins respectively Added V _{IH(max)} specification in Note# 2 Changed reference voltage level for measurement of High Z parameters from ±500 mV to ±200 mV Added Data Retention Characteristics, Waveform, and footnotes 11 and 12 Changed Package Diagram name from 44-pin TSOP II Z44 to 44-pin TSOP II ZS44 Changed part names from Z to ZS in the Ordering Information Table Added 8 ns parts in the Ordering Information Table Added Pb-free Ordering Information Shaded Ordering Information Table |
| *C | 446328 | See ECN | NXR | Converted from Preliminary to Final Removed -8 speed bin Removed Commercial Operating Range product information Added Automotive Operating Range product information Updated Thermal Resistance table Updated footnote #8 on High Z parameter measurement Replaced Package Name column with Package Diagram in the Ordering Information table |
| *D | 1274726 | See ECN | VKN/AESA | Corrected typo in the 44-Pin TSOP II pinout |
| *E | 2899972 | 03/29/2010 | AJU | Updated Package Diagrams . |
| *F | 3059162 | 10/14/2010 | PRAS | Added Ordering Code Definitions . Updated Package Diagrams . |
| *G | 3266084 | 05/28/2011 | PRAS | Updated Functional Description (Removed "Refer to the Cypress application note AN1064, SRAM System Guidelines for best practice recommendations."). Added Acronyms and Units of Measure . Updated in new template. |

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