

SED1797D0B Series



Contents

Overview	1
Features	1
Block Diagram	2
Bump Layout	3
Bump Coordinates	4
Functions of Pins	7
Operations	9
Shift Data Transfer	9
Gate Output	10
Timing Chart	10
Absolute Maximum Ratings	11
Recommended Operating Conditions	12
Electrical Characteristics within Recommended Operating Conditions	13
DC Characteristics	13
AC Characteristics	14
Input Timing Characteristics	14
Output Timing Characteristics	14

Overview

SED1797 is a gate driver IC to drive the TFT-LCD panel. The amplitude of the gate output voltage is maximum 40V, enabling output of negative voltage.

This IC incorporates a power circuit for internal logic, eliminating the need to supply separate power source for internal logic.

The bump layout of this IC is compatible with COG implementation, and it is possible to achieve a narrow-framed and thin type module.

Features

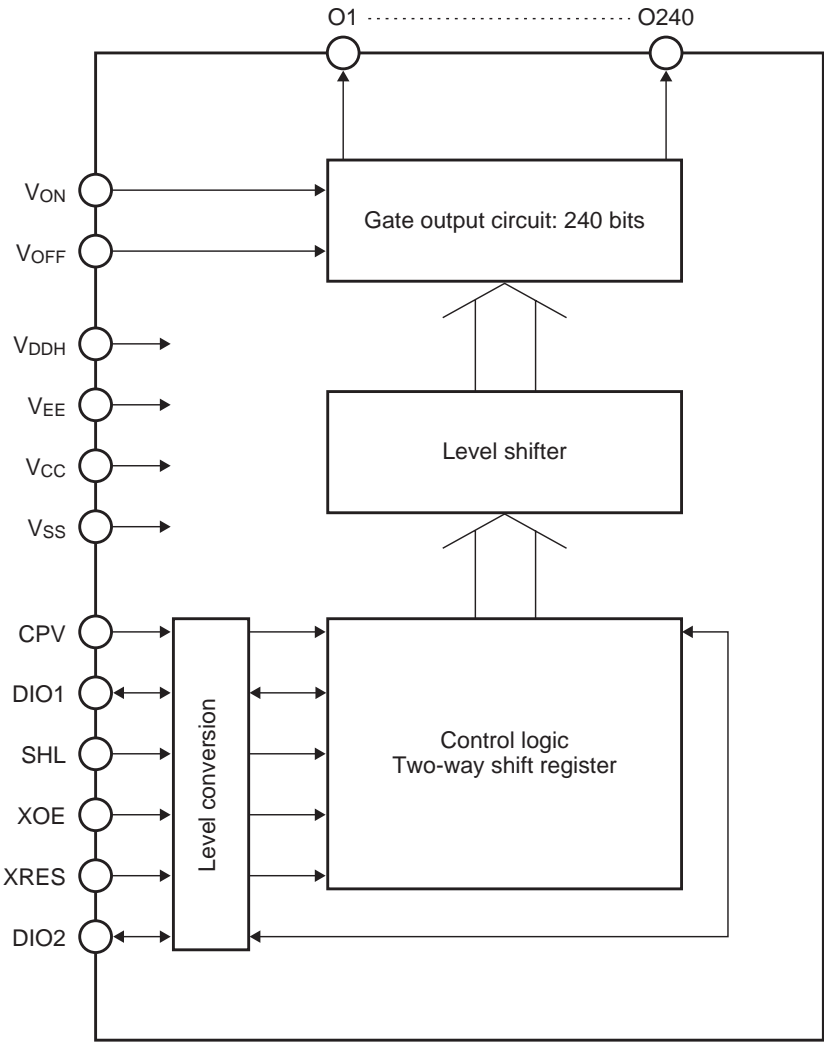
- Gate output voltage level: two values (V_{ON}/V_{OFF})
- Gate output voltage amplitude: Max. 40V
- Input signal amplitude: Min. 1.8V
- Number of gate drive outputs: 240
- Pin selection in the output shift direction is possible.
- Asynchronous reset of data in the shift register is possible.
- The level shift circuit enables output of negative voltage from the gate outputs
- Complete with a built-in power circuit for internal logic.
- This IC does not incorporate X-ray resistant or light-resistant design.

In using semiconductor devices, follow the precautions below.

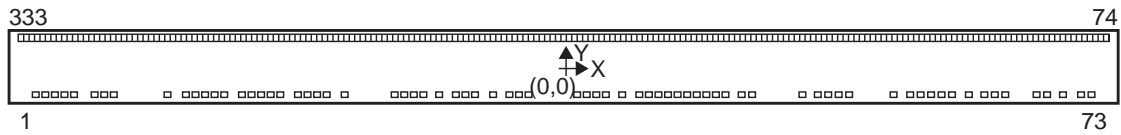
“Precautions for Handling the Product against Light”
Characteristics of semiconductor devices are affected when exposed to light. Therefore, this IC product may malfunction when exposed to light. In order to prevent malfunction of the IC due to exposure to light, take the following points in consideration for a substrate and any other product on which this IC is mounted.

- (1) Develop design and implementation methods to achieve a light-shielding IC structure in actual operation.
- (2) For the inspection process, prepare an environment where the light-shielding feature of the IC can be tested.
- (3) Light-shielding design should include considerations for light-shielding features of the front and backside surfaces as well as side faces of the IC.

Block Diagram



Bump Layout



Shipping form:	Chip
Chip size:	(X) 17.1 mm × (Y) 1.1 mm
Wafer thickness:	625μm
Bump shape:	Straight wall
Bump height (general standard)	15 ± 4μm
Deviation of bump height (within a chip):	Range of 4μm
Bump hardness:	30 to 70 HV
Bump size:	

(Unit: μm)

Pin	X	Y
Input	88	80
Output	45	80

Tolerance: ±4 μm

Bump Coordinates


Unit: μm

No.	Signal Name	X coordinate	Y coordinate	No.	Signal Name	X coordinate	Y coordinate	No.	Signal Name	X coordinate	Y coordinate
1	DUMMY	-8172.8	-420.6	51	VOFF	2466.4	-420.6	101	O27	6600.8	423.0
2	VDDH	-8024.8		52	DUMMY	2738.4		102	O28	6536.8	
3	VDDH	-7872.8		53	DUMMY	2867.5		103	O29	6472.8	
4	VDDH	-7716.8		54	DUMMY	3657.1		104	O30	6408.8	
5	DUMMY	-7568.8		55	CPV	3938.7		105	O31	6344.8	
6	VON	-7268.8		56	DUMMY	4086.7		106	O32	6280.8	
7	VON	-7116.8		57	DUMMY	4234.8		107	O33	6216.8	
8	VON	-6968.8		58	DUMMY	4382.7		108	O34	6152.8	
9	DUMMY	-6139.2		59	DUMMY	5074.7		109	O35	6088.8	
10	XRES	-5858.0		60	SHL	5356.3		110	O36	6024.8	
11	DUMMY	-5706.0		61	DUMMY	5508.3		111	O37	5960.8	
12	VCC	-5558.0		62	DUMMY	5656.3		112	O38	5896.8	
13	VCC	-5410.0		63	DUMMY	5804.2		113	O39	5832.8	
14	VCC	-5262.0		64	DIO2	5952.2		114	O40	5768.8	
15	VSS	-5037.1		65	DUMMY	6233.8		115	O41	5704.8	
16	VSS	-4889.1		66	DUMMY	6495.4		116	O42	5640.8	
17	VSS	-4741.1		67	DUMMY	6643.4		117	O43	5576.8	
18	VSS	-4589.1		68	DUMMY	6791.4		118	O44	5512.8	
19	DUMMY	-4370.7		69	DUMMY	7306.5		119	O45	5448.8	
20	DUMMY	-4118.7		70	DUMMY	7454.5		120	O46	5384.8	
21	DUMMY	-3970.7		71	DUMMY	7706.6		121	O47	5320.8	
22	DUMMY	-3822.7		72	DIO1	7988.2		122	O48	5256.8	
23	XOE	-3670.7		73	DUMMY	8136.2		123	O49	5192.8	
24	DUMMY	-3389.1		74	DUMMY	8356.0	423.0	124	O50	5128.8	
25	DUMMY	-2629.9		75	O1	8264.8		125	O51	5064.8	
26	DUMMY	-2477.9		76	O2	8200.8		126	O52	5000.8	
27	DUMMY	-2329.9		77	O3	8136.8		127	O53	4936.8	
28	VL	-2177.9		78	O4	8072.8		128	O54	4872.8	
29	DUMMY	-1959.5		79	O5	8008.8		129	O55	4808.8	
30	DUMMY	-1707.5		80	O6	7944.8		130	O56	4744.8	
31	DUMMY	-1559.5		81	O7	7880.8		131	O57	4680.8	
32	IPC	-1399.5		82	O8	7816.8		132	O58	4616.8	
33	DUMMY	-1117.9		83	O9	7752.8		133	O59	4552.8	
34	DUMMY	-865.9		84	O10	7688.8		134	O60	4488.8	
35	DUMMY	-717.9		85	O11	7624.8		135	O61	4424.8	
36	DUMMY	-570.0		86	O12	7560.8		136	O62	4360.8	
37	DUMMY	136.8		87	O13	7496.8		137	O63	4296.8	
38	DUMMY	284.8		88	O14	7432.8		138	O64	4232.8	
39	DUMMY	432.8		89	O15	7368.8		139	O65	4168.8	
40	TEST	580.8		90	O16	7304.8		140	O66	4104.8	
41	DUMMY	862.4		91	O17	7240.8		141	O67	4040.8	
42	DUMMY	1114.4		92	O18	7176.8		142	O68	3976.8	
43	DUMMY	1262.4		93	O19	7112.8		143	O69	3912.8	
44	VEE	1414.4		94	O20	7048.8		144	O70	3848.8	
45	VEE	1562.4		95	O21	6984.8		145	O71	3784.8	
46	VEE	1714.4		96	O22	6920.8		146	O72	3720.8	
47	DUMMY	1866.4		97	O23	6856.8		147	O73	3656.8	
48	DUMMY	2018.4		98	O24	6792.8		148	O74	3592.8	
49	VOFF	2166.4		99	O25	6728.8		149	O75	3528.8	
50	VOFF	2314.4		100	O26	6664.8		150	O76	3464.8	

Unit: μm

No.	Signal Name	X coordinate	Y coordinate	No.	Signal Name	X coordinate	Y coordinate	No.	Signal Name	X coordinate	Y coordinate
151	O77	3400.8	423.0	201	DUMMY	160.0	423.0	251	O159	-3080.8	423.0
152	O78	3336.8		202	DUMMY	96.0		252	O160	-3144.8	
153	O79	3272.8		203	DUMMY	32.0		253	O161	-3208.8	
154	O80	3208.8		204	DUMMY	-32.0		254	O162	-3272.8	
155	O81	3144.8		205	DUMMY	-96.0		255	O163	-3336.8	
156	O82	3080.8		206	DUMMY	-160.0		256	O164	-3400.8	
157	O83	3016.8		207	DUMMY	-224.0		257	O165	-3464.8	
158	O84	2952.8		208	DUMMY	-288.0		258	O166	-3528.8	
159	O85	2888.8		209	DUMMY	-325.0		259	O167	-3592.8	
160	O86	2824.8		210	DUMMY	-416.0		260	O168	-3656.8	
161	O87	2760.8		211	DUMMY	-480.0		261	O169	-3270.8	
162	O88	2696.8		212	DUMMY	-544.0		262	O170	-3784.8	
163	O89	2632.8		213	O121	-648.8		263	O171	-3848.8	
164	O90	2568.8		214	O122	-712.8		264	O172	-3912.8	
165	O91	2504.8		215	O123	-776.8		265	O173	-3976.8	
166	O92	2440.8		216	O124	-840.8		266	O174	-4040.8	
167	O93	2376.8		217	O125	-904.8		267	O175	-4104.8	
168	O94	2312.8		218	O126	-968.8		268	O176	-4168.8	
169	O95	2248.8		219	O127	-1032.8		269	O177	-4232.8	
170	O96	2184.8		220	O128	-1096.8		270	O178	-4296.8	
171	O97	2120.8		221	O129	-1160.8		271	O179	-4360.8	
172	O98	2056.8		222	O130	-1224.8		272	O180	-4424.8	
173	O99	1992.8		223	O131	-1288.8		273	O181	-4488.8	
174	O100	1928.8		224	O132	-1352.8		274	O182	-4552.8	
175	O101	1864.8		225	O133	-1416.8		275	O183	-4616.8	
176	O102	1800.8		226	O134	-1480.8		276	O184	-4680.8	
177	O103	1736.8		227	O135	-1544.8		277	O185	-4744.8	
178	O104	1672.8		228	O136	-1608.8		278	O186	-4808.8	
179	O105	1608.8		229	O137	-1672.8		279	O187	-4872.8	
180	O106	1544.8		230	O138	-1736.8		280	O188	-4936.8	
181	O107	1480.8		231	O139	-1800.8		281	O189	-5000.8	
182	O108	1416.8		232	O140	-1864.8		282	O190	-5064.8	
183	O109	1352.8		233	O141	-1928.8		283	O191	-5128.8	
184	O110	1288.8		234	O142	-1992.8		284	O192	-5192.8	
185	O111	1224.8		235	O143	-2056.8		285	O193	-5256.8	
186	O112	1160.8		236	O144	-2120.8		286	O194	-5320.8	
187	O113	1096.8		237	O145	-2184.8		287	O195	-5384.8	
188	O114	1032.8		238	O146	-2248.8		288	O196	-5448.8	
189	O115	968.8		239	O147	-2312.8		289	O197	-5512.8	
190	O116	904.8		240	O148	-2376.8		290	O198	-5576.8	
191	O117	840.8		241	O149	-2440.8		291	O199	-5640.8	
192	O118	776.8		242	O150	-2504.8		292	O200	-5704.8	
193	O119	712.8		243	O151	-2568.8		293	O201	-5768.8	
194	O120	648.8		244	O152	-2632.8		294	O202	-5832.8	
195	DUMMY	544.0		245	O153	-2696.8		295	O203	-5896.8	
196	DUMMY	480.0		246	O154	-2760.8		296	O204	-5960.8	
197	DUMMY	416.0		247	O155	-2824.8		297	O205	-6024.8	
198	DUMMY	352.0		248	O156	-2888.8		298	O206	-6088.8	
199	DUMMY	288.0		249	O157	-2652.8		299	O207	-6152.8	
200	DUMMY	224.0	▼	250	O158	-3016.8	▼	300	O208	-6216.8	▼

Unit: μm

No.	Signal Name	X coordinate	Y coordinate
301	O209	-6280.8	423.0
302	O210	-6344.8	
303	O211	-6408.8	
304	O212	-6472.8	
305	O213	-6536.8	
306	O214	-6600.8	
307	O215	-6664.8	
308	O216	-6728.8	
309	O217	-6792.8	
310	O218	-6856.8	
311	O219	-6920.8	
312	O220	-6984.8	
313	O221	-7048.8	
314	O222	-7112.8	
315	O223	-7176.8	
316	O224	-7240.8	
317	O225	-7304.8	
318	O226	-7368.8	
319	O227	-7432.8	
320	O228	-7496.8	
321	O229	-7560.8	
322	O230	-7624.8	
323	O231	-7688.8	
324	O232	-7752.8	
325	O233	-7816.8	
326	O234	-7880.8	
327	O235	-7944.8	
328	O236	-8008.8	
329	O237	-8072.8	
330	O238	-8136.8	
331	O239	-8200.8	
332	O240	-8264.8	
333	DUMMY	-8356.0	

Functions of Pins

Pin Name	I/O	Function	Number of Pins															
CPV	1	Vertical shift clock input pin The vertical shift clock is the shift clock in the shift register. Data shift, synchronizing with the rising-edge of this shift clock.	1															
DIO1 DIO2	I/O	Shift data input/output pins These are data I/O pins to and from the shift registers. When data are input, they are captured, synchronizing with the rising-edge of CPV, and data are output, synchronizing with the falling edge. I/O of DIO1 and DIO2 is switched by the level set by SHL. The output level is always "Vcc"- "Vss."	2															
SHL	I	Pin for selecting the shift direction and for switching the I/O function of the shift data I/O pin This pin selects the shift direction and switches I/O of the shift data I/O pins. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>SHL</th> <th colspan="2">Gate Output</th> <th>DIO1</th> <th>DIO2</th> </tr> </thead> <tbody> <tr> <td>Vcc</td> <td>O1</td> <td style="text-align: center;">→</td> <td>O240</td> <td>Input</td> </tr> <tr> <td>Vss</td> <td>O1</td> <td style="text-align: center;">←</td> <td>O240</td> <td>Output</td> </tr> </tbody> </table>	SHL	Gate Output		DIO1	DIO2	Vcc	O1	→	O240	Input	Vss	O1	←	O240	Output	1
SHL	Gate Output		DIO1	DIO2														
Vcc	O1	→	O240	Input														
Vss	O1	←	O240	Output														
XOE	I	Output enable pin This is a pin that controls the gate output pins (O1 - O240). XOE="Vcc" : VOFF voltage output XOE="Vss" : Normal output status	1															
XRES	I	Reset pin Setting XRES = "Vss" resets data in all the shift registers. The gate output voltage is set to the "VOFF" level.	1															
TEST	I	Test pin Fix this pin to the "VEE" level.	1															
IPC	I	Built-in power control pin Fix this pin to the "VEE" level.	1															

Pin Name	I/O	Function	Number of Pins
O1 to O240	0	Gate output pins Data in the shift register are output after level conversion.	240
VON	Power supply	Power for gate output $V_{EE} \leq V_{OFF} \leq V_{ON} \leq V_{DDH}$	TBD
VOFF	Power supply	Power for gate output $V_{EE} \leq V_{OFF} \leq V_{ON} \leq V_{DDH}$	TBD
VDDH	Power supply	Power supply for high-voltage logic $V_{ON} \leq V_{DDH}$	TBD
VEE	Power supply	Power supply for logic (ICs' shared power supply) $V_{EE} \leq V_{OFF}$	TBD
VCC	Power supply	Power supply for logic $V_{EE} \leq V_{DDH}$	TBD
VSS	Power supply	GND $V_{EE} \leq V_{SS}$	TBD
VL	0	Test pin for internal logic power supply. Set it to "OPEN."	1
DUMMY	N/A	Dummy bump Auxiliary bump for COG implementation. Electrically, it is "OPEN."	TBD

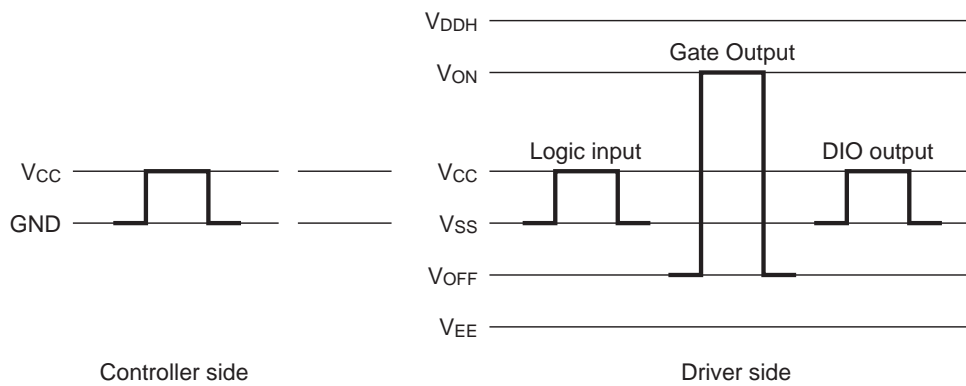
Operations

Shift Data Transfer

Data input from one of the DIO pins are captured at the rising-edge of the shift clock CPV, to be sequentially shifted, synchronizing with the rising-edge of CPV, then to be output to the other DIO, synchronizing with the falling edge of the 240th CPV.

SHL	Data Input Pin	Shift Direction	Data Output Pin
Vcc	DIO1	O1→O2.....O239→O240	DIO2
Vss	DIO2	O240→O239.....O2→O1	DIO1

To cascade-connect more than one ICs, connect the DIO output of the first IC to the DIO input of the next IC.



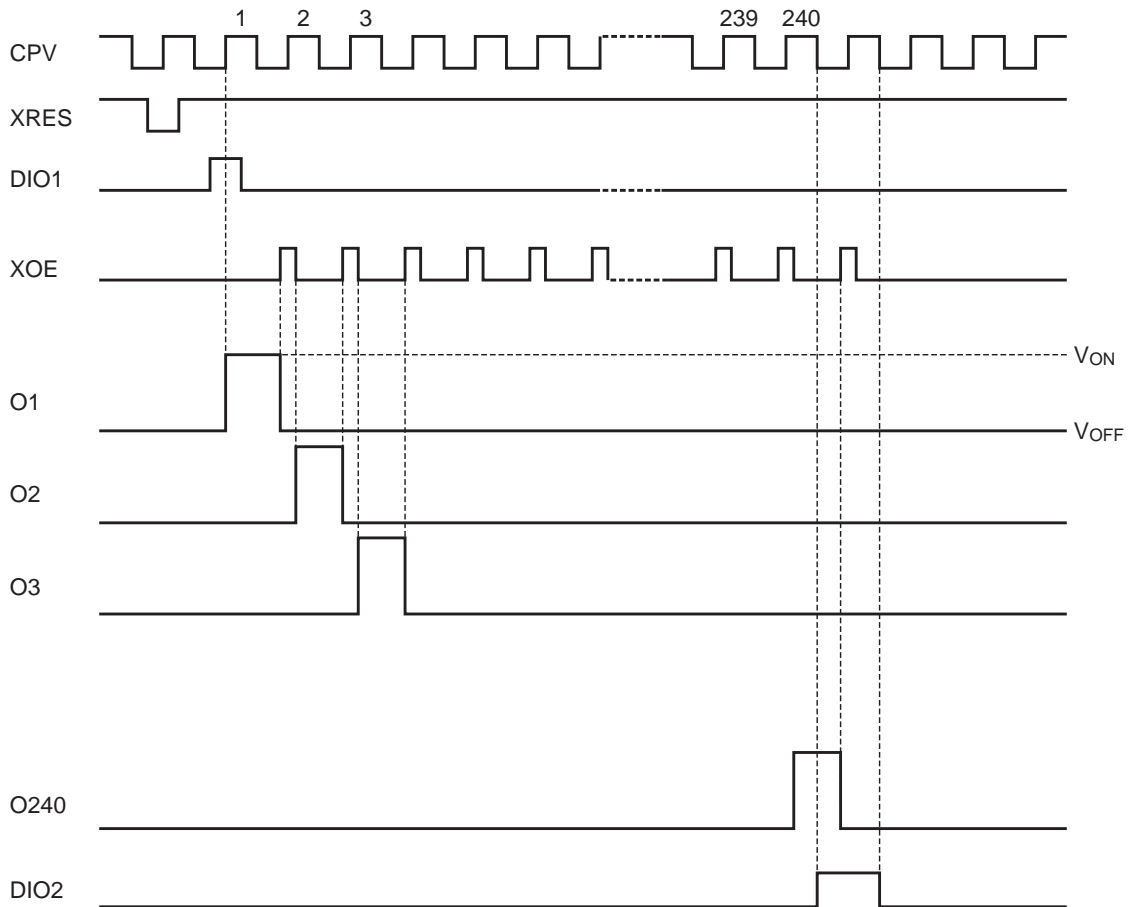
Gate Output

“VON” voltage is output while “H” level ON signals are output for data in the shift registers associated with the respective gate output pins, and “VOFF” voltage is output while “L” level OFF signals are output. Inputting “L” level to the reset pin (XRES) resets data in all the shift registers and “VOFF” voltage is applied for gate output.

If the reset pin is not used, inputting 240 clocks clears data in all the shift registers with shift data input fixed to the “L” level. Note, however, gate output during this initialization period becomes indefinite.

Timing Chart

Case: SHL = “VCC” (reference example)



Absolute Maximum Ratings (VSS = 0V)

Item	Symbol	Rating	Unit
Supply voltage (1)	VCC	-0.3 to +7.0	V
Supply voltage (2)	VDDH	-0.3 to +45.0	V
Supply voltage (3)	VEE	-23.0 to +0.3	V
Supply voltage (4)	VDDH-VEE VON-VOFF	-0.3 to +45.0	V
Supply voltage (5)	VON	-0.3 to +VDDH+0.3	V
Supply voltage (6)	VOFF	VEE-0.3 to +0.3	V
Input voltage	VIN	-0.3 to VCC+0.3	V
Input current	IIN	±10	mA
Output current operating ambient	IO	±10	mA
Temperature range	Ta	-40 to +85	°C
Storing temperature	Tstg2	-55 to +125	°C

(Note 1) Unless otherwise noted, VSS is the reference voltage for all voltages.

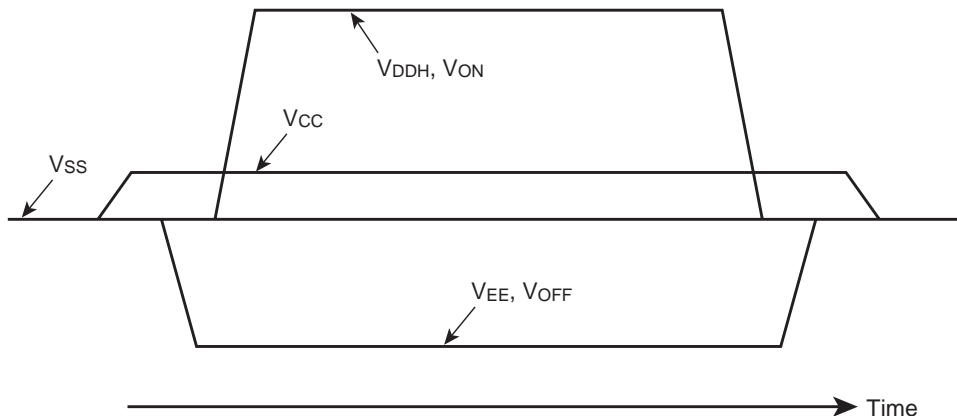
(Note 2) The IC may be permanently damaged if it is operated under conditions beyond the above ratings. Also note that reliability of the IC may be affected if it is exposed to a condition with the absolute maximum ratings for a long time.

(Note 3) As for voltages of VDDH, VEE, VCC and VSS, always maintain the relation $VEE \leq VSS \leq VCC \leq VDDH$. Additionally, maintain such condition for VON and VOFF that the relations, $VEE \leq VOFF$ and $VON \leq VDDH$, are always present.

(Note 4) To input power, follow the order below: Logic system 1 (VCC, VSS) → Logic system 2 (VEE) → high-voltage logic system (VDDH) → gate output system (VON, VOFF) → logic signals, in this order. Or input power to all simultaneously. To shut down, follow this order inversely or disconnect all at the same time. Take care as well so that the relations between the levels of the power voltages would not reversed even while power is input, disconnected or in transient.

(Note 5) Input logic signals at the same time as power input to Logic System 1 (VCC, VSS) or during the power inputting process. Meanwhile, the operations of the IC are assured if it is operated within the recommended operating conditions.

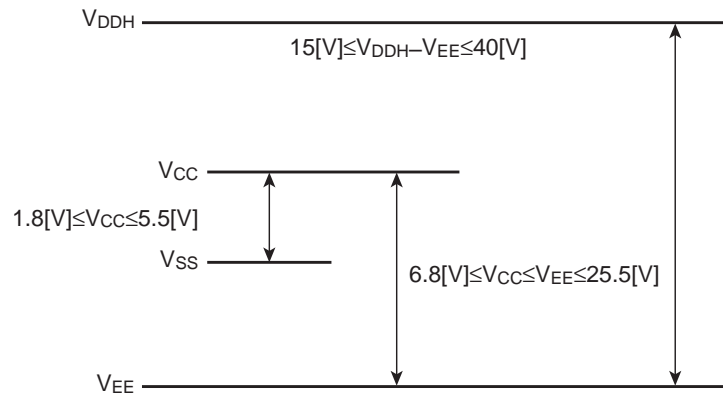
(Note 6) Avoid floating of the logic power while the high-voltage logic power or gate output power is applied. Avoid a condition where VCC-VEE becomes 0.7V or under as well. These conditions may affect reliability of the IC.



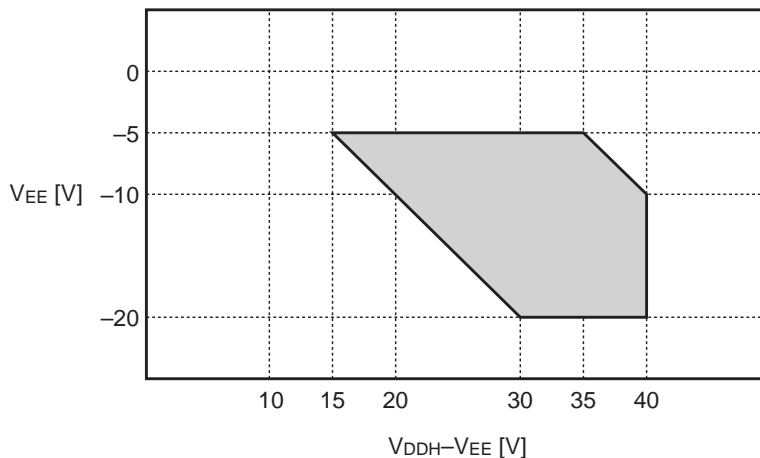
Recommended Operating Conditions (VSS = 0V)

Item	Symbol	Rating	Unit
Supply voltage (1)	VCC	+1.8 to +5.5	V
Supply voltage (2)	VDDH, VON	+10.0 to +30.0	V
Supply voltage (3)	VEE, VOFF	-20.0 to -5.0	V
Supply voltage (4)	VDDH-VEE VON-VOFF	+15.0 to +40.0	V
Operating frequency	fCPV	DC to 200	kHz

- (Note 1) The operations of the IC are assured if it is operated within the recommended operations conditions.
- (Note 2) Insert a bypass capacitor in the vicinity of the power pins as countermeasures against noise.
- (Note 3) If the voltage of VOFF power supply is not swung, keep VOFF at the same potential as that of VEE.
- (Note 4) As for the swing of the VOFF power voltage, maintain the relation $V_{EE} \leq V_{OFF} \leq V_{ON} - 15[V]$. In this case, different assurance standards are applied to the output resistance, output rise time and output fall time.
- (Note 5) When inputting power, it is recommended that the reset pin should be fixed to the “L” level and gate output to “VOFF” voltage. This prevents gate output from becoming indefinite and also prevents overcurrent as well as faulty display on the LCD panel.



The recommended operating voltages are combinations within the shaded area in the figure below.



Electrical Characteristics within Recommended Operating Conditions

DC Characteristics

($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 3.3 \pm 0.3\text{V}$, $V_{SS} = 0\text{V}$, $V_{DDH} = 30\text{V}$, $V_{EE} = -10\text{V}$)

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			MIN.	TYP.	MAX.		
"L" input voltage	V_{IL}		V_{SS}		$V_{SS} + 0.3 \times (V_{CC} - V_{SS})$	V	All input pins
"H" input voltage	V_{IH}		$V_{SS} + 0.7 \times (V_{CC} - V_{SS})$		V_{CC}	V	All input pins
"L" output voltage	V_{OL}	$I_{OL} = 40\mu\text{A}$	V_{SS}		$V_{SS} + 0.4$	V	DIO1 DIO2
"H" output voltage	V_{OH}	$I_{OH} = 40\mu\text{A}$	$V_{SS} + 0.8 \times (V_{CC} - V_{SS})$		V_{CC}	V	DIO1 DIO2
Output resistance	R_{ON}	$\Delta V_{ON} = 0.5\text{V}$ $V_{ON} = 30\text{V}$ $V_{OFF} = -10\text{V}$			1.0	k	O1 to O240
Input leakage current	I_{LI}		-1.0		+1.0	μA	All input pins
Input capacity	C_{IN}	$T_a = 25^\circ\text{C}$			15	pF	All input pins
Static current consumption (1)	I_{CCS}	*1		100	300	μA	V_{CC}
Static current consumption (2)	I_{DDs}			50	150	μA	V_{DDH}
Static current consumption (3)	I_{SSs}			-10	-30	μA	V_{SS}
Static current consumption (4)	I_{EES}			-150	-450	μA	V_{EE}
Dynamic current consumption (1)	I_{CC}	*2		200	400	μA	V_{CC}
Dynamic current consumption (2)	I_{DD}			100	200	μA	V_{DDH}
Dynamic current consumption (3)	I_{SS}			-10	-20	μA	V_{SS}
Dynamic current consumption (4)	I_{EE}			-300	-600	μA	V_{EE}

*1: SHL="H", XRES="H", DIO1=CPV=XOE="L", DIO2="OPEN", no load on the output pins.

*2: VGA display, fCPV=36 kHz, fDIO=75 Hz, no load on the output pins.

AC Characteristics

Input Timing Characteristics

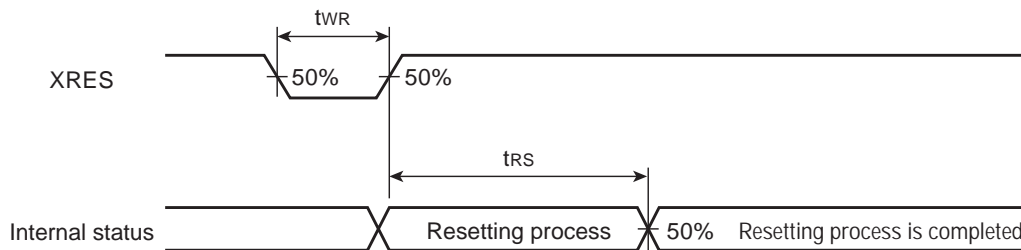
($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 3.3 \pm 0.3\text{V}$, $V_{SS} = 0\text{V}$, $V_{DDH} = 30\text{V}$, $V_{EE} = -10\text{V}$)

Item	Symbol	Condition	MIN.	MAX.	Unit
CPV frequency	tCPV		5.0		μs
CPV high-level pulse width	tCPVH		0.9		μs
CPV low-level pulse width	tCPVL		0.9		μs
Data setup time	tDS		300		ns
Data hold time	tDH		300		ns
XRES low-level pulse length	tWR		1.0(*2)		μs
Reset time	tRS			5.0(*2)	μs
High-level pulse length	tWOE		1.0(*3)		μs

*1: The rise and fall times of input signals (t_r and t_f) are defined as 30ns or less.

*2: This value is not applied if XRES is not used.

*3: This value is not applied if XOE is not used.



Output Timing Characteristics

($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 3.3 \pm 0.3\text{V}$, $V_{SS} = 0\text{V}$, $V_{DDH} = 30\text{V}$, $V_{EE} = -10\text{V}$)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPV-to-DIO output delay time	tpd1	CL=20pF		0.6	1.5	μs
	tpd2			0.6	1.5	μs
CPV-to-DIO output delay time	tpd3	CL=220pF		0.4	1.5	μs
	tpd4			VON=30V	0.4	1.5
XOE-to-On output delay time	tpd5	VOFF=10V		0.6	1.5	μs
	tpd6			0.6	1.5	μs
On output rise time	tor		0.4	1.8	μs	
On output fall time	tof		0.4	1.8	μs	

